Small-Area, Low-Power Circuits and Systems for Ultrasound Matrix Probes

September 2025

Shinya Kajiyama

A Thesis for the Degree of Ph.D. in Engineering

Small-Area, Low-Power Circuits and Systems for Ultrasound Matrix Probes

September 2025

Graduate School of Science and Technology

Keio University

Shinya Kajiyama

Abstract

Medical ultrasound imaging diagnosis is a widely used modality due to its safety, real-time capability, and low cost. However, it also involves issues that depend on the examiner's skills, which can affect image quality and examination throughput. This study examines the technologies required for small-area and low-power dissipation in application-specific integrated circuits (ASICs) for two-dimensional array matrix probes capable of volumetry imaging without skills. Additionally, it explores the technologies required to achieve both high spatial resolution and signal-to-noise ratio (SNR) in the deep regions of the human body.

Chapter 1 summarizes the background and issues related to ASIC-embedded matrix probes.

Chapter 2 examined ASIC specifications based on system requirements.

Chapter 3 describes the details of the novel time-shared configurable transmit (TX)/receive (RX) beamformer, which is implemented in each of the 3072-channel transceivers in the ASIC and has a significant impact on area and power dissipation. The digital TX bus signal is delayed by parallel delayers for RX, allowing for a compact and low-power configuration without requiring an extra first-in-first-out (FIFO) memory. The proposed circuit configuration achieved a single-channel transceiver circuit area of 300 μm × 300 μm and power dissipation of 0.74 mW/channel.

Chapter 4 describes the details of the novel TX/RX isolation switch (TRSW), which protects low-voltage RX from high-voltage TX pulse, using only three high-voltage MOSFETs, resulting in a small area and low power operation. The proposed dynamic shunt architecture ensures the switch is in the off state with only a low-voltage MOSFET circuit and requires only one high-voltage MOSFET for on/off control. Furthermore, a per-channel loopback test function is provided to verify the signal continuity of the 3072-channel transceiver without probing the 3072 electrodes.

Chapter 5 describes the details of a continuous-time pulse compressor (CTPC) that achieves both signal enhancement and higher axial spatial resolution by transmitting a chirp waveform and compressing pulses at the RX, thereby resolving the trade-off between SNR and axial spatial resolution in burst TX. The RX signal is compressed in the time domain by passing it through a proposed CTPC whose delay varies linearly with frequency, and the pulse peak is enhanced by 6.7 dB. Furthermore, improvement in spatial resolution was verified by acoustic measurements and brightness (B)-mode imaging.

Chapter 6 summarizes the results of this study and further discusses prospects.

Acknowledgements

This research was conducted in the Ishikuro Laboratory, School of Integrated Design Engineering, Graduate School of Science and Technology, Keio University, under the mentorship of Professor Hiroki Ishikuro. I would like to express my deepest gratitude to Prof. Ishikuro for his guidance and encouragement in the execution of this research.

I would also like to express my sincere gratitude to Prof. Nobuhiko Nakano, Prof. Takahisa Mitsui of the Faculty of Medicine, Associate Prof. Kentaro Yoshioka, Prof. Tetsuya Iizuka of the University of Tokyo, and Assistant Prof. Yosuke Shiiki for their valuable guidance and advice on this thesis.

I would like to express my deepest gratitude to the students in Ishikuro Laboratory, especially Mr. Shuya Nakagawa, Mr. Nobuhiro Toneyama, and Mr. Kaoru Yamashita, and the students in Nakano Laboratory, especially Mr. Mizuki Mori, Mr. Yuki Koroyasu, Mr. Tomonari Nagata, and Mr. Yu Watanabe for their cooperation in technical discussions, circuit design, building signal processing software, and experiments in conducting this research.

A part of this research was conducted at the Research and Development Group and Healthcare Business Unit of Hitachi, Ltd. I would like to express my gratitude to the following people for their support. Dr. Tatsuo Nakagawa, Mr. Yasuyuki Okuma, Mr. Yohei Nakamura, Dr. Takahide Terada, Mr. Taizo Yamawaki, Dr. Hiroki Tanaka Mr. Yutaka Igarashi, Dr. Toru Yazaki, Mr. Yusaku Katsube, Mr. Takuma Nishimoto, Mr. Yoshihiro Hayashi, Mr. Kazuhiro Amino, and Mr. Takuya Kaneko.

Finally, I would like to express my deepest gratitude to my beloved wife, Asako, who fully supported me in my research and pursuit of a Ph.D. degree while working full-time at a company; to my beloved dog, Jacqueline, who brought me peace and comfort during my busy days; and to my parents, who supported me until I became a working adult and have continued to watch over me with warmth and kindness.

Contents

List of Figures

List of Tables

Abbreviations

1dBGCP	1-dB Gain Compression Point
AAF	Antialiasing Filter
ABF	Analog Beamforming
ADC	Analog-to-Digital Converter
AFE	Analog Front-End
AM	Amplitude Modulation
AMUX	Analog Multiplexer
AoV	Angle of View
APF	All-Pass Filter
ASIC	Application-Specific Integrated Circuit
BBD	Bucket-Brigade Device
BCD	Bipolar CMOS DMOS
BDR-SCD	Bidirectional Dynamic-Reconfigurable Switched-Capacitor Delayer
BF	Beamforming
B-mode	Brightness mode
BPF	Band-Pass Filter
CFM	Color Flow Mapping
CMUT	Capacitive Micromachined Ultrasonic Transducer
CPU	Central Processing Unit
CRM	Capacitor Ring Memory
CT	Conputed Tomography
CTPC	Continuous-Time Pulse Compressor
CW	Continuous Wave
DAC	Digital-to-Analog Converter
DAS	Delay and Sum
DBF	Digital Beamformer
DDL	Dispersive Delay Line
D-FF	D-Flip Flop
DMOS	Double-diffused MOS
DR	Dynamic Range
DSP	Digital Signal Processor

EBG	Electromagnetic Bandgap
ECh	Element Channel
EF	Ejection Fraction
FIFO	First-In First-Out
FPC	Flexible Printed Circuit
FPGA	Field Programmable Gate Array
FWHM	Full Width at Half Maximum
GBW	Gain Bandwidth Product
GD	Group Delay
gm-C	Transconductor-Capacitor
HIV	Human Immunodeficiency Virus
HV	High Voltage
HVSW	High-Voltage Switch
IC	Integrated Circuit
IIP3	Third-Order Input Intercept Point
I/Q	In-phase/Quadrature
LDMOS	Laterally Diffused MOS
LNA	Low Noise Amplifier
LPF	Low-Pass Filter
LTCC	Low-Temperature Co-fired Ceramic
LV	Low Voltage
LVDS	Low Voltage Differential Signal
μBF	Microbeamforming
MEMS	Micro Electro Mechanical System
MIM	Metal-Insulator-Metal
M-mode	Motion mode
MRI	Magnetic Resonance Imaging
MSB	Most Significant Bit
NF	Noise Figure
OPA	Operational Amplifier
PA	Power Amplifier
PC	Pulse Compression
PCB	Printed Circuit Board
Pcell	Parameterized Cell
PMN-PT	$Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$

PMUT	Piezoelectric Micromachined Ultrasonic Transducer
POC	Point of Care
PP	Push-Pull
PSF	Point Spread Function
PZT	Lead Zirconate Titanate $Pb(Zr, Ti)O_3$
Q	Quality Factor
RF	Radio Frequency
RX	Receiver
RZ	Return to Zero
S/H	Sample-and-Hold
SAR	Successive Approximation Register
SCD	Switched Capacitor Delayer
SCh	Subarray Channel
SERDES	Serializer/Deserializer
SJ-LDMOS	Super-Junction Laterally-Diffused MOS
SNR	Signal-to-Noise Ratio
SOI	Silicon on Insulator
SPI	Serial Peripheral Interface
STRB	Strobe
SW	Switch
TD	Transducer
TEG	Test Element Group
TGC	Time Gain Control
THI	Tissue Harmonic Imaging
TRSW	Transmit/Receive isolation switch
TX	Transmitter
UWB	Ultra-Wide Band
VCM	Common Voltage
VOH	Output High Logic Level
VOL	Output Low Logic Level

Chapter 1
Introduction

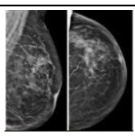
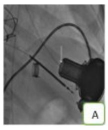
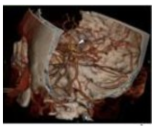
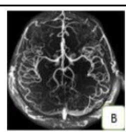
1.1 Ultrasound Imaging as a Medical Modality

Differences significantly influence the diagnosis of diseases around the world in demographics, sanitation, and healthcare systems. The aging population in developed countries makes early diagnosis of chronic diseases such as heart disease, diabetes, and cancer important. In addition, obesity is increasing worldwide due to urbanization and dietary changes. While advanced diagnostic technologies have become widespread in developed countries, health checkups and screenings as a form of preventive medicine are becoming increasingly common, medical costs remain high and are influenced by insurance systems. It is necessary to reduce the burden on healthcare providers and cut total costs, including not only the cost of medical equipment but also operating costs and personnel expenses associated with operating and managing the equipment. On the other hand, infectious diseases such as malaria, tuberculosis, and human immunodeficiency virus (HIV) remain major health problems in developing countries, and delays in diagnosing infectious diseases lead to high mortality rates. Since developing countries often lack adequate medical infrastructure and have limited access to diagnostic equipment, portable mobile diagnostic technology and telemedicine are desirable for the future.

Medical ultrasound imaging is an examination method in which ultrasound waves are irradiated into a living body, and the reflected waves (echoes) are visualized. Unlike other imaging modalities that use radiation, ultrasound is safe and does not expose the patient to radiation, and it is the only modality that can be used on a fetus before birth. Furthermore, unlike computed tomography (CT) and magnetic resonance imaging (MRI), which occupy space and are expensive to install, ultrasound systems are compact, cart-type, and relatively inexpensive. In addition, ultrasound can achieve a frame rate of more than 100 frames per second, compared to MRI's maximum of 10 frames per second, which is superior in real-time performance. It can also be synchronized with electrocardiography to observe heart movement.

Table 1.1 shows a comparison of medical imaging modalities. This table is a reorganized version of Table 1 in reference [1] with additional images as examples. All modalities are non-invasive methods for visualizing the inside of the human body without the need for surgical incision. However, there are pros and cons related to spatial resolution, contrast, real-time performance, cost, and safety, including heat and radiation exposure. The risks and benefits must be considered in their operation [1]. As mentioned earlier, ultrasound is superior in terms of real-time imaging, safety, and cost, as it does not use radiation and instead deals with mechanical information, and the equipment is compact. On the other hand, ultrasound is totally reflected by hard tissues, such as bones, and air-containing tissues, like the lungs, limiting the examination to soft tissues. In addition, the higher the frequency of the ultrasound, the better the spatial resolution;

Table 1.1 Comparison between medical imaging modalities. Summarized from [1].

Modality	X-ray Radiography	Mammography	Fluoroscopy	Computed Tomography	Magnetic Resonance Imaging	Ultrasound Imaging
Spatial resolution	1 mm	1 mm	1 mm	0.5 mm	0.5 mm	1 mm
Contrast	Soft and fluid contrast good	Soft tissue contrast good	Soft and hard contrast good	Soft and hard tissue contrast very good	Soft tissue contrast very good	Soft and fluid tissue contrast good
Real time availability	No	No	No	No	No	**Yes**
System cost	Medium	Medium	Medium	High	High	**Low**
Safety Heating effect	Low	Low	Low	Low	Medium	**Low**
Safety Radiation	Yes ionizing	Yes ionizing	Yes ionizing	Yes ionizing	Yes non ionizing	**No**
Example Image						

however, the higher the frequency, the greater the attenuation in the body, making it challenging to obtain high spatial resolution deep within the body. Furthermore, the examiner must manipulate the ultrasound probe to find the cross-section that contains the specific landmarks necessary for diagnosis, making the quality of the examination inevitably facility- and examiner-dependent. It is while overcoming some of these shortcomings that ultrasound imaging technology has developed. The following section provides an overview of medical ultrasound systems, focusing on their history and the role of electronics in this field.

1.2 Overview of Medical Ultrasound Imaging Systems

1.2.1 History of Ultrasound Imaging

Technology that utilizes sound for positioning and imaging has been applied to the medical field after being used in military sonar for detecting submarines, fish detection, and detecting metal flaws. The history of ultrasound imaging for medical applications spans over 80 years, as illustrated in Figure 1.1. First, the history of ultrasound imaging, including its ology, systems, and applications, will be described. Then, the history of the elemental technologies that support the applications will be explained.

Dussik in Austria first attempted medical applications of ultrasound in the 1940s [2]. In the 1950s, ultrasound was further applied to living organs, and in the 1950s, Edler et al. used motion (M)-mode to continuously record the motion of the heart wall and compared the motion of normal and diseased mitral stenotic hearts [3]. M-mode is a method that takes time on the horizontal axis and converts reflection intensity to luminance on the vertical axis. As early as the late 1950s, stereoscopic visualization was used to construct a three-dimensional image from multiple projections [4]. In the late 1950s, Satomura further reported the measurement of cardiac function by the Doppler effect using continuous wave (CW) ultrasound irradiation [5]. This technique has become an indispensable measurement method for blood flow measurements in the field of cardiology today. In the same era, Donald et al. used pulsed ultrasound to obtain brightness (B)-mode images of abdominal masses by positioning the probe in close contact with the abdomen [6]. B-mode is the most basic method of using ultrasound to understand the structure of a living body. Although the images are obtained by compound scanning with the probe in close contact with the body surface and manually moving it, this study is important for establishing B-mode imaging from the body surface, rather than the conventional imaging in a water tank.

In the 1980s, the technology of color flow mapping (CFM) appeared [7]. This function, which displays Doppler signals in color images according to the direction and velocity of blood flow, is crucial for today's routine cardiovascular system examination, particularly of the heart and carotid arteries. In these examinations, color images are used to locate regurgitation in heart valves, and CW Doppler is used to evaluate the degree of regurgitation. A new feature, elastography, appeared in the late 1990s [8]. This technology provides palpation information on tissue shear elasticity using shear waves and is currently used to diagnose liver cirrhosis.

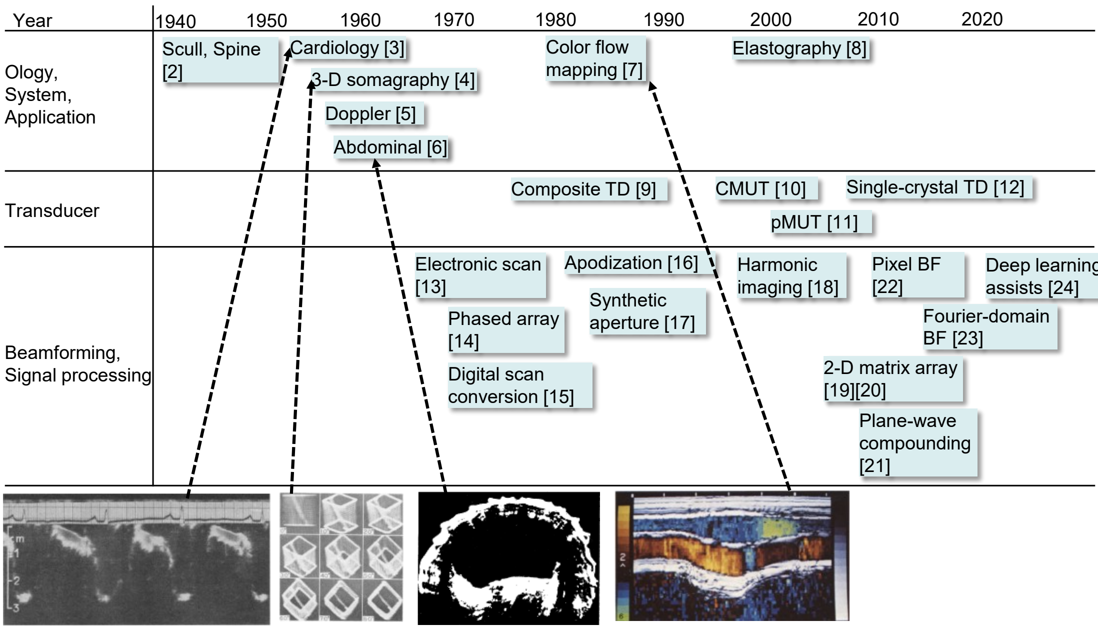


Figure 1.1 History of medical ultrasound diagnosis.

The above is an introduction from an application perspective. The major elemental technologies that support this progress are ultrasound transducer (TD), beamforming (BF), and signal processing. Ultrasound image quality depends on the sensitivity of the ultrasound TD to pick up small sound pressure, the ultrasound beam characteristics that determine spatial resolution in the axial and azimuthal directions, and the signal-to-noise ratio (SNR) and dynamic range (DR) of the signal processing. An overview of the history of these factors is given below.

Ultrasound TDs are elements that provide mutual conversion between electrical and mechanical energy through the piezoelectric and inverse piezoelectric effects. They are responsible for converting electrical signals into acoustic signals during ultrasound transmission (TX) and for converting acoustic signals into electrical signals during ultrasound reception (RX). Ultrasound TD requires acoustic/electric conversion of pulses with a center frequency on the order of MHz. Since short pulses with a wide bandwidth are required for high spatial resolution, composite TDs that combine piezoelectric materials and composite materials, such as polymers, rather than piezoelectric ceramics like the conventional Lead Zirconate Titanate $Pb(Zr, Ti)O_3$ (PZT), have been investigated [9]. In the 1990s, Capacitive Micromachined Ultrasonic Transducers (CMUT) [10] and Piezoelectric Micromachined Ultrasonic Transducers (PMUT) [11], which are silicon TDs utilizing Micro-Electro-Mechanical Systems (MEMS) technology, emerged. The CMUT transmits and receives ultrasound by driving a film formed on a silicon substrate with electrostatic force. Since silicon material has an acoustic impedance close to that of a living body, a matching layer is not required, and short pulses with little ringing can be available. On the other hand, a PMUT is a device that utilizes the piezoelectric effect by forming a film of PZT on a silicon substrate. Unlike CMUT, PMUT does not require high-voltage (HV) bias. Both of these devices have excellent processability using MEMS technology, and when they are processed into multiple elements as an array, they can be processed at a narrow pitch without being restricted by the element pitch due to dicing. Meanwhile, piezoelectric TD can utilize single-crystal elements, such as

$Pb(Mg_{1/3}Nb_{2/3})O_3$-$PbTiO_3$ (PMN-PT), to achieve high sensitivity due to their high piezoelectric effect [12].

Other elemental technologies supporting ultrasound imaging include BF and signal processing technologies for focusing and beam steering, which are closely related to the content of this thesis. To image internal tissues using ultrasound echoes, scanning is necessary. In modern techniques, ultrasound is focused on the desired local area to obtain a better signal intensity. Electronic scanning technology was introduced in the 1960s. Until then, the compounding method was performed by manually moving the probe and combining each signal [6]. However, Buschmann proposed a method of scanning by switching the TX and RX circuits connected to multi-channel TDs using switch circuits [13]. The TDs further evolved into phased arrays, and Sommer used a 1-D array transducer with 21 elements arranged at a pitch of 0.525 mm, along with a delay circuit, to perform a sector scan in which the beam is deflected by applying a delay to each element [14]. In the late 1960s, a digital processing system using computers was proposed [15]. Rather than displaying signals from the TDs directly on an oscilloscope, they were processed by an electronic circuit and displayed as grayscale images of real-space coordinates, contributing to detailed visualization of internal organ structures.

Subsequently, the apodization technique, in which the signal from the TD array is multiplied by a window function to reduce sidelobes and improve beam characteristics, was considered. Harris reported the results of a comparative study on the effects of multiple window functions in 1978 [16]. Synthetic aperture techniques, such as those used in radar, are also applied to integrate and process multiple TX and RX data. Nagai theoretically investigated synthetic aperture by Fourier domain reconstruction using the Fourier transform and demonstrated its computational cost advantage over conventional delay-and-sum (DAS) processing [17]. Tissue Harmonic Imaging (THI) is a technology that utilizes the physical characteristics of ultrasound. The nonlinear propagation of ultrasound generates harmonics. Because harmonic beams are narrower and have lower sidelobe levels than fundamental beams, THI improves spatial resolution and contrast [18]. THI is widely used in today's diagnosis.

2-D array transducers for 3-D imaging have been developed at Duke University since 1986. The conventional 1-D array can scan only in the Azimuth direction, thus only a 2-D cross-section can be imaged. Smith et al. of Duke University have created 2-D array TDs with up to 256 × 256 = 65536 elements [19]. Turnbull et al. studied beam steering and focus control in 2-D arrays, as well as the effects of apodization and element cross-coupling on the beam characteristics of 2-D TD arrays [20]. 2-D array-based ultrasound probes are also referred to as matrix probes. Since the realization of integrated circuits (ICs) for matrix probes with low power dissipation and a small area is a major outcome of this thesis, the technical issues of matrix probes are discussed in detail in Section 1.2.3.

Let us turn back to the 1-D array. Ultrasound imaging is excellent for real-time imaging; however, when scanning with focused ultrasound beams, the frame rate, which is the number of images per unit time, is determined by the round-trip time of the ultrasound and the number of beams that make up the image. A high frame rate can be achieved by transmitting a plane wave without TX focusing and relying on RX focusing, a technique referred to by Montaldo et al. as Coherent Plane-Wave Compounding. This technique utilizes signals from multiple deflected plane waves to compose high-quality images without degrading the high frame rate capability [21]. Pixel BF, which can eliminate blurring artifacts caused by scan conversion by performing the RX BF per pixel instead of per scan line [22]. BF in the frequency domain instead of the time domain, which is referred to as Fourier domain BF, has also been proposed to achieve sub-Nyquist sampling by relaxing the delay resolution constraint required for BF [23]. Finally, the application of deep learning to ultrasound imaging is introduced: as deep learning becomes more practical, its use in adaptive BF and clutter suppression is being investigated [24]. For example, the learning results are reflected in the weighting of apodization, the weighting of matched filter banks in Doppler, and other applications for image super-resolution. The above is an overview of the elemental technologies that support ultrasound diagnostic imaging.

Currently, commercially available ultrasound systems used in hospitals and clinics look like Figure 1.2. A linear probe (b), a convex probe (c), and a sector probe (c) are connected to a cart-type main instrument unit (a), and the probes are placed on the examinee's body surface to acquire in vivo images. The linear probe is suitable for observing areas close to the body surface, such as the carotid artery, at high frequencies that provide high resolution. The convex probe, on the other hand, is suitable for observing deep areas, such as the abdomen, with a wide field of view. Sector probes are used to image the entire heart from a limited and narrow area between the ribs, magnifying it in a fan-like shape through a sector scan [14]. In addition, handheld wireless probes (e), which are battery-powered and display images on a smartphone screen, are commercially available. The elemental technologies described above are used in these products. BF and signal processing can be implemented in either hardware or software; however, for real-time performance, hardware implementation is typically preferred. Until the weak echo signals from the TDs are converted into digital data, it is necessary to rely on analog circuits. The next section provides an overview of the electronic technology required for ultrasound diagnostic systems.

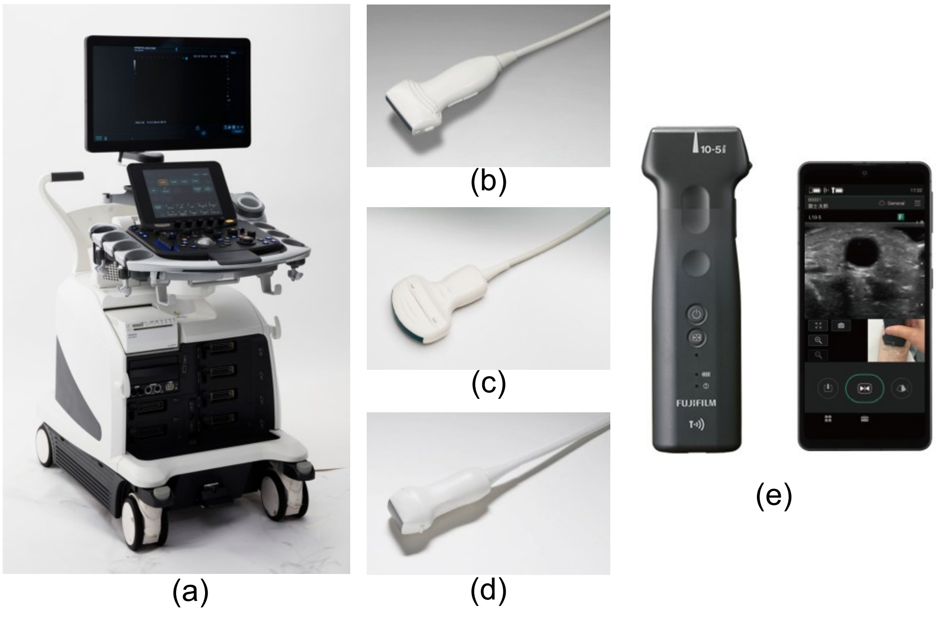


Figure 1.2 Photograph of a commercial ultrasound diagnostic system. (a) cart-type main instrument unit, (b) linear probe, (c) convex probe, (d) sector probe, (e) wireless handheld linear probe. Reproduced from [25], [26]. [27].

1.2.2 Electronics in Ultrasound Imaging

As described in the previous section, the elemental technologies of ultrasound imaging comprise ultrasound TD devices, BF, and signal processing technology, among others. The TX circuit that drives the TD and generates ultrasound waves, the RX circuit that processes the ultrasound received signal, and the back-end hardware that performs beam control are key enablers that support overall signal processing. Figure 1.3 shows a block diagram of a conventional ultrasound imaging system. The ultrasound probe contains an array of 1-D N-channel TD, which are connected to the main instrument unit (Imaging System in Figure 1.3) via N bundled cables. An N-channel analog front-end (AFE) is mounted in the main instrument unit, and the HV driver shown in Figure 1.3 drives the TDs in the probe via the cable with HV pulses, and the acoustic pulses converted by the TDs are transmitted. It then switches to an RX operation, where the echoes received by the TDs are converted to an electrical signal and then amplified by a low noise amplifier (LNA). The same TD is time-shared between TX and RX. For this purpose, a transmit/receive isolation switch (TRSW) is provided to protect the LNA, which is composed of low-voltage (LV) devices, from HV pulses. In other words, during TX, TRSW is turned off to separate the HV driver from the LNA to protect the LNA from HV, and during RX, TRSW is turned on to transfer the small echo signal from the TDs. By increasing the gain over time from the start of RX using time gain control (TGC) in the latter stage, the DR can be secured by compensating for the level difference between the large signal from shallow areas and the small signal from deep areas, due to in vivo attenuation. Since ultrasound images are created by converting the round-trip time from the TD to the biological tissue into a distance, assuming the speed of sound in vivo to be 1540 m/s, such compensation can be achieved by increasing the gain over time [28], [29]. The amplified analog RX signals are converted to digital signals of about 12 to 14 bits by analog-to-digital converters (ADCs) and then beamformed by a digital beamformer (DBF). DBF processing is possible using the central processing unit (CPU) and software, albeit at the expense of sacrificing frame rate. However, since real-time processing is required, it is generally performed using hardware such as field programmable gate arrays (FPGAs) or digital application-specific integrated circuits (ASICs).

As shown in Figure 1.4 (a), by applying an arc-shaped delay to the TX pulse driving each channel of the TD array for each element, a converging wavefront can be created and focused to a single point at an arbitrary depth normal to the TD array. Furthermore, as shown in Figure 1.4(b), the wavefront can be steered with respect to the normal of the TD array to deflect and focus the TX beam on an arbitrary point in space. In RX BF, assuming the reflector is a point source, as shown in (c), the differences caused by path differences to each TD channel from the reflector that received the transmitted ultrasound beam are compensated for by delay, and then the signals are added. In addition, by deflecting the RX beam as shown in (d), the RX signal can be focused on an arbitrary point in space. Since the TX BF and RX BF in Figure 1.3 are implemented digitally, the first-in first-out (FIFO) registers are used to delay the data according to the number of clock cycles. The above is an overview of the electronics in a typical ultrasound imaging system with conventional 1-D probes. In the next section, a system with matrix probes, which is related to this thesis, will be outlined.

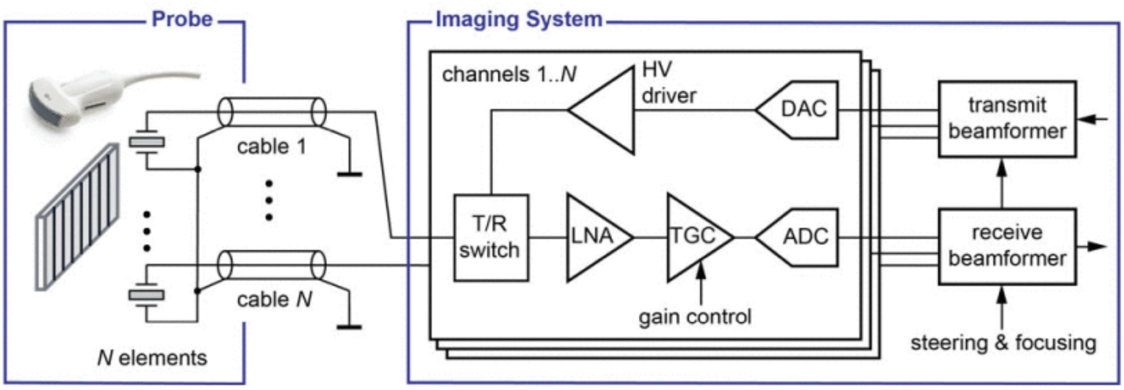


Figure 1.3 Block diagram of a conventional ultrasound imaging system. Reproduced from [28].

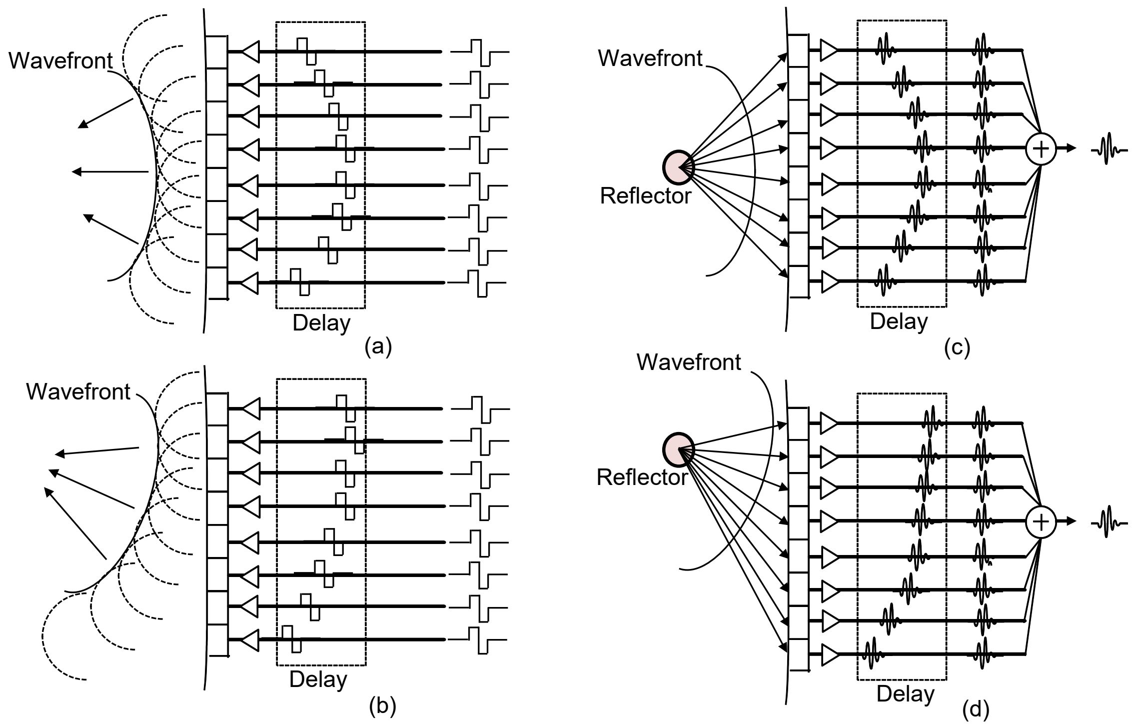


Figure 1.4 Beam steering and focusing:
(a) TX focusing, (b) TX steering and focusing,
(c) RX focusing, (d) RX steering and focusing.

1.2.3 Overview of Matrix Probe and Challenges

Despite widespread use of ultrasound diagnosis, the quality of the images is dependent on the examiner's skill, requiring the examiner to hold the probe in his or her hand and scan to find the cross-section containing the necessary landmarks. Matrix probes differ from conventional 1-D probes in that the TD array is two-dimensional, allowing the examiner to steer and focus the ultrasound beam not only in the azimuth direction, but also in the elevation direction. Figure 1.5 shows a schematic of a 2-D scan with a 1-D probe and a 3-D scan with a matrix probe [19]. A is a sector scan including beam steering, B is a linear scan in which the aperture is moved, and C is a convex scan in which the beam is scanned on an arc with a probe having curvature. D, E, and F are extensions of these to 2-D arrays that also scan in the elevation direction perpendicular to the azimuth direction. With these 3-D scans, for example, it is possible to display a realistic 3-D image of the fetus, like an endoscopic image, during antenatal checkups in obstetrics departments. Real-time 3-D imaging is also known as 4-D imaging. In the field of cardiology, sector scans such as Figure 1.5 D make it possible to obtain multiple arbitrary cross-sections of the heart within the same heartbeat without moving the probe placed between the examinee's ribs. This enables the automatic measurement of left ventricular ejection fraction (EF), an index used to assess the heart's pump function. With the conventional 1-D probe, the examiner must search for two orthogonal optimal cross-sections while moving the probe to measure the left ventricular EF from multiple cross-sectional images obtained between different heartbeats. This represents a significant step forward toward a probe that anyone can easily use.

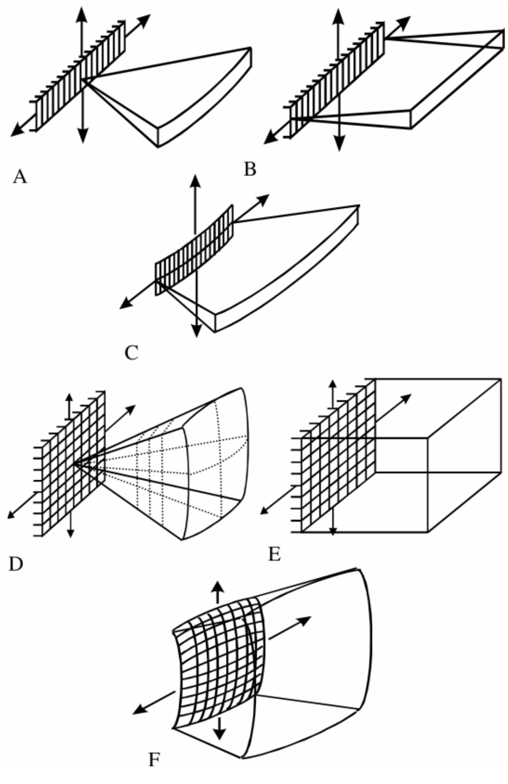


Figure 1.5 Schematic showing traditional 2-D scanning array transducers and their 3-D analogs: A, sectored phased array; B, linear sequential; C, curvilinear array; D, pyramidal scan; E, rectilinear scan and F, curvilinear scan.

Reproduced from [19].

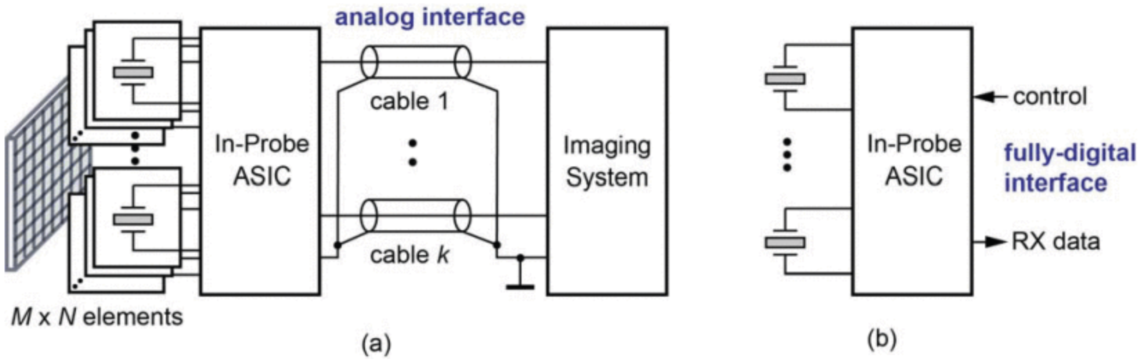


Figure 1.6 Smart ultrasound probe with in-probe ASIC. Reproduced from [28].

The configuration of a system including a matrix probe is shown in Figure 1.6, where the number of TD channels increases to the power of two if the 1-D array is expanded to a 2-D array. It is not practical to connect the probe to the main instrument unit (Imaging System in Figure 1.6 (a)) with several thousand to ten thousand coaxial cables. To reduce the number of cables to approximately 100, a channel reduction in the probe or processing to convert them to digital signals within the probe is necessary. In either case, an in-probe ASIC is necessary. In other words, the in-probe ASIC is a key enabler in the realization of a matrix probe.

The concept of the commercially available matrix probe with the 2-D array TD and ASIC is shown in Figure 1.7. With the 2-D array, the matrix probe can focus and steer the beam not only in the azimuth direction but also in the elevation direction, enabling 3-D and 4-D imaging. This enables the acquisition of arbitrary cross-sectional B-mode images from volume data, even when offline. The ASIC performs BF for both TX and RX. During RX, partial BF is used to reduce the number of channels to the same level as a conventional 1-D probe.

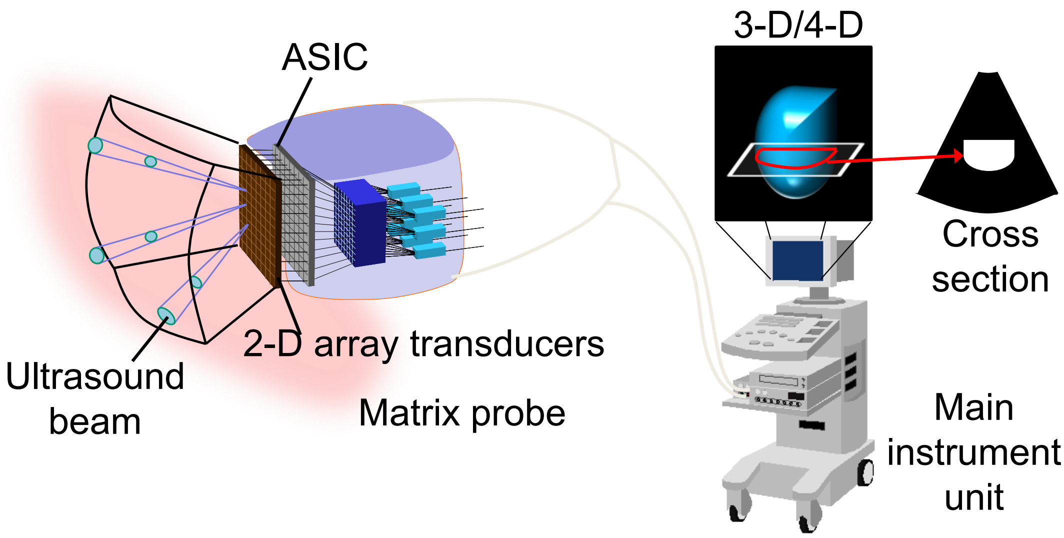


Figure 1.7 Concept of matrix probe.

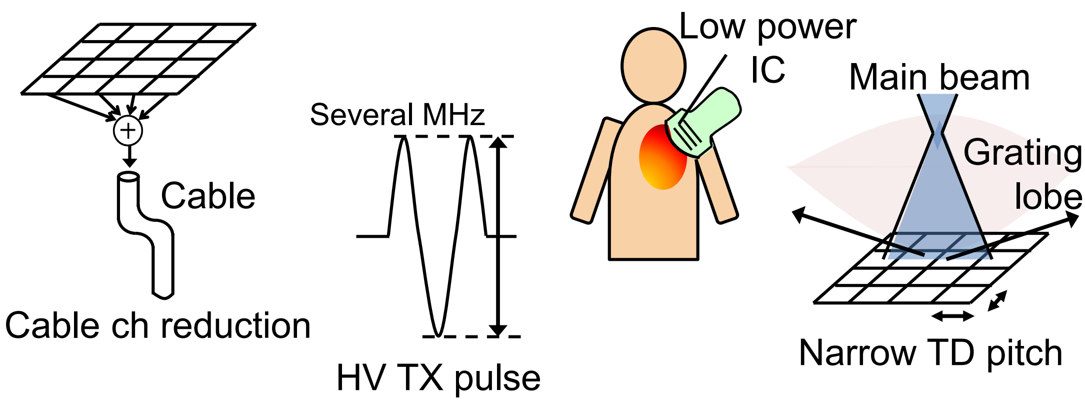


Figure 1.8 Technical issues with in-probe ASIC embedded in matrix probes.

The challenges of an ASIC in a matrix probe are illustrated in Figure 1.8. As mentioned above, it is not practical to connect the probe to the main instrument unit using thousands to 10000 coaxial cables. Therefore, it is necessary to perform channel reduction by RX BF in subarray units. It is also necessary to transmit HV pulses of 60 Vpp or more and several MHz to obtain the required sound pressure, even from deep inside the body. A technology that includes HV-MOSFETs, such as bipolar CMOS DMOS (BCD), should be selected to configure the TX circuit. The probe is a device that is in contact with the examinee, and the in-probe ASIC consumes power, becoming a heating source. Therefore, the ASIC must operate with low power to prevent low-temperature burns of the examinee. According to the IEC 60601-2-37 safety standard for ultrasound medical diagnostic and monitoring equipment, the temperature of the part of the probe in contact with the examinee must not exceed 43 °C. That leads to the constraint that the power of the in-probe ASIC must be kept to approximately 2 W to ensure natural air cooling during a normal examination. In-probe ASICs are mounted 1:1 facing the 2-D TD array. Therefore, the pitch of the TD and the pitch of the ASIC's 1-channel transceiver circuit must be matched. The grating lobe angle and scanning angle constrain the TD pitch. In BF, an undesired grating lobe is formed at an angle determined by the ultrasound frequency and TD pitch due to diffraction, in addition to the main beam. Thus, in in-probe ASICs, the chip area is not only a cost factor but also a performance factor.

1.3 Thesis Motivation

The objective of this research in this thesis is to develop technologies for a small area, low-power in-probe ASIC embedded in matrix probes as described above, as well as the technology necessary to realize a handheld matrix probe, which has not yet been achieved. To shrink the area of the transceiver circuit connected to one channel of TD within the desired 0.3 mm × 0.3 mm area, we investigated the reduction of area and low power dissipation of the analog BF (ABF) circuit and the TRSW circuit embedded in each channel. Furthermore, a new concept of a continuous-time pulse compressor (CTPC) was investigated to achieve both spatial resolution and SNR as a means of further improving the image performance of the ultrasound imaging system. If the effect of CTPC is used not only to improve performance but also to reduce the TX voltage, the circuit area can be reduced and the power dissipation can be lowered. The above reductions in area and power dissipation can contribute to the realization of a battery-operated wireless hand-held matrix probe. Matrix probes are suitable for home healthcare because they reduce the examiner's dependence on manual handling skills and provide ease of use, allowing anyone to use them. Whereas it is difficult to bring a cart-type of equipment into the home. The realization of the matrix wireless hand-held probe has the potential to be a significant support for home healthcare in an aging society, and we believe its social significance is great.

1.4 Thesis Organization

Figure 1.9 and Figure 1.10 show the organization of this thesis. In Chapter 1, we have provided a summary of the research background on ultrasound imaging for medical applications, which is the subject of this thesis, as well as the challenges associated with matrix probes featuring 2-D arrays. Chapter 2 describes the considerations involved in determining the target specifications for ASICs based on system requirements. In Chapter 3, we discuss the issues of small area and low power dissipation of the in-probe ASIC, with a particular focus on the ABF, which consists of analog delayers and an adder. In Chapter 4, we discuss the reduction of the area and power dissipation of the TRSW. Chapter 5 describes a continuous-time pulse compressor, which further improves system image performance and resolves the trade-off between spatial resolution and SNR. In Chapter 6, we describe the diagnostic ultrasound system that can be realized by combining the technologies described in Chapters 3 through 5, and conclude.

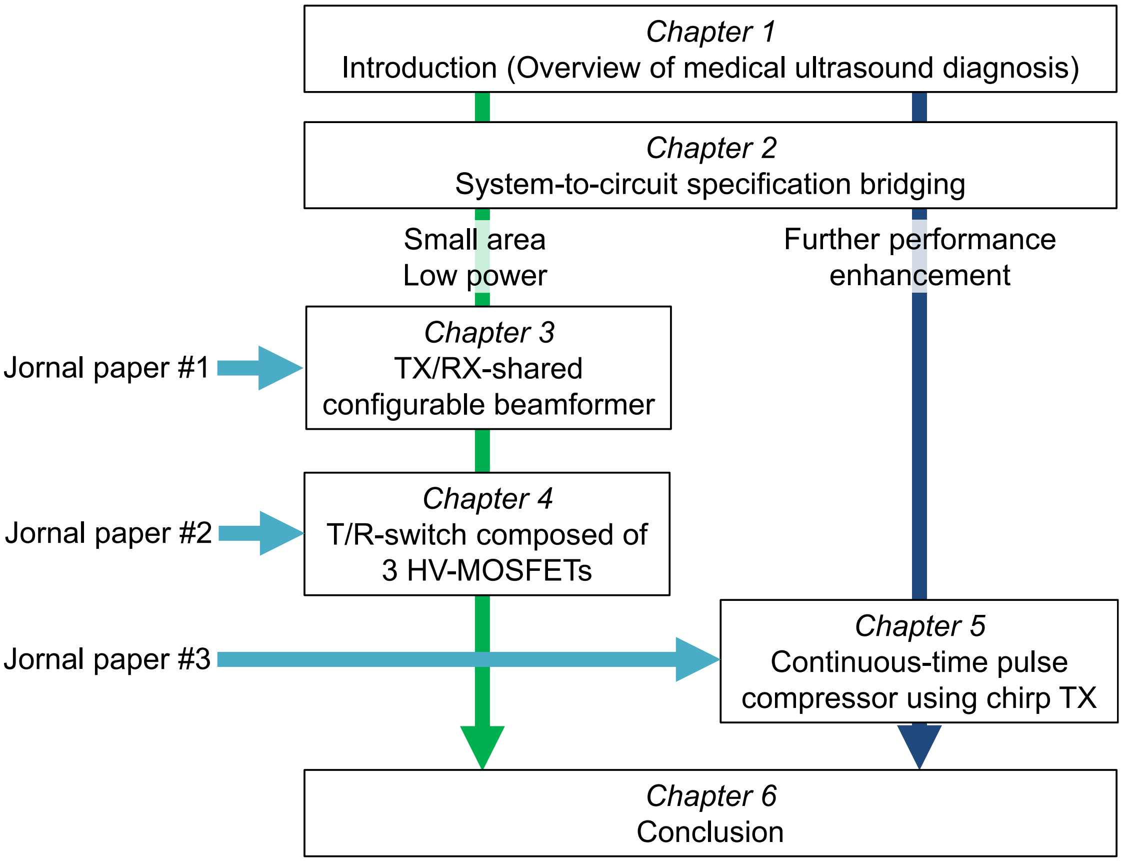


Figure 1.9 Organization of this thesis.

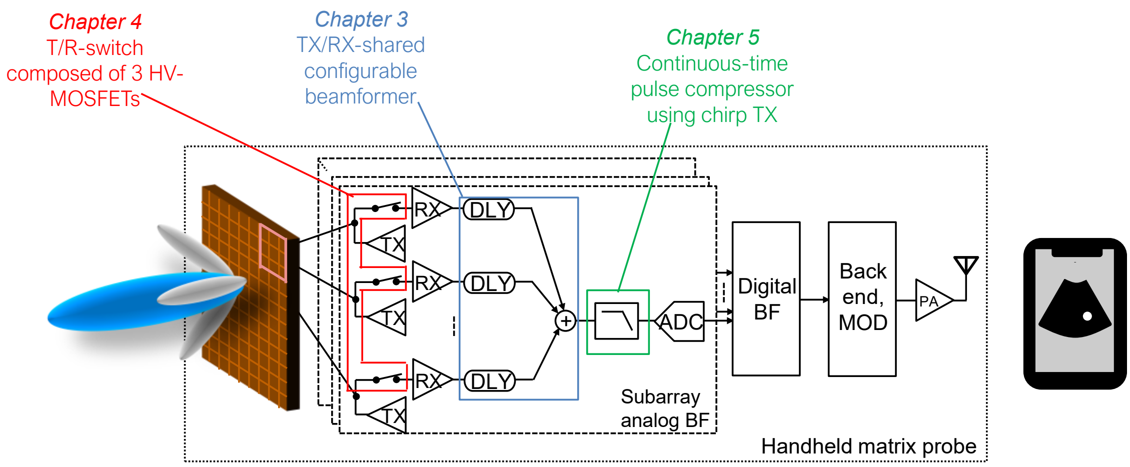


Figure 1.10 Block diagrams showing the organization of this thesis.

Chapter 2
System-to-Circuit Specification Bridging

2.1 Background

This chapter describes the requirements for a 2-D array matrix probe system and the approach for establishing specifications to implement this as a specific circuit. The biological structures targeted by ultrasound imaging diagnostic systems are complex, and there is significant variability due to individual differences in body size. Among diagnostic areas, the cardiovascular (heart) region is particularly challenging due to its complex structure, the need for beam steering via sector scanning, and the requirement for imaging at relatively deep locations of approximately 100 mm. Therefore, this study will focus on this region to examine the system requirements and break them down into circuit specifications. Note that the required TX voltage depends on the voltage-sound pressure conversion characteristics of the TD. The larger the voltage amplitude, the larger the signal. However, this affects the maximum acoustic power that can be irradiated to living bodies and is restricted by safety standards. Focusing, operation mode, and TX apodization [16] are also complex factors that affect maximum acoustic power.

2.2 Transducer Pitch Design

For cardiovascular applications, imaging the heart from the body surface requires placing the probe head between the ribs, where sound is completely reflected, and utilizing sector scanning to view a wide area from a narrow footprint. The pitch of the TD is determined by the condition that unwanted beams, i.e., grating lobes, do not appear within the scanning angle, as described in Section 1.2.3 of Chapter 1, when the ultrasound frequency is given.

First, consider a sector scan that performs beam steering, and establish the geometric model shown in Figure 2.1 for the TX wave. Here, X represents the direction in which the TD array is arranged, and the Y-axis represents the depth direction in which the beam is transmitted. The gray circles represent each TD, which is considered to be a non-directional point source. Let the pitch of the TD be p, and tilt the main beam by θ_m from the Y-axis as shown by the red arrow in Figure 2.1. For simplicity, assume that no focusing is performed and that plane waves are transmitted (this condition is equivalent to infinite far focusing). Let the angle between the grating lobe indicated by the pink arrow and the Y-axis be θ_g. Let the wavelength of the ultrasound wave be λ. As shown in Figure 2.1, the wavefront of the main beam indicated by the red thin line is perpendicular to the main beam direction. Therefore, the spherical waves from each TD are circular arcs tangent to the main beam wavefront. Here, the radius of the spherical wave of the fourth TD element from the left is $3p \sin \theta_m$. Therefore, focusing on the red right triangle, equation (2.1) holds.

$$a\, sin\theta_g = 3p\, sin\theta_m \tag{2.1}$$

Furthermore, based on the similarity of the red hatching right triangle and the blue hatching right triangle, the following is true.

$$\frac{3p + a}{a} = \frac{3\lambda}{3p\, sin\theta_m} \tag{2.2}$$

Eliminating a from the simultaneous equations (2.1) and (2.2) and solving for p yields (2.3).

$$p = \frac{\lambda}{sin\theta_g + sin\theta_m} \tag{2.3}$$

Since the grating lobe angle θ_g of 90 degrees is the most severe condition for pitch, substitute 1 for $sin\ \theta_g$ to obtain (2.4).

$$p \leq \frac{\lambda}{1 + |sin\theta_m|} \tag{2.4}$$

Using (2.4), the angle of view that can be secured at frequencies from 1.5 MHz to 5.0 MHz is calculated as shown in Figure 2.2. Increasing the frequency improves spatial resolution; however, this comes at the cost of increased attenuation. For cardiovascular applications, frequencies of 1.5 MHz to 2.0 MHz are generally used for TX. However, assuming that frequencies up to 3.0 MHz will be used in this case, it can be seen that a TD pitch of 0.3 mm or less is required to achieve a field of view of ±45 degrees at 3.0 MHz. Based on this, the target area for the ASIC channel directly connected to the TD was set to 0.3 mm square.

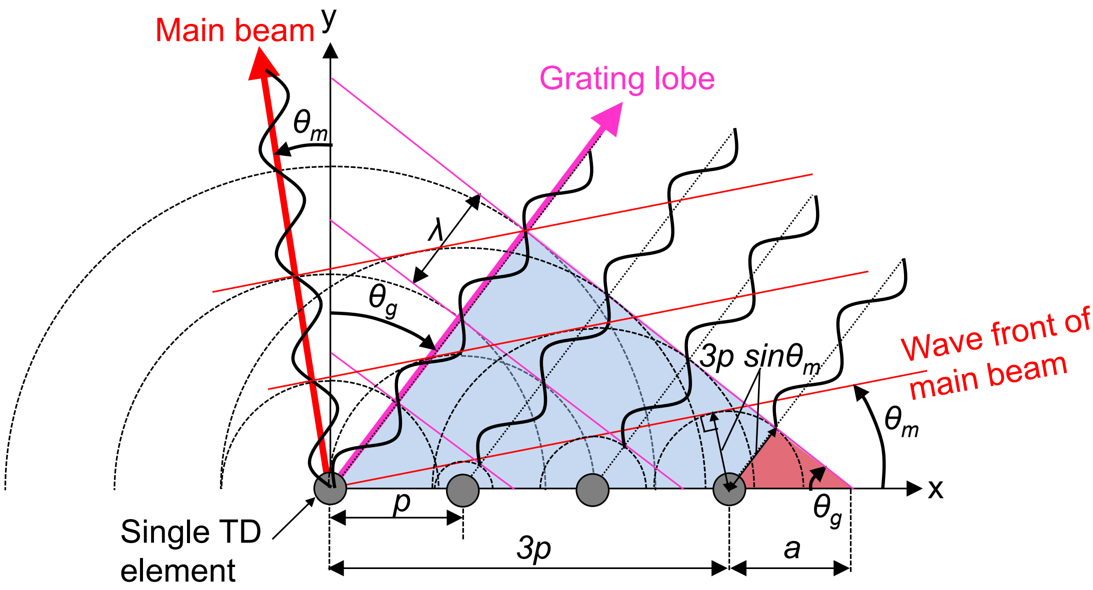


Figure 2.1 Geometry of the main beam and grating lobe in sector scanning.

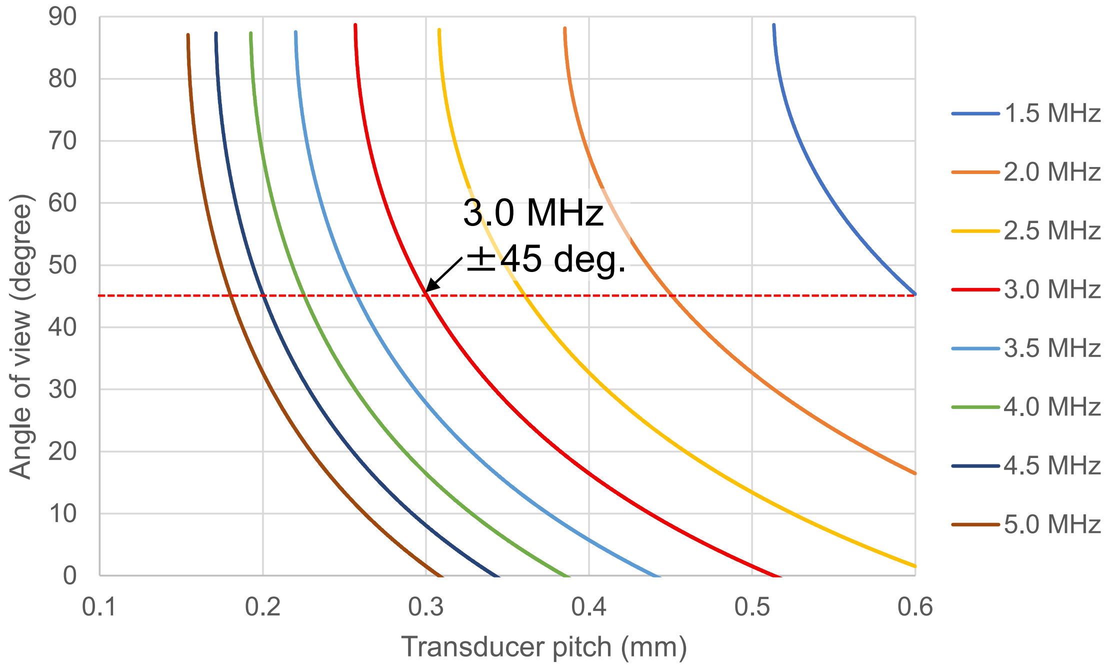


Figure 2.2 TD pitch dependence on angle of view.

2.3 Aperture Area Design

The larger the aperture through which ultrasound waves are transmitted and received, the higher the sound pressure at the focal point can be increased through beamforming. Therefore, in general, a larger aperture is preferable. However, in cardiovascular applications, it is necessary to place the probe head between the ribs and use sector scanning to view the entire heart with a wide field of view from the intercostal space. As a result, the aperture area of the TD array is constrained by the intercostal space. Since the human intercostal space is approximately 19.7 ± 3.7 mm at its widest point [30], a target aperture area of approximately ϕ20 mm should be targeted.

Consider the beam quality at a ϕ20 mm aperture. The relationship between the sound pressure I on the beam center axis, normalized across the entire TD array, and the depth Z, normalized so that the geometric focal depth is 1, is given by equation (2.5) below.

$$I = \frac{2}{1-Z} sin\left\{\frac{\pi D}{2}\left(\frac{1}{Z}-1\right)\right\} \tag{2.5}$$

Here, a is defined as the radius of the aperture, λ is the wavelength of the sound wave, R is the focal depth, and D is defined as follows.

$$D = {a^2}/{\lambda R} \tag{2.6}$$

D is called the D factor, which represents the degree of focusing. For a frequency of 3 MHz, a focal depth R set to half of the maximum diagnostic depth of 100 mm (50 mm), and an intercostal space constraint of $2a$ = 20 mm (i.e., a = 10 mm), the D factor is calculated to be 3.9≈4. Figure 2.3 shows the relationship between sound pressure and normalized depth Z when the D factor is varied from 1 to 5. In the far Fraunhofer zone, the beam diameter widens, and the sound pressure along the beam center axis decreases. As the D factor increases, the focal point approaches the geometric focal point, resulting in higher peak sound pressure and a narrower half-width sound pressure. At D=4, which corresponds to the ϕ20 mm aperture determined by the intercostal space, the maximum sound pressure is obtained in an area relatively close to the geometric focal point, and no significant issues are expected with this aperture. Note that with RX DBF, it is possible to achieve multiple depths of focus from data stored in memory. However, it is not possible to focus on multiple points with a single transmission. For this reason, it is necessary to make the TX aperture smaller than the RX aperture and optimize the D factor of the TX beam separately from that of the RX.

Considering a ϕ20 mm aperture, the single TD is 0.3 mm square based on the calculation results in the previous section, so the number of channels in the 2-D array is as follows.

$$\frac{\pi a^2}{p^2} = \frac{\pi 10^2}{0.3^2} = 3491 \tag{2.7}$$

From this point on, approximately 3000 or more channels will be required.

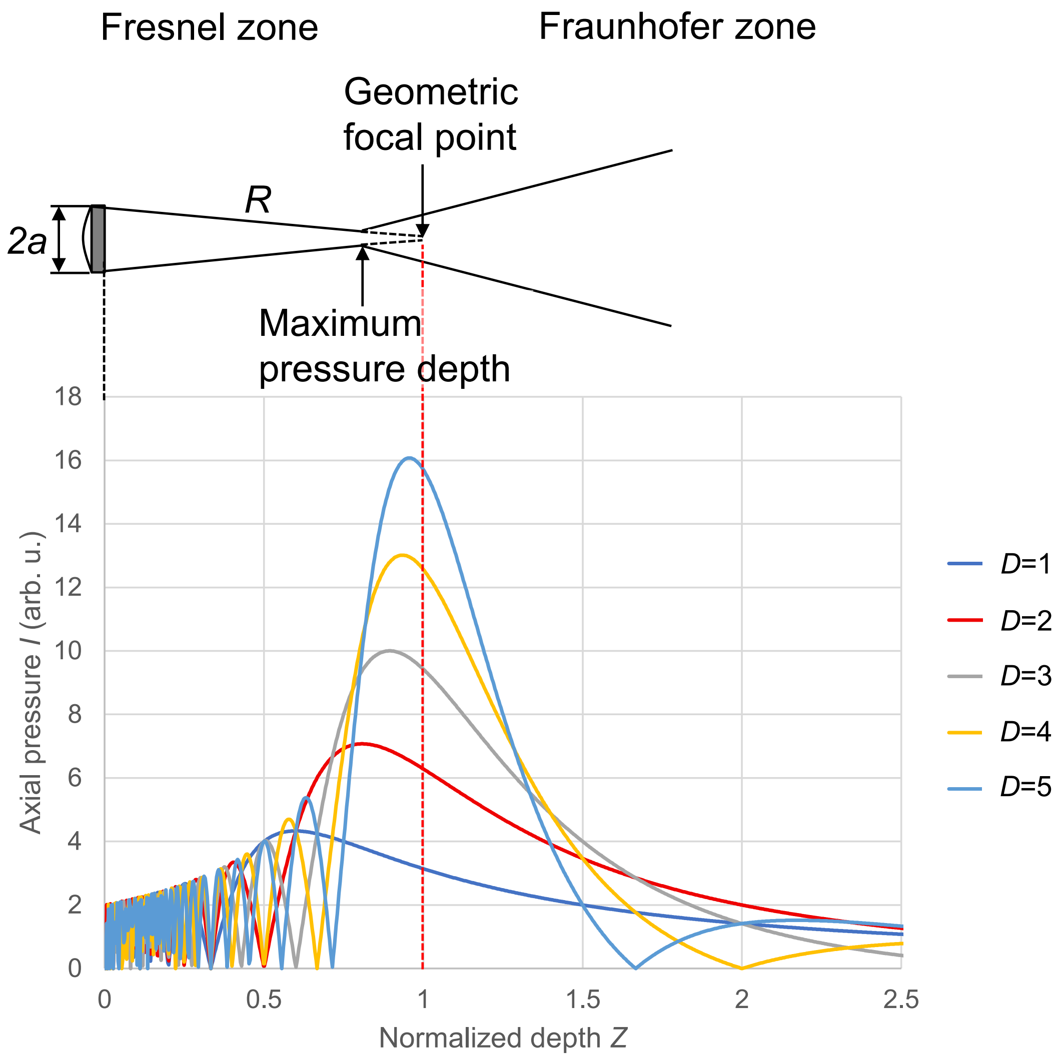


Figure 2.3 Dependence of focus on D factor.

2.4 Design of Delay for Beamforming

In this section, we examine the maximum delay and delay resolution required for BF using the geometry shown in Figure 2.4. In Figure 2.4, the suffix of the TD channel at the origin of the 2-D array is (*0,0*), and the suffix of the TD channel in the *i*-th position in the x direction and the *j*-th position in the y direction is (*i, j*). Let *R* denote the distance from the origin to the focal point. The difference between the distance from the focal point to the TD($0,0$) and the distance from the focal point to the TD(i, j) must be compensated by the beamforming delay. This delay Δtij can be expressed as follows, where c is the sound speed, p is the TD pitch, and θ_0 and ϕ_0 are defined in the polar coordinate system as shown in Figure 2.4 [20].

$$\Delta t_{ij} = \left(R - R_{ij}\right)/c$$

$$= \frac{R}{c}\left\{1 - \sqrt{(\mu_0 - ip/R)^2 + (v_0 - jp/R)^2 + cos^2\theta_0}\right\} \tag{2.8}$$

Here, the direction cosine μ_0 and v_0 are as follows.

$$\mu_0 = sin\theta_0 \cdot cos\phi_0 \tag{2.9}$$

$$v_0 = sin\theta_0 \cdot sin\phi_0 \tag{2.10}$$

The maximum delay required can be calculated from the above equations.

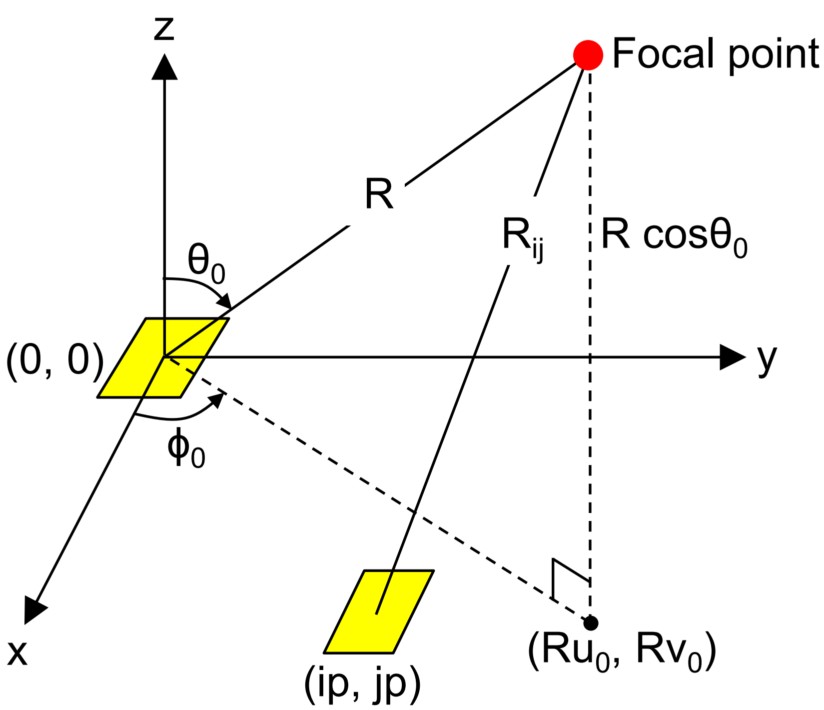


Figure 2.4 Geometry of a 2-D array representing the path difference between the center element and arbitrary elements. Adapted from [20].

In the previous section, it was determined that an array of approximately 3000 channels is required. Considering the reduction of 3000 channels to the channel count of conventional 1-D probes (64–192 channels) within an ASIC, it is practical to reduce the number of channels to 3072 / 24 = 128 channels by using a 24-channel subarray DAS RX BF with a 3072-channel transceiver in the ASIC. The desired delay profile required for TX and RX BF is achieved by combining fine delays, realized by analog circuits within the ASIC, and coarse delays, realized by DBF after signal digitization. This two-stage BF configuration enables the maximum delay of the delay circuit in the ASIC's single-channel transceiver to be mitigated. Two-stage BF will be described in more detail in Section 3.3.1. Specifically, the delay calculation results for a maximum scanning angle of 45 degrees are shown in Figure 2.5 based on equations (2.8), (2.9), and (2.10). For simplicity, the focal depth is assumed to be infinite. A maximum delay of 10.7 μs is required for a ±45-degree beam steering. When this is assigned to coarse delay via DBF and delay in a 4 × 6 = 24-channel subarray, the maximum coarse delay becomes 9.9 μs, and the maximum fine delay becomes 0.78 μs.

Next, let’s consider delay resolution. Continuous delay is ideal for beam characteristics; however, actual delay control is quantized by clock cycles in DBF, as well as by serial configuration of unit delay cells or sampling periods in analog delayer circuits. Quantization affects signal coherence during addition, leading to contrast degradation due to an increase in side lobes and a decrease in lateral resolution.

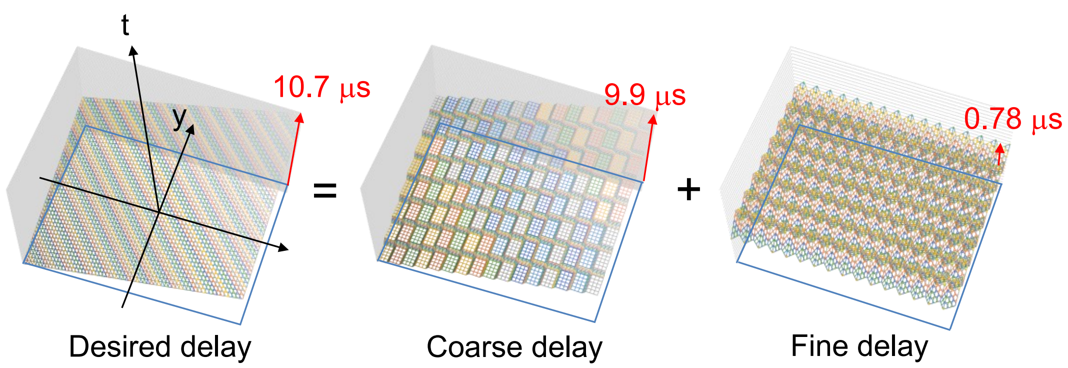


Figure 2.5 Delay profile when the steering angle is 45 degrees.

Figure 2.6 shows the simulation results examined by Bae et al. in reference [31]. They have quantified the impact of delay resolution in an in-phase/quadrature (I/Q) beamformer, which applies time delay and phase rotation to the baseband signal (envelope) obtained through complex demodulation of the RX radio frequency (RF) signal, rather than performing DAS RX BF on the RF signal itself. As the phase delay resolution becomes finer, corresponding to 1/4 (q_{ph}=4) and 1/8 (q_{ph}=8) of the period equivalent to the center frequency, the point spread function (PSF) in Figure 2.6(a) improves, and in the lateral profiles of PSFs (Figure 2.6(b)), the side lobe level decreases. At q_{ph}=64 and 32, the side lobe level decreases to a level close to ideal. Therefore, q_{ph}=32 is desirable; however, considering coverage of the center frequency upto 3 MHz, a delay resolution of 10.4 ns and a sampling rate of 96 MSample/s are required, which raises concerns about power dissipation. The area required for the analog delayer to ensure maximum delay is also a concern. Thus, the practical goal is to perform DAS BF with a delay resolution of approximately 21 ns by setting q_{ph}=16.

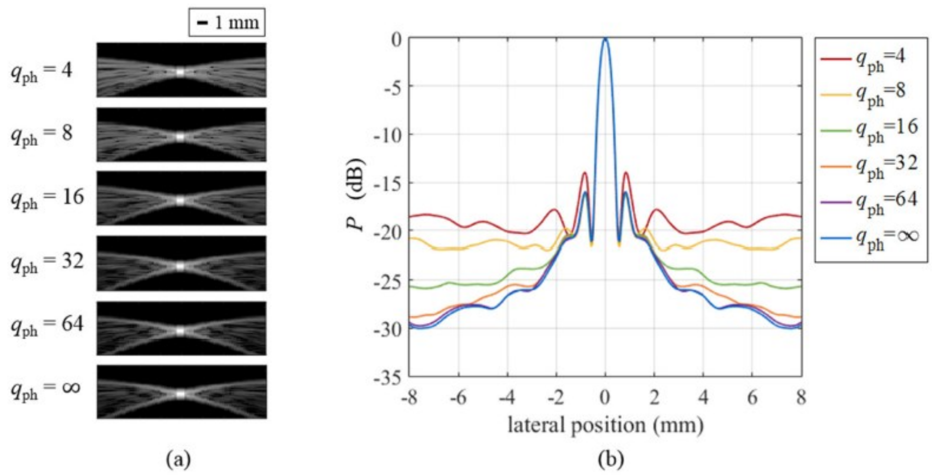


Figure 2.6 (a) Simulated point spread functions (PSFs) of the I/Q beamformer with sampling rate factors of q_{ph} = 4, 8, 16, 32, 64 and ideal (from top to bottom) and (b) cumulative lateral profiles of the PSFs shown in (a). Reproduced from [31].

2.5 Conclusions

At the end of this chapter, the system requirements and target specifications for the ASIC based on the considerations in this chapter are summarized in Table 2.1. Starting in the next chapter, we describe how to implement the ASIC to meet these target specifications.

Table 2.1 System requirements and ASIC target specifications

	System requirements	ASIC specifications
TD pitch = 1-ch transceiver pitch	Angle of view ≥ 45 degrees	0.3 mm
Aperture area	≈Intercostal space: 20 mm	19.2 mm × 14.4 mm
Number of channels	Aperture area / single TD area	3072
Maximum coarse delay	45 degrees beam steering	12.8 μs
Maximum fine delay	45 degrees beam steering, Subarray size: 6 × 4 ch	0.75 μs
Delay resolution	≈Center frequency × 16 sampling	25 ns

Chapter 3
TX/RX Time-Shared Configurable Analog Beamformer

3.1 Background

As described in Chapter 1, image quality in ultrasound imaging is dependent on the examiner's skill and expertise. Echocardiography, in particular, requires a high level of skill due to the need to acquire cross-sectional images that capture specific landmarks of the heart, which is a dynamic, complex, and microscopic structure. The solution to avoid image obscurity caused by the skills and experience of medical technicians is a matrix probe that enables high-speed, high-resolution 3-D/4-D imaging and allows arbitrary cross-sectional images to be obtained after volume imaging. This requires thousands of lead bulk piezoelectric material TDs to be squeezed into a small probe.

In echocardiography, for the required frequency bandwidth of 1-5 MHz, a TD pillar of about 300 μm × 300 μm is required due to the grating lobe constraint described in Chapter 2, Section 2.2. Assuming the maximum footprint of the probe tip is given by the space between the ribs, considering the above 300 μm pitch, approximately 3000 transducers would be desired. Since the number of cables is limited to approximately a hundred due to cable thickness constraints, the probe requires an in-probe ASIC, which must practically include thousands of ultrasound transceivers and a channel reduction function to interface with a main instrument unit. Recently, switch ICs and other ICs have been embedded in 1-D probes as well. Therefore, in this thesis, ASICs embedded in matrix probes will be referred to as 2-D array ICs hereafter. 2-D array ICs perform TX BF and RX DAS BF processing in units of subarrays to reduce the required number of cables.

Several 2-D array ICs have been proposed [32][33][34][35][36][37][38]. The number of transceivers, which equals the number of TD channels, depends on the application. Echocardiography requires a dedicated RX and a TX with HV drivers with BF capability. However, some prior works have no TX-RX BF [34][35][36], no RX BF [32], or no TX [37]. For THI [39], which primarily utilizes second harmonics [40], the second harmonic must be extracted using the pulse inversion method [40], and the HV output signal must be bipolar. In contrast, some conventional 2-D array ICs have unipolar HV drivers. The 2-D array IC must implement the above functions and operate with low power dissipation to maintain heat generation at a level that satisfies the IEC 60601-2-37 safety standard. Specifically, to prevent low-temperature burns, it is necessary to limit the heat generated to a level that satisfies a probe head surface temperature of ≤43 °C while in contact with the examinee. In this chapter, we address the above issues and present a new 2-D array IC architecture, and in particular, discuss a configurable ABF circuit for TX/RX time-sharing. The 2-D array IC is assembled into a matrix probe, which is then connected to a cart-type main instrument unit to evaluate image performance.

3.2 Volumetric Imaging System Architecture

This section describes a study of system architecture that enables real-time 3-D imaging, commonly referred to as 4-D imaging. As a definition of the terminology, the ultrasound transceivers and the TDs connected to each are referred to as element channels (ECh), and each of the coaxial cable channels connecting the probe to the main instrument unit is referred to as a subarray channel (SCh) in the subsequent sections of this thesis. As described below, approximately 3000 ECh are reduced to approximately 100 SCh through subarray BF of the 2-D array IC.

3.2.1 System Architecture

Figure 3.1 illustrates the block diagram of the targeted ultrasound system and the proposed 2-D array IC, which includes 3072-ECh transceivers. The single TD pillar cross-section is 300 μm × 300 μm, designed to have the desired frequency response for echocardiography [41], [42], and each ECh transceiver on the 2-D array IC must have the same pitch for electrically uniform interconnection. The TDs are connected to the 2-D array IC via a low-temperature co-fired ceramic (LTCC) interposer, which mitigates fabrication difficulties associated with the probe head module. On the other side of the pillar, the acoustic impedance matching layer and lens are placed. The 2-D array IC and TDs are electrically connected via wires through the acoustic backing layer and ground sheet. The backing layer absorbs undesired acoustic waves propagating backward from the TDs. It also leads to the placement of the interposer in a thicker area within the probe to accommodate an interposer larger than the lens, which is important for implementing decoupling capacitance near each power supply terminal of the 2-D array IC. In the THI of a transthoracic echocardiography system, ultrasound is transmitted at a frequency of 1.5 to 2.0 MHz [41] and echoes are received at twice that frequency [39], [40]. Therefore, the proposed system uses a signal passband of 1-5 MHz.

The 2-D array IC bidirectionally interfaces a 3072-ECh TD array and a bundle of 128-SCh approximately two-meter-long coaxial cables. The proposed 2-D array IC features a TX DBF, eliminating the need for the main equipment unit to transmit TX signals. 6 × 4 = 24-ECh transceivers are grouped to form a subarray to process RX signals coherently. The main instrument unit digitizes the signals, performs RX DBF, and renders images.

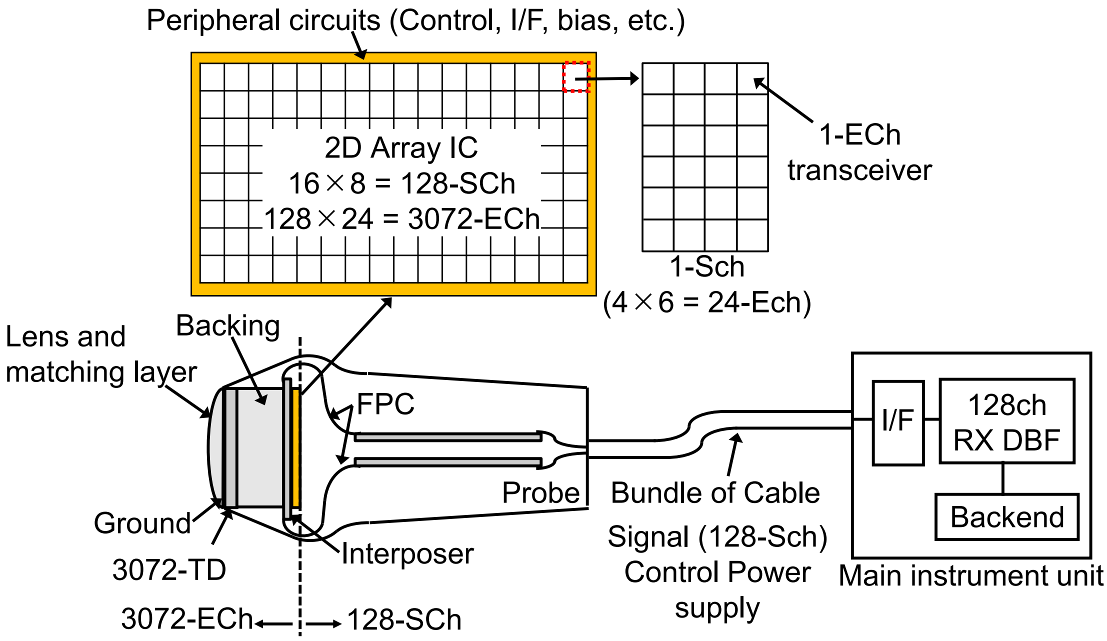


Figure 3.1 Block diagram of the volumetric imaging system with 3072-ECh/128-SCh 2-D array IC.

3.2.2 2-D Array IC Architecture

A block diagram of the proposed 2-D array IC is shown in Figure 3.2. The TX chain is an all-digital architecture, consisting of a TX DBF, a bidirectional dynamic reconfigurable switched-capacitor delayer (BDR-SCD), which will be described in detail in Section 3.3, and a tunable amplitude three-level TX pulser. Therefore, it is free from waveform distortion and timing error due to cable propagation from the main instrument unit to the probe. In general, a pulser is a static-current-free device, and its power dissipation is significantly lower than that of a linear amplifier. However, its constant output amplitude limits image quality. Besides, it is challenging to transition from B-mode, which displays images in grayscale, to CFM mode, which displays color according to blood flow velocity and direction, within an allowable transition period, as the power supply voltage must be changed mode by mode. To address this issue, the TX pulser features a built-in amplitude control function. The TX and RX chains utilize the BDR-

SCD to squeeze the ECh transceiver blocks into a 300 μm × 300 μm ECh area. The BDR-SCD can delay both 2-bit TX digital and RX analog signals utilizing its dynamic reconfigurability.

The TD-side signal I/O (ECh I/O) is connected to a TX/RX isolation switch (TRSW) to protect subsequent RX blocks, which are composed of LV-MOS. While conventional TRSWs utilize Zener diodes for floating gate bias and inherently require significant power, the proposed TRSW consumes only 12.1 μW in RX mode and zero μW in TX mode by employing a dynamic shunt switch topology. The TRSW is described in detail in Chapter 4.

In the RX chain, RX signals amplified by the subsequent LNAs are delayed through the BDR-SCDs and added in the charge-domain adder (CDADD) to bundle 24 signals into one, then the cable buffer (CBUF) drives the cable. The 2-D array IC was designed using 180-nm HV-silicon on insulator (SOI) CMOS technology.

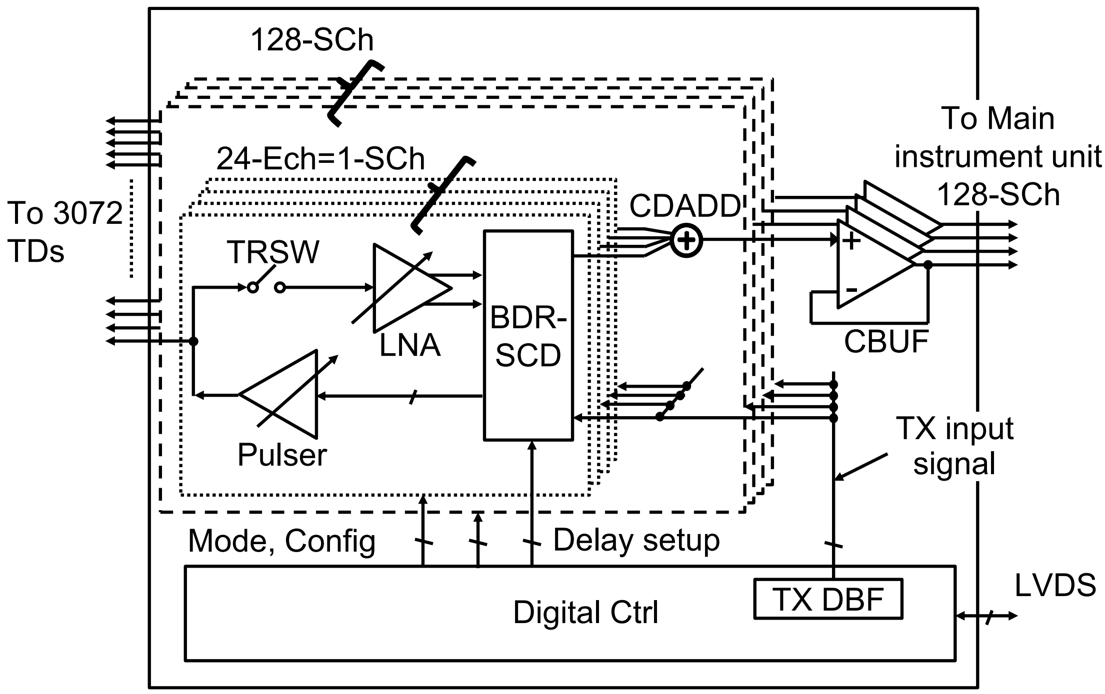


Figure 3.2　Block diagram of 2-D array IC.

3.2.3 RX LNA and Cable Buffer

The blocks dedicated to the RX chain are the LNA and the CBUF. In the RX chain, the next stage following TRSW is a programmable-gain-and-input-impedance LNA, which consists of a common-source differential amplifier and a source follower, as shown in Figure 3.3. The LNA amplifies weak input signals to a suitable level for the next stage, BDR-SCD. Utilizing programmable input and load impedances, a dynamic range (DR) exceeding 85 dB is achieved. The power dissipation of the LNA is 72.7 μW.

The BDR-SCD serves as a delay unit, and the CDADD functions as an adder, forming an RX ABF, as described later in detail in Section 3.3. 24-ECh-to-1-SCh charge domain adder (CDADD) performs correlated signal summation of 24 BDR-SCD outputs in the charge domain. They are distributed in parallel in an SCh; in other words, 1/24 CDADDs are placed within the ECh transceiver area, so there is no signal headroom concern. If the performance of all BDR-SCDs is the same and their correlation is ideal, the SNR of the RX will be $\sqrt{24}$ times higher than that of each BDR-SCD input. This means that the noise level would be $1/\sqrt{24}$ × through ABF.

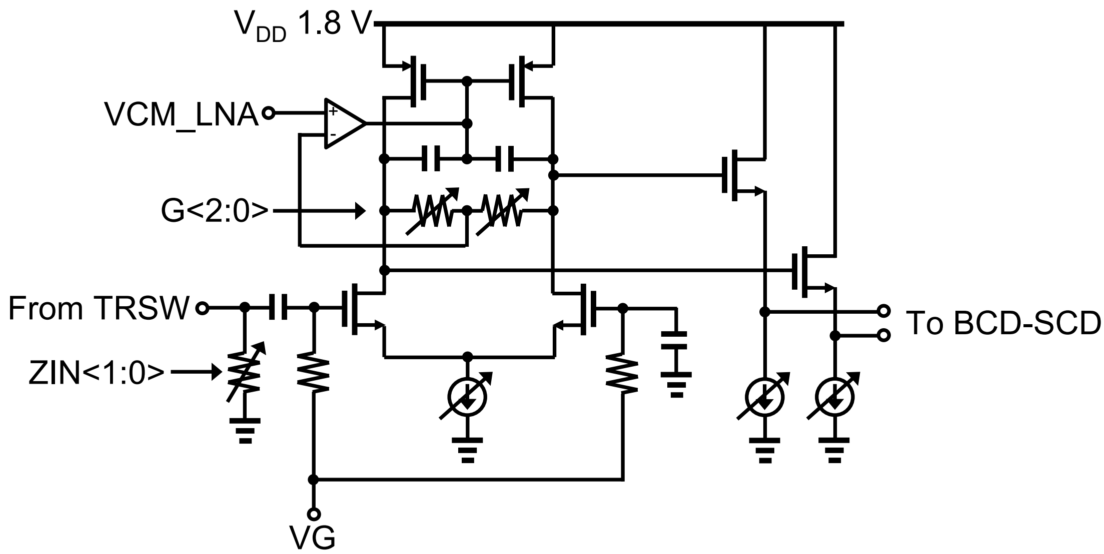


Figure 3.3 Programmable-gain-and-input-impedance LNA.

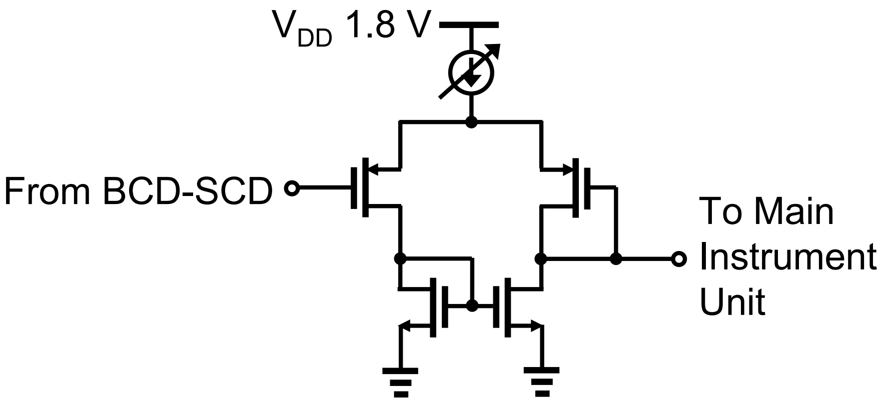


Figure 3.4 Low-noise cable buffer.

Therefore, the next stage, the CBUF shown in Figure 3.4, must have low noise characteristics and the ability to drive heavy coaxial cables, as the cables are very thin, resulting in a capacitance of several hundred pF over just a few meters. The CBUF is a single-stage voltage follower, resulting in being free from instability despite a heavy cable load. The power dissipation of the BUF is 1.35 mW. Finally, in the RX chain, the main instrument unit digitizes the RX signal, performs DBF, and renders the image.

3.2.4 Tunable-Amplitude-and-Slew-Rate Three-Level Pulser

Figure 3.5 shows the conventional and proposed pulser architectures. In the conventional pulser, the amplitude of the output signal is constant and dependent on the HV supply voltage, while the rise and fall times depend on the characteristics of the high-side PMOS and low-side NMOS. The proposed pulser topologically varies the supply voltage within a limited ECh transceiver area and also adjusts the rise and fall times. If the TD drive current passes through the supply voltage regulation circuit, the corresponding MOSFETs will occupy a large area. However, the proposed architecture separates the supply voltage regulation path from the output buffer path. Figure 3.6 illustrates the proposed pulser circuit, which converts a 2-bit digital signal representing three levels into a high-voltage signal, outputting +HV, zero, and -HV level signals. This bipolar signal output function is necessary for achieving high image quality and high resolution in the imaging mode called THI [39], [40], as described above. Ultrasound signals are distorted as they propagate through the body, and RX echoes contain second-harmonic components. The image rendered using the RX second harmonic signal (the fundamental component is filtered out) has higher contrast and resolution than when using fundamental B-mode. The second harmonic component in the TX output signal must be as low as possible in order to capture the second harmonic of biological origin. Therefore, the TX output signal should be symmetrically shaped with positive and negative levels.

The output buffer of the proposed pulser employs a complementary source follower push-pull (PP) topology; the PP consumes dynamic power only during pulse transitions, reducing the bias current of the previous drain output stage and its transistor size. The input of the drain-output pre-driver stage features high-side and low-side HV level shifters with cascode HV-MOS to protect the LV-MOS. The pre-driver output includes a return-to-zero (RZ) switch to achieve a zero level. The RZ is connected to the pre-driver output instead of the PP output to reduce the size of the HV-MOS. By calibrating the rise side and fall side of the slew rate control shown in Figure 3.6 separately, the rise time and fall time can be adjusted, and second harmonic distortion can be suppressed by adjusting the waveform symmetrically up and down.

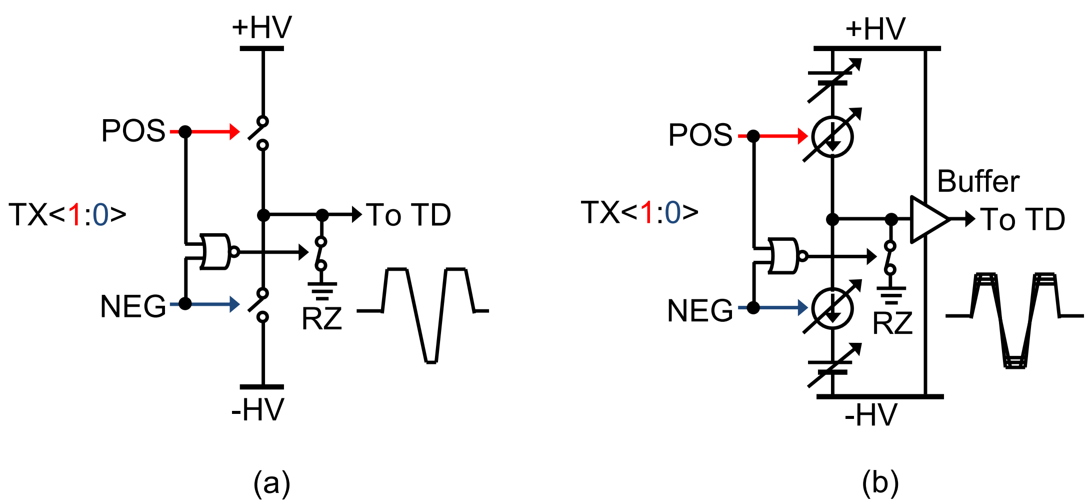


Figure 3.5 (a) Conventional pulser and (b) proposed tunable pulser.

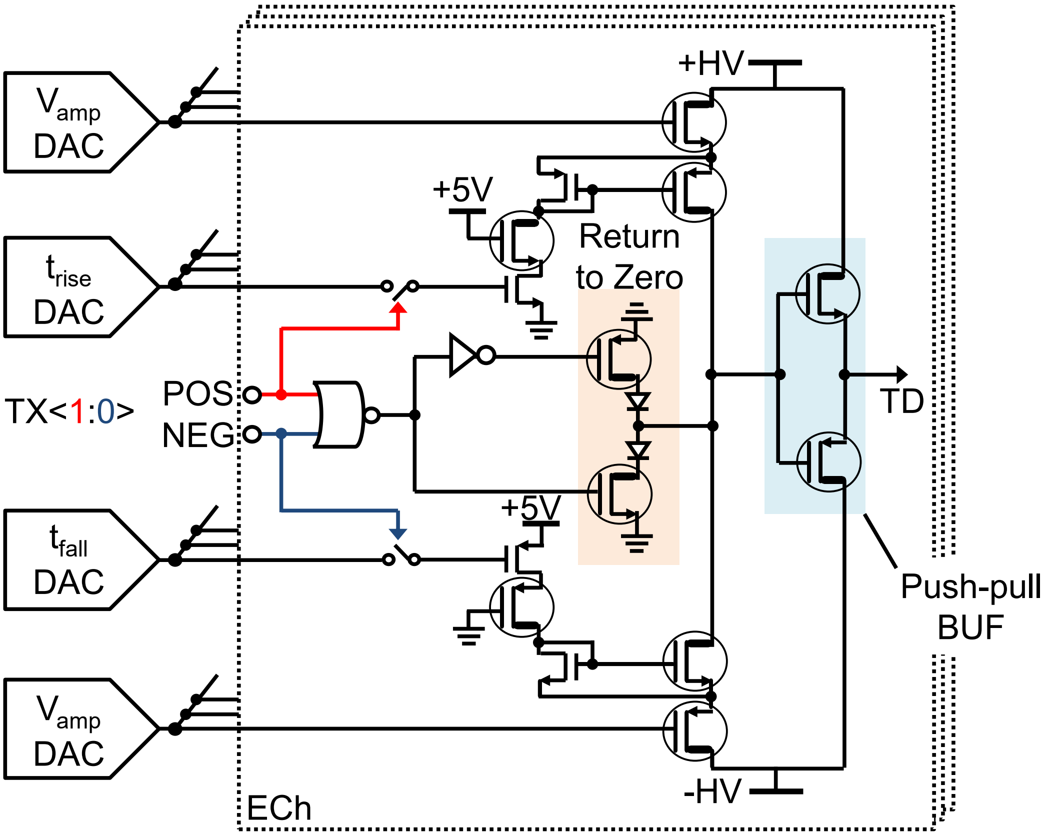


Figure 3.6 Tunable-amplitude-and-slew-rate three-level pulser.

The proposed pulser has a 256-level amplitude adjustment module that competes with linear amplifier systems and supports the fast diagnostic mode transitions required for ultrasound systems. Amplitude transitions settle within 4.4 μs.

3.3 TX/RX Time-Shared Configurable Beamformer

3.3.1 Subarray Microbeamforming

As mentioned above, the 2-D array IC performs channel reduction by DAS BF per unit of SCh, which includes 24-ECh, to interface the 3072-ECh TDs with the 128-SCh main instrument unit. Such partial BF is called microbeamforming (μBF). The main instrument unit and the on-chip TX DBF digitally provide SCh signal chain circuitry with long-time coarse delay (inter-SCh delay). The ECh transceiver on the 2-D array IC performs μBF by adding a short-time fine delay (intra-SCh delay) to coarse delay, causing the TD array to operate as an electrically emulated lens. At full aperture, BF is performed by converting the difference in distance between the focal point and each ECh into time, as described in reference [20], assuming a constant sound speed of 1540 m/s, and adding a compensating delay.

The desired delay profiles required for TX and RX BF are spherical, as shown in Figure 3.7 (a). The delay is divided into the inter-SCh coarse delay (Figure 3.7 (b)) provided by the TX DBF in the ASIC and the RX DBF in the main instrument unit, and the intra-SCh fine delay (Figure 3.7 (c)) provided by the BDR-SCD in the ASIC. The inter-SCh delay is given by the average of the delays required for each ECh within the SCh of interest, as expressed by the following equation.

$$t_d(N_{SCh}) = \frac{1}{24} \sum_{N_{ECh}=0}^{23} t_p\,(N_{SCh}, N_{ECh}) \tag{3.1}$$

where $N_{(ECh)}$ (=0, 1, ... , 23) is the ECh transceiver index on an SCh, and $N_{(SCh)}$ (=0, 1, ... , 127) is the SCh index. The azimuth direction is defined as x (row), and the elevation direction is defined as y (column) in Figure 3.7.

The intra-SCh delay, which is obtained by subtracting the inter-SCh delay from the desired delay, should be assigned to each ECh. This combination of coarse and fine delays for BF, i.e., the combination of system BF and μBF, reduces the required maximum delay of the ABF circuit in each ECh in the 2-D array IC, contributing to a smaller circuit area and lower power dissipation.

3.3.2 Reconfigurable Switched-Capacitor Delayer

This section describes a novel small-area, low-power ABF circuit. RX μBF requires delayers and an adder for DAS BF for channel reduction in analog form. While the TX pulser requires digital delayers to delay the logic signals for TX BF. Conventional architectures require both dedicated digital TX delay chains and an analog RX delayers as shown in Figure 3.8. The TX chain generally requires a first-in-first-out (FIFO) digital shift register for TX BF. A three-level pulsar requires a 2-bit digital signal. The RX path requires an analog signal delayer. As a result, it is challenging to place both the TX and RX delayers within the limited ECh transceiver area; therefore, the proposed architecture shares a delay unit between the RX and TX, as shown at the bottom of Figure 3.8, to reduce the required resources.

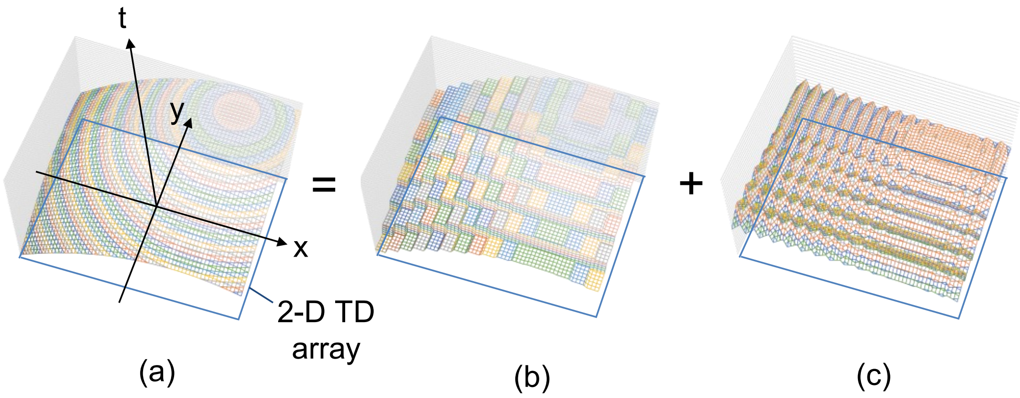


Figure 3.7 Example of division into coarse inter-SCh delay and fine intra-SCh delay: (a) desired spherical delay, (b) inter-SCh coarse delay for DBF, (c) intra-SCh fine delay for μBF.

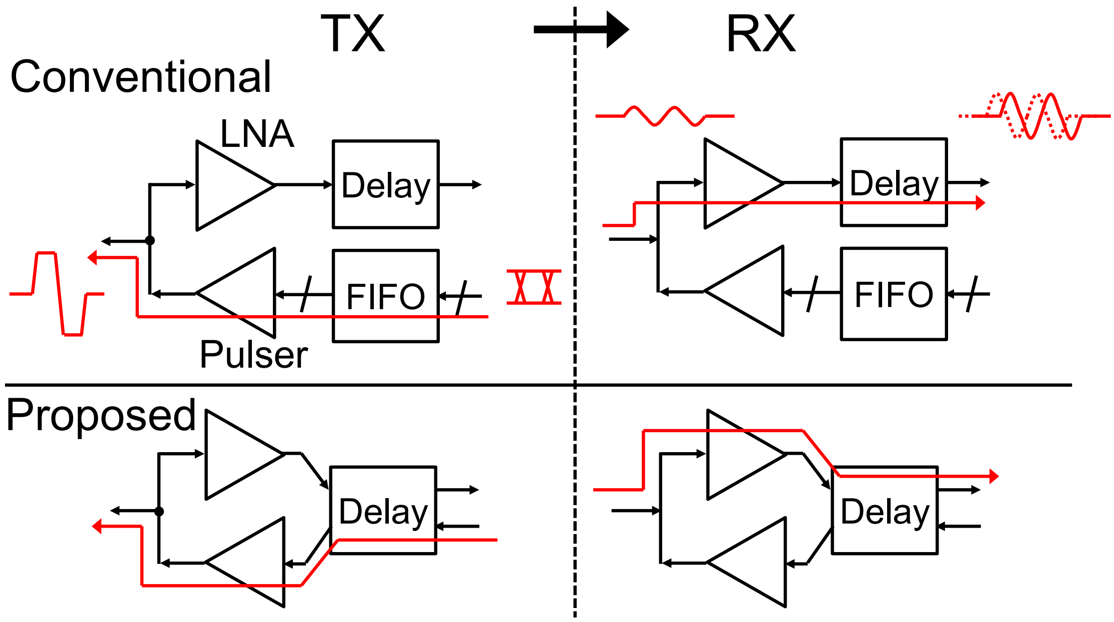


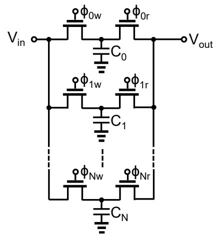
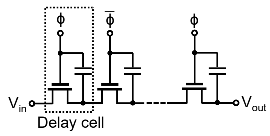
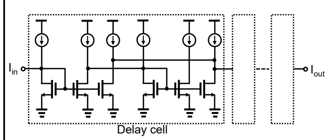
Figure 3.8 Time-sharing of the delayer for TX and RX.

First, we compare and examine the architectures of delay circuits that handle analog signals. Table 3.1 shows the topologies of possible candidates. The first candidate is a capacitor ring memory, in which the input analog voltage V_{in} is sampled sequentially into each capacitor, and the voltages held in the capacitors are read out sequentially to the V_{out} port. Specifically, analog voltages are written to capacitors C_0, C_1, …, C_N in sequence, synchronized with the clock cycle, and then read out sequentially after the desired delay. After writing to C_N, the operation cycles back to C_0. The delay resolution is determined by the clock period, and the number of capacitors used limits the maximum delay. Since this circuit operates passively, it is advantageous for low power dissipation. However, there is a concern of low-harmonic spurs due to mismatches between capacitors. When N capacitors are circulated, low-frequency spurs of clock frequency/N appear in the bandwidth; however, it is possible to take countermeasures at the system level.

Next, the second candidate is a bucket-brigade device (BBD) [43]. This classic circuit configuration enables delay by transferring charge sequentially to subsequent stages in a manner similar to a bucket brigade, synchronized with a clock. The delay resolution is determined by the clock period, and the maximum delay is limited by the number of stages provided. Like capacitor ring memory, it operates passively and has the advantage of low power dissipation; however, it has the drawback that errors accumulate as charge is transferred through multiple stages.

Finally, the third candidate is a cascaded all-pass filter (APF) [44]. By preparing multiple stages of delay cells with constant group delay, the desired delay can be achieved. The topology shown in Table 3.1 is based on current cells, which makes it easy to obtain the desired transfer function through current addition and subtraction. This architecture is suitable for wideband applications since it can easily provide short delays without a high-frequency clock; however, there is a concern that power dissipation may increase due to static current.

Table 3.1 Comparison of analog delayer architectures

Architecture	Capacitor ring memory (Proposed)	Bucket-brigade device (BBD)	All-pass filter (APF)
Schematic			
Operating principle	Analog ring memory (Interleaved sample/hold)	Cascaded charge-transfer delay cell	Cascaded constant-group-delay cell
Pros	Passive operation	Passive operation	Broadband (>30 MHz)
Cons	Low harmonic spurs at ring period (removable at the system level)	Accumulated error with each stage	Static power PVT sensitive

Based on the above comparison of architectures, we decided to employ a switched capacitor delayer (SCD) based on the capacitor ring memory shown in Table 3.1. The SCD with output buffer, proposed in this study for delaying the RX analog signal, is illustrated in Figure 3.9. This circuit consists of an interleaved sample-and-hold (S/H) using capacitor ring memory (CRM). An output buffer with a flip-around, closed-loop operational amplifier (OPA) is added to drive the next-stage CDADD, providing a low-impedance output. The input differential voltage from the LNA is written to each of the capacitors that make up the CRM in turn and held as stored charges. The "Write to Cap" in the upper right corner of Figure 3.9 is the equivalent circuit for writing analog voltages to the capacitors. The analog voltage held in the capacitor is then read out by the equivalent circuit shown in Figure 3.9, "Read from Cap" (bottom right). The inverting input of the operational amplifier is virtually shorted to the signal common voltage (VCM), eliminating the effect of the input capacitance of the OPA.

The control signal for the SCD consists of one-hot cyclic write and read signals. As shown in Figure 3.10, the one-hot write signals are cycled to store voltage to each capacitance in turn. Meanwhile, a one-hot read signal is also cycled to read out the voltage from each capacitance in turn. Focusing on one capacitance in the CRM, for example, if we examine the suffix 0, the time from writing to capacitance #0 to reading from capacitance #0 provides the delay for μBF. Thus, with this circuit configuration, it is possible to realize a delayer that operates with a delay resolution of a single clock cycle.

The clock period determines delay resolution, and the number of capacitors in the CRM determines the maximum delay. Note that it is prohibited to perform Write and Read in the same cycle. In practice, the maximum delay difference between EChs is (N-2)× clock cycles when N capacitors are provided, because the delay needs to be shortened by one cycle during RX operation due to dynamic focus, as described later. In addition, each of the write and read signals must have non-overlapping intervals, so that the capacitors being written or read do not share the charge with the adjacent capacitor.

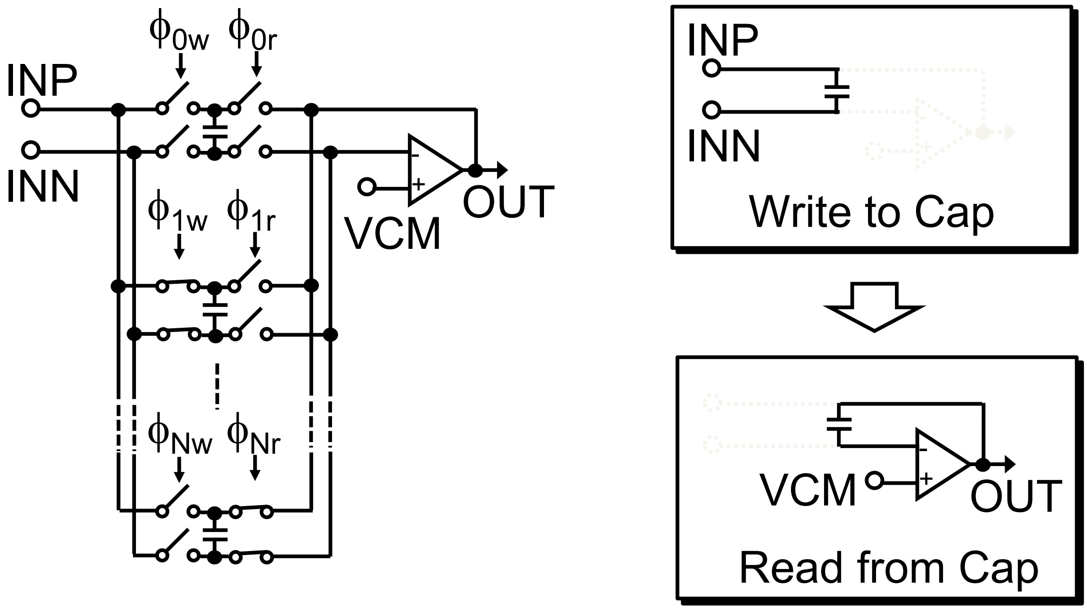


Figure 3.9 Proposed switched-capacitor delayer employing capacitor ring memory and flip-around buffer.

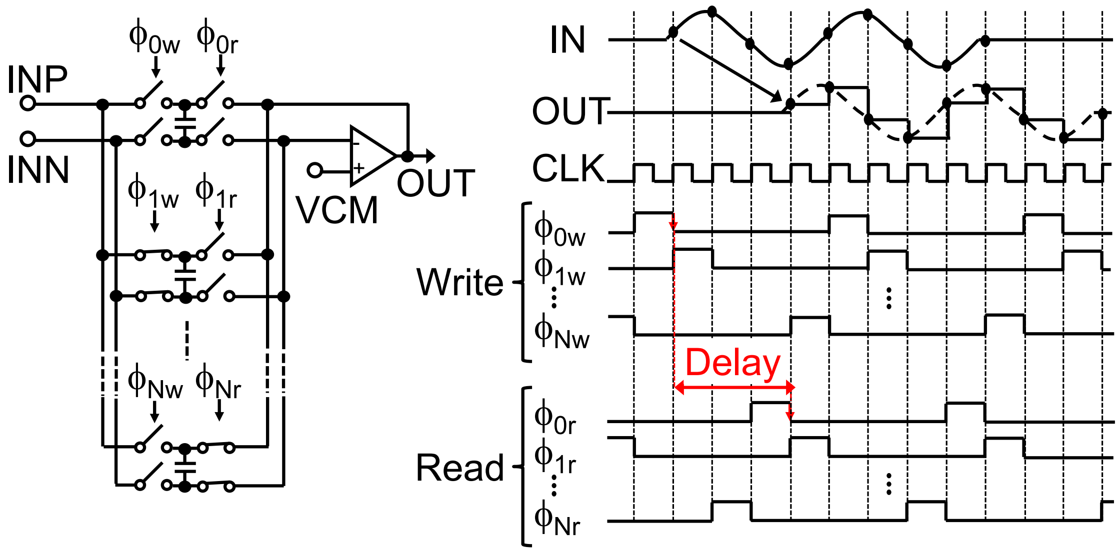


Figure 3.10 Operation principle of the proposed switched-capacitor delayer.

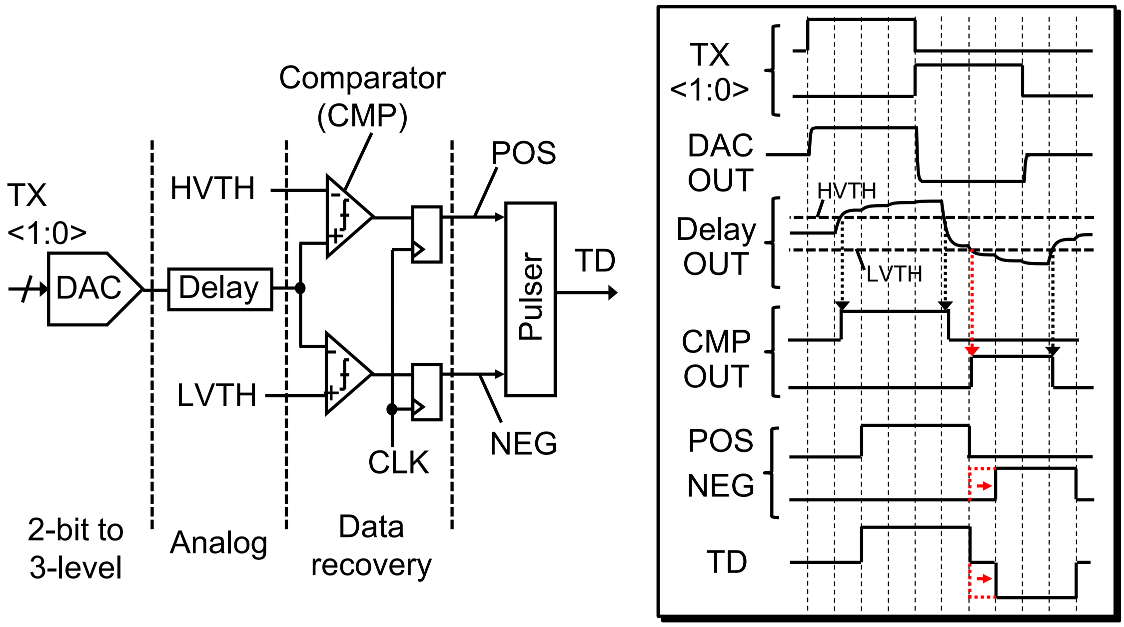


Figure 3.11 Pulse width fluctuation problem in 2-bit recovery from three-level square waves.

Here, we will discuss the issues involved in cases where the SCD is shared for both TX and RX. If a SCD circuit is to be applied to a three-level pulser, the first possible configuration is the three-level waveform transfer and data recovery scheme shown in Figure 3.11. In this architecture, a digital-to-analog converter (DAC) generates a three-level square wave from a 2-bit input. When the three-level square wave passes through an SCD, the slew rate is degraded due to the SCD's bandwidth, resulting in a waveform with a slow slew rate. When this SCD output waveform is recovered to 2 bits by comparing it with the threshold voltage on the high side and the threshold voltage on the low side, the pulse width deviates from the desired width due to the SCD's limited bandwidth. Thus, the TX waveform differs from the original pulse. In other words, it is difficult to correctly recover 2-bit data with a practical SCD bandwidth for such a transfer of three-level waveforms. Therefore, this research proposes an architecture that does not transfer a three-level waveform, but instead recovers it differentially with a binary waveform, 0 or 1.

First, to confirm the validity of the approach, we estimate the area impact of preparing another SCD for 2-bit bus to accommodate the delay operation in TX. Specifically, by mapping which option—adding a new 2-bit TX dedicated FIFO or adding another SCD—results in a smaller area, taking into account the standard cell size of D-flip flop (D-FF) and capacitance density, we can quantify the benefits of adding SCD in a design space. The FIFO configuration is assumed to consist of D-FFs and multiplexers. The SCD capacitance is determined based on the kT/C thermal noise. Since the area of the designed capacitor depends on the capacitance density, this is taken as the horizontal axis, and the calculation results with the area ratio of SCD and FIFO taken as the vertical axis are plotted in Figure 3.12. If adding one additional SCD is more area-efficient than adding a 2-bit FIFO, the ratio on the vertical axis will be less than 1. Even with the same 180-nm technology, the standard cell area and capacitance density vary depending on the foundry, and D-FF functions also vary, such as asynchronous-reset-enabled or scan-compatible. Therefore, in this estimation, the capacitance density was varied in the range up to 8 fF/μm^2 and the cell size of a single D-FF was varied in the range of 30 μm^2 to 100 μm^2. As shown in Figure 3.12, in areas where the D-FF cell size is large and the capacitance density is high, adding an SCD is more advantageous than adding a TX-dedicated FIFO. Note that this estimate assumes that another set of SCDs for RX is prepared to make a 2-bit bus. However, it is also possible to implement the additional SCD only for TX with smaller capacitors by considering a binary operation. Based on this estimation, an implementation was employed that delays the 2-bit waveform data for the TX 3-level pulser by preparing an additional SCD.

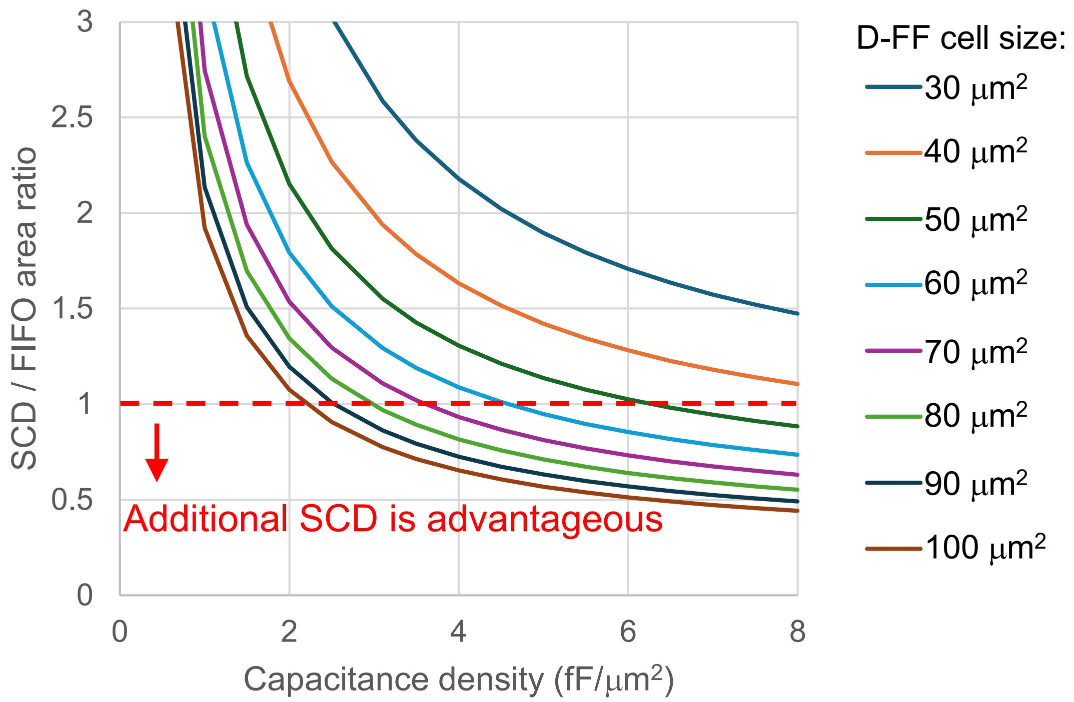


Figure 3.12 Area advantage of preparing additional SCD over additional FIFO considering D-FF cell area and capacitance density.

Figures 3.13 and 3.14 illustrate SCDs consisting of two CRMs, two OPAs. Figure 3.14 also includes a CDADD, described in the next section. The CRM provides the signal delay function. In the RX operation, the capacitor is used as a memory for analog signals, while in the TX chain it is used as a pseudo D-latch, i.e., a memory for digital signals. Generating a logic inversion of the TX digital signal enables the transfer of logic True and Bar differential signals. During TX operation, the OPA acts as a comparator, followed by a clock-edge-triggered digital D-FF. The comparators and the 2-bit digital D-FF recover the 2-bit pulse waveform, ensuring that the pulser output waveform is accurately controlled by clock timing.

The maximum delay time of 25 ns × 30 = 750 ns is achieved by providing 32 CRM capacitances. All the parasitic capacitances of the metal wiring in $\phi_w[31:0]$ and $\phi_r[31:0]$ are almost identical to avoid signal distortions.

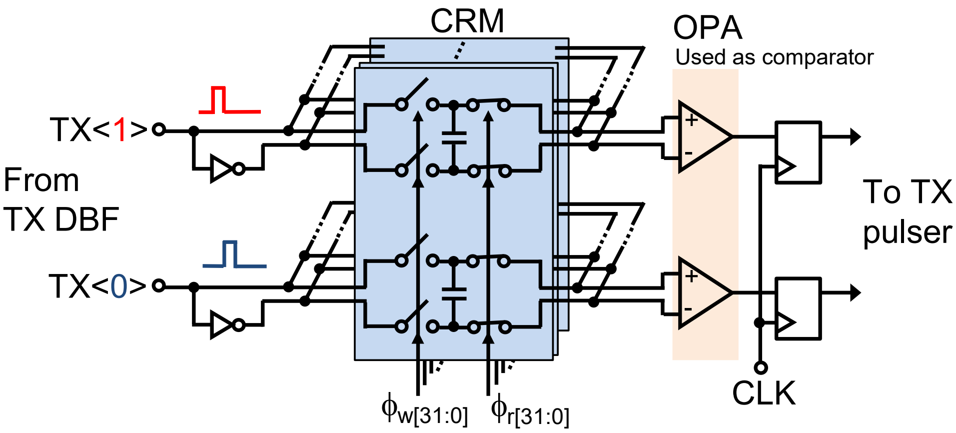


Figure 3.13 TX configuration of BDR-SCD.

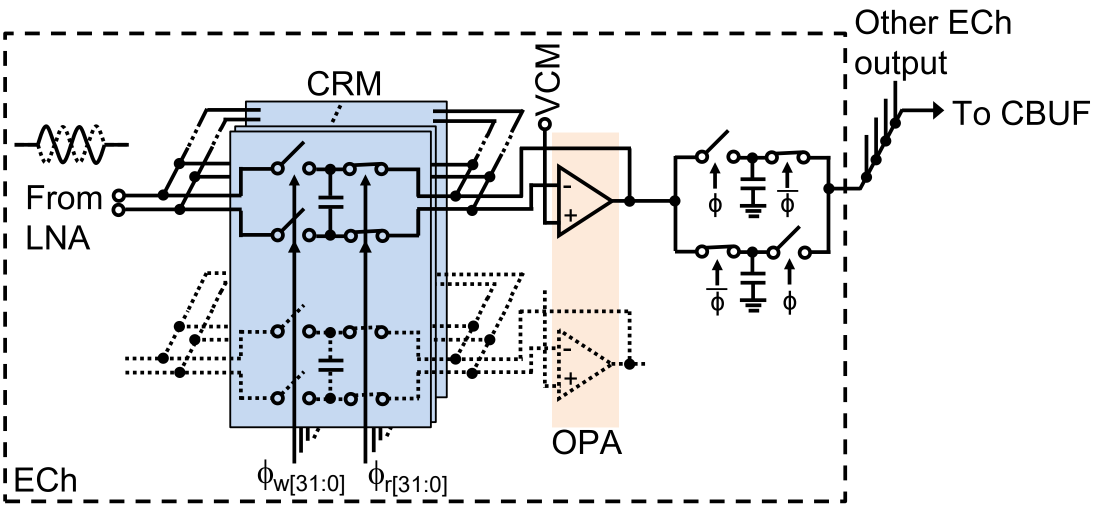


Figure 3.14 RX configuration of BDR-SCD and CDADD.

Here, the TX operation, as shown in Figure 3.13, and RX, as shown in Figure 3.14, are described in detail. Since the three-level TX pulser requires a 2-bit digital input bus, the signal path can be switched by an analog multiplexer (AMUX), as shown in Figure 3.15. Two SCDs are used to support the 2-bit bus. We propose a 2-bit bus, binary True and Bar differential comparison and recovery scheme as shown in Figure 3.16. First, from the input 2-bit waveform data, the SCD creates True and Bar signals through logic inversion, allowing them to be treated as differential signals. Two SCDs delay these differential signals as a 2-bit bus. At this time, the OPAs operate as comparators, comparing True and Bar to recover the 2-bit digital data. It is then captured by the FF to synchronize the timing and sent to the pulser to transmit a three-level high HV pulse.

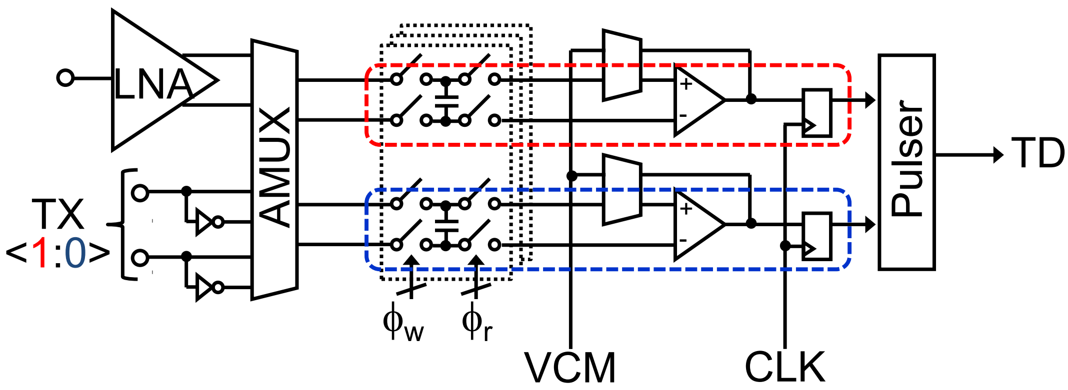


Figure 3.15 TX configuration of proposed SCD.

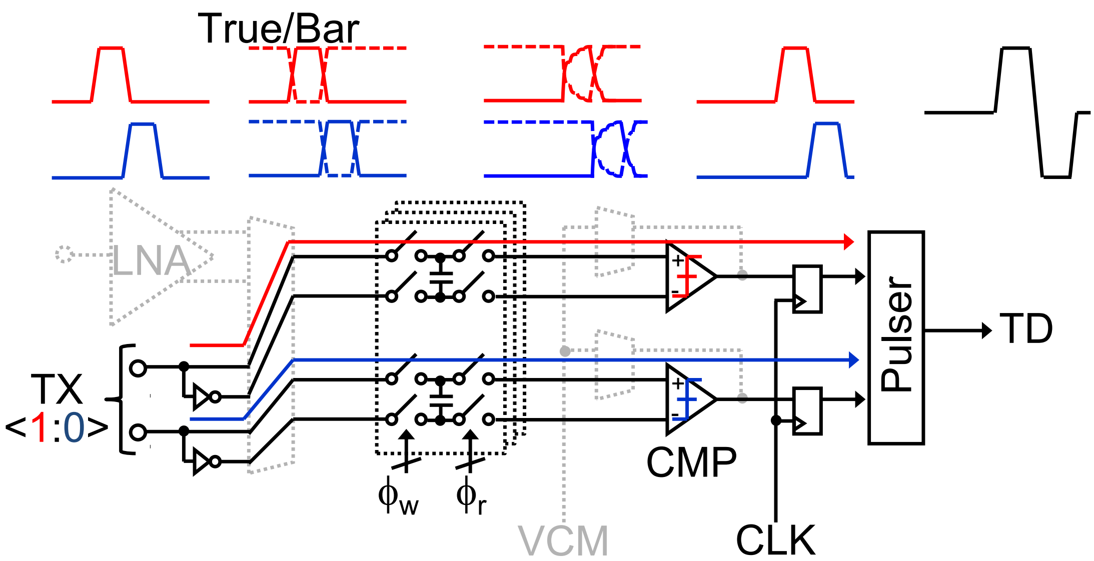


Figure 3.16 TX operation of proposed SCD.

In RX, one of the two SCDs is used for low-power operation. During RX, as explained before, the OPA operates as a closed-loop flip-around buffer. In other words, the same OPA is used as a closed-loop buffer during RX and as an open-loop comparator during TX to further reduce area. Following the OPA, a passive charge-domain adder is used to sum the 24-channel delayed signals. Since the summing operation is performed by redistributing the charge in passive operation, low-power dissipation can be achieved.

The RX dynamic focus operation is described at the end of this section. In RX DBF, performed in the main instrument unit, signals are stored as digital data, enabling BF with various focus depths, even offline. Whereas, in ABF, the original signals for each ECh are lost as soon as they are summed, and only the result of the summation remains. Therefore, it is essential to change the focus depth during the RX period dynamically. Figure 3.18 illustrates an example of a timing chart for fixed focus and dynamic focus operations. Since write-to-readout gives a delay time, duplicating the write pulse or doubling the read pulse width can increase the subsequent time delay. Conversely, doubling the write pulse width or skipping the read pulse will shorten the time delay.

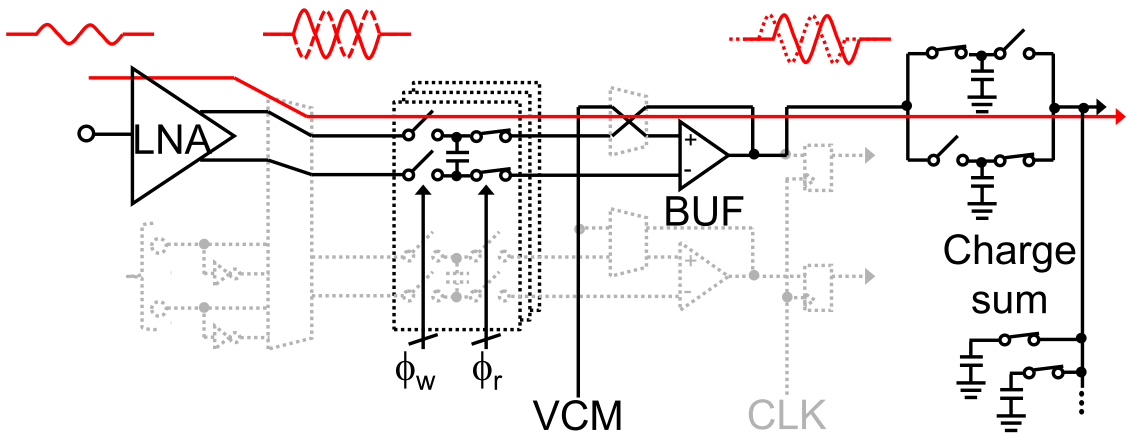


Figure 3.17 RX operation of proposed SCD.

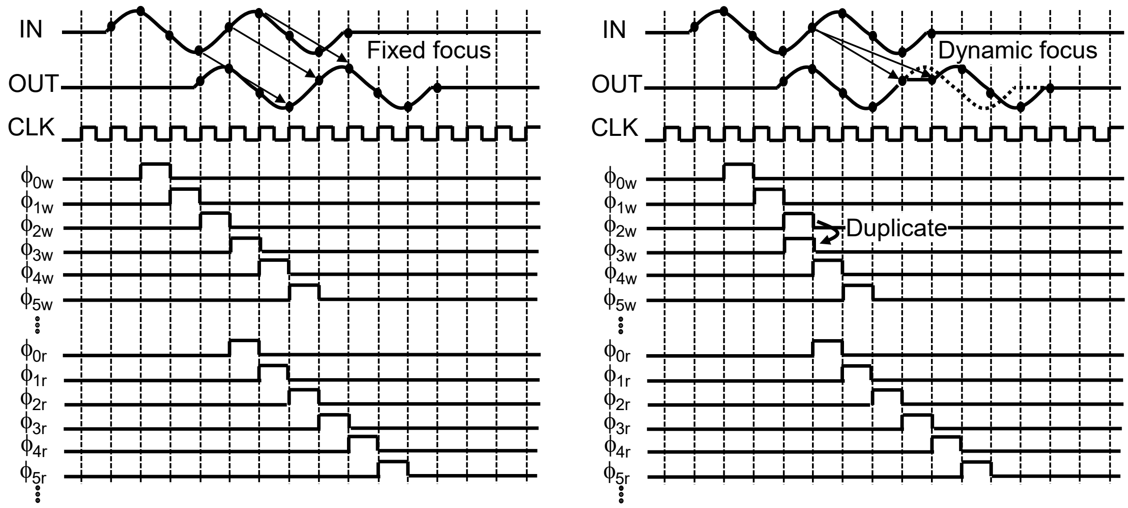


Figure 3.18 Timing chart of RX fixed focus (left) and dynamic focus (right).

3.3.3 Charge Domain Adder

As mentioned earlier, CDADD performs coherent addition of the 24 BDR-SCD outputs in the charge domain. Because of its passive operation, it consumes only clock distribution power. As shown in Figures 3.14 and 3.17, the signal is sampled alternately on the two capacitors, and the hold node is shorted between the EChs to redistribute the charge. Although this is correctly averaging rather than summing the signals, we will refer to it as summation for convenience.

Figure 3.19 (a) shows the schematic of CDADD, and (b) shows the timing diagram of its operation. Charge is alternately sampled to the two C_{add} capacitors connected to the plate nodes V_{ct} and V_{cb}, and the output in the hold state is shorted between 24-ECh to form the summed output. C_{par} is the wiring parasitic capacitance. During the hold phase, charge redistribution occurs across the 24 C_{add} and C_{par} capacitors. While C_{add} capacitors are distributed across each ECh area, the wiring that shorts each ECh output extends a long distance outside the array, causing large C_{par} to affect the bandwidth. Figure 3.20(a) shows the transfer characteristics of the CDADD, and (b) shows a step response as an example of the frequency response. Due to the charge sharing effect of the 24 C_{add} and C_{par}, even when a step with an amplitude of V_s is applied to the input, the output does not reach a swing of V_s within one clock cycle, exhibiting the hysteresis characteristics shown in the transfer characteristic (a). Here, G_s and G_p are expressed by the following equations.

$$G_s = \frac{24C_{add}}{24C_{add} + C_{par}} \tag{3.2}$$

$$G_p = \frac{C_{par}}{24C_{add} + C_{par}} \tag{3.3}$$

Therefore, the transfer function is as follows.

$$\frac{V_{out}}{V_{in}} = \frac{G_s}{1 - G_p z^{-1}} \tag{3.4}$$

As a result, the step response gradually approaches V_s while repeatedly sharing charge between 24 C_{add} and C_{par}, as shown in Figure 3.20(b).To achieve a wider bandwidth, one option is to increase C_{add} or decrease C_{par}. However, C_{par} is actually determined by the parasitic capacitance of long-distance wiring, making it difficult to reduce. In this design, we selected C_{add} to meet the target bandwidth of up to 5 MHz. Additionally, bandwidth expansion through charge reset at each cycle is also possible. However, in this design, low power dissipation and small area were prioritized.

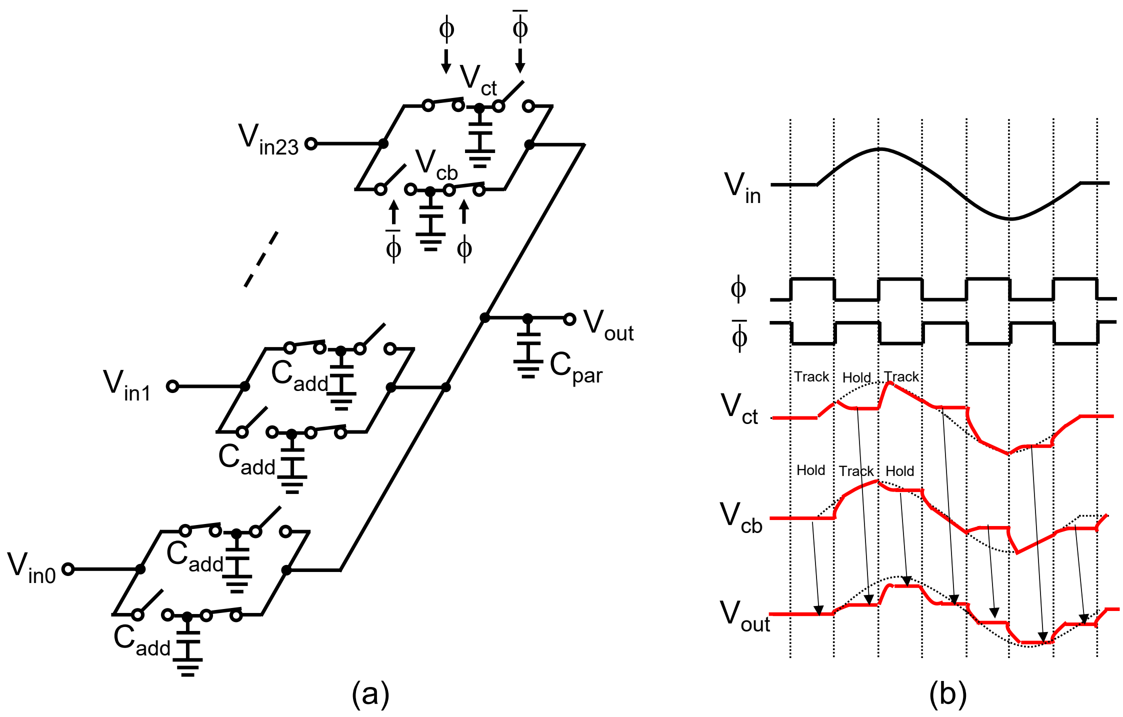


Figure 3.19 CDADD timing diagram.

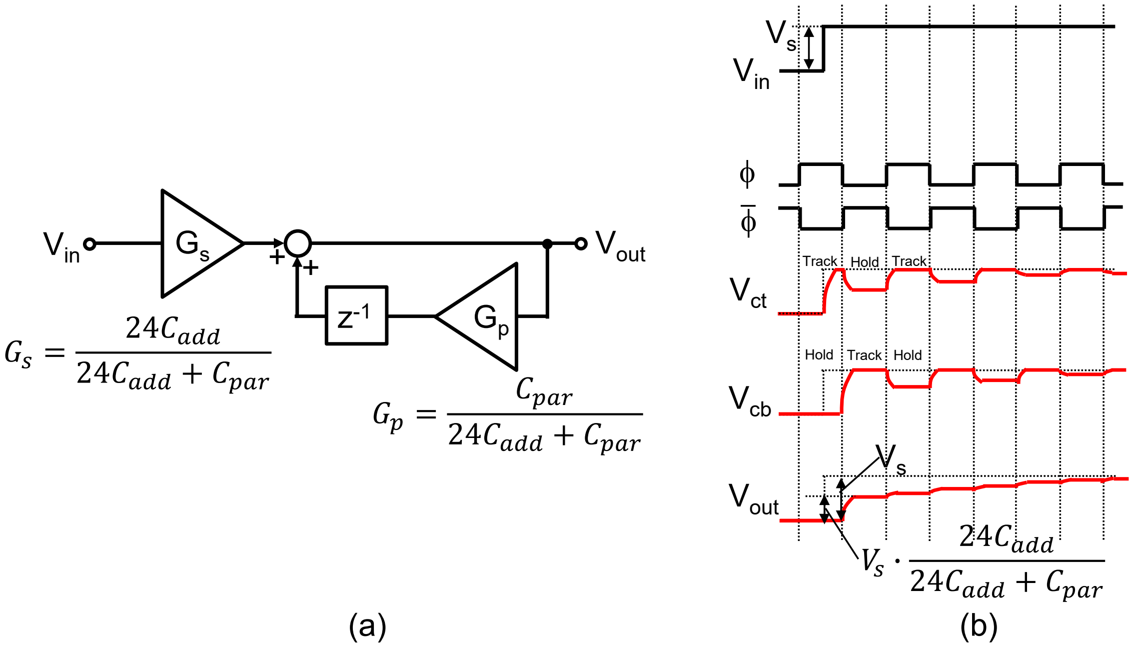


Figure 3.20 CDADD transfer characteristic and step response.

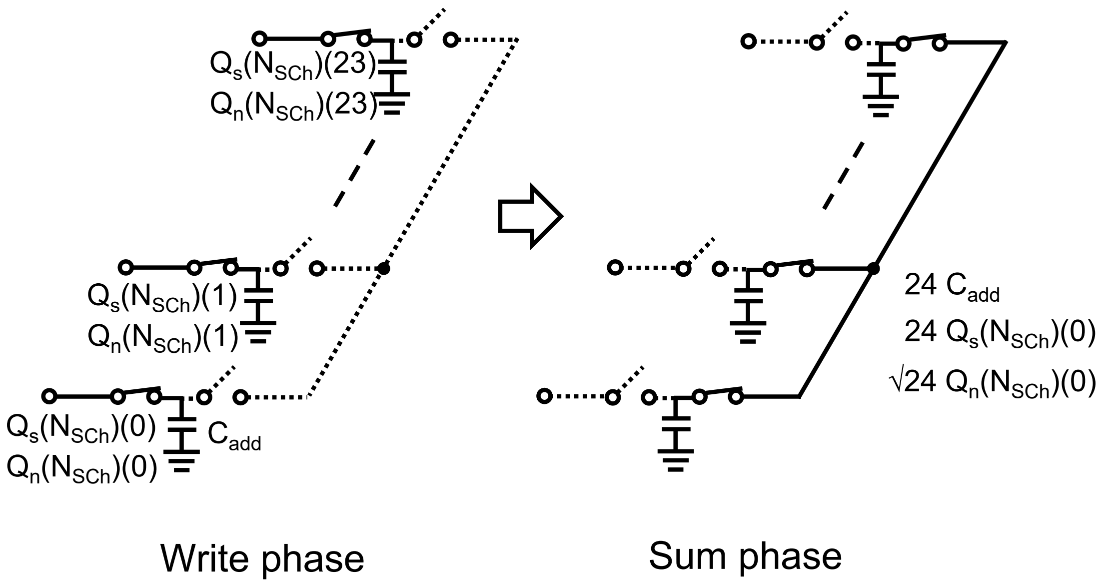


Figure 3.21 CDADD noise reduction mechanism.

The noise reduction mechanism of CDADD are explained using Figure 3.21. Let each CDADD input signal on the SCh be $S_{in}(NSCh)(NECh)$, and ignore C_{par} for simplicity. Then the stored charge $Q_s(N_{SCh})(N_{ECh})$ in the write phase is as follows:

$$Q_s(N_{SCh})(N_{ECh}) = C_{add}(N_{SCh})(N_{ECh}) \cdot S_{in}(N_{SCh})(N_{ECh}) \tag{3.5}$$

Assuming that the signals are coherently aligned at the SCD output due to the delay, the signal charge from each ECh is redistributed when transitioning to the addition phase, resulting in the following signal charge.

$$Q_s(N_{SCh}) = \sum_{N_{ECh}=0}^{23} Q_s(N_{SCh})(N_{ECh}) = 24Q_s(N_{SCh})(0) \tag{3.6}$$

On the other hand, the noise charges Q_n are uncorrelated and random among the EChs, so these are summed in power, resulting in the following.

$$Q_n(N_{SCh}) = \sqrt{\sum_{N_{ECh}=0}^{23} Q_n^2(N_{SCh})(N_{ECh})} = \sqrt{24}Q_n(N_{SCh})(0) \tag{3.7}$$

Therefore, the signal charge after summation is 24 times larger than each ECh signal charge, and the noise charge is√ 24 times larger, and the summation improves SNR by √ 24 times = 13.8 dB.

Figure 3.22 shows the CDADD transient noise simulation results when the CDADD input is grounded. The plot compares the CDADD output noise of 1-ECh with the CDADD output noise of 24-ECh (= 1-SCh). This signal processing reduces the noise level instead of amplifying the signal. This feature is important for headroom considerations because a simple 24-signal summation scheme would increase the SCh signal by 27.6 dB (= 20 log 24), resulting in DR issues.

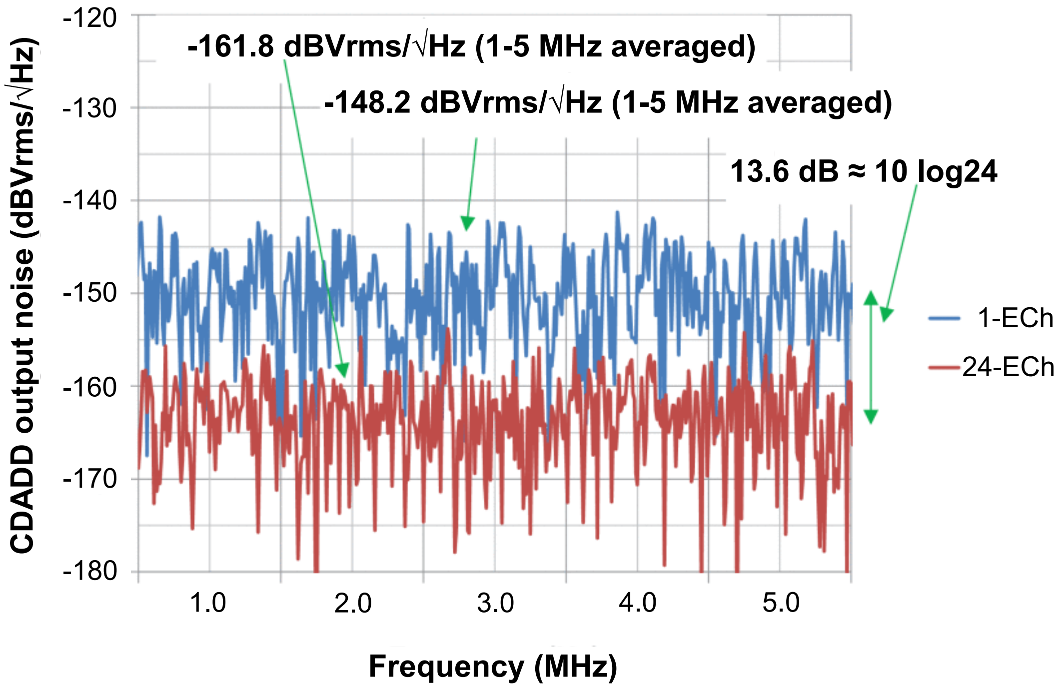


Figure 3.22 CDADD output noise (transient noise simulation results).

Throughout Section 3.3, we have described the design of an ABF circuit consisting of BDR-SCD and CDDADD. The area breakdown of the ECh is shown in Figure 3.23. The TX pulser, which contains a significant amount of HV-MOS, occupies 43 % of the area, followed by BDR-SCD + CDDADD, which occupies 34 % of the area.

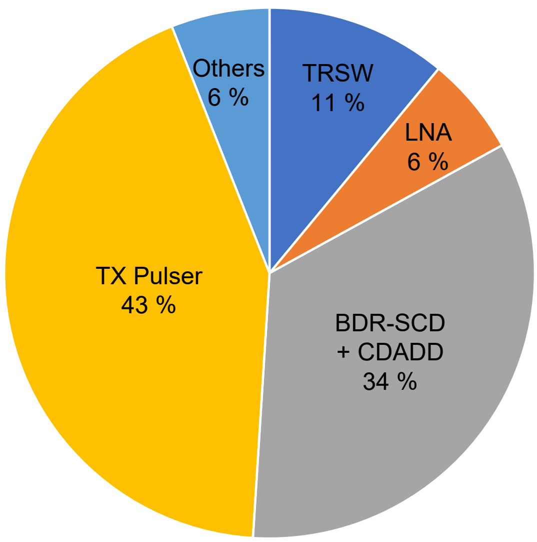


Figure 3.23 ECh area breakdown.

3.4 Evaluation

In this section, the electrical and image evaluation results of the designed 2-D array IC are presented. Figure 3.24 shows a die photograph of the 2-D array IC implemented with a 180-nm HV SOI CMOS technology. With the circuit implementation strategy described above, all of the ECh transceiver circuits occupy only a 300 μm × 300 μm area; the total die size, including the TX DBF, control peripherals, and interface circuits, is 417 mm^2 (22.4 mm × 18.6 mm). Figure 3.25 shows the evaluation setup. Since electrical evaluation is constrained after assembly into a matrix probe, an evaluation board for functional and performance testing was also prepared. To measure RX analog electrical characteristics, a signal is injected into the TD-side I/O of the ECh and a cable connection is made through the FPC using a holder.

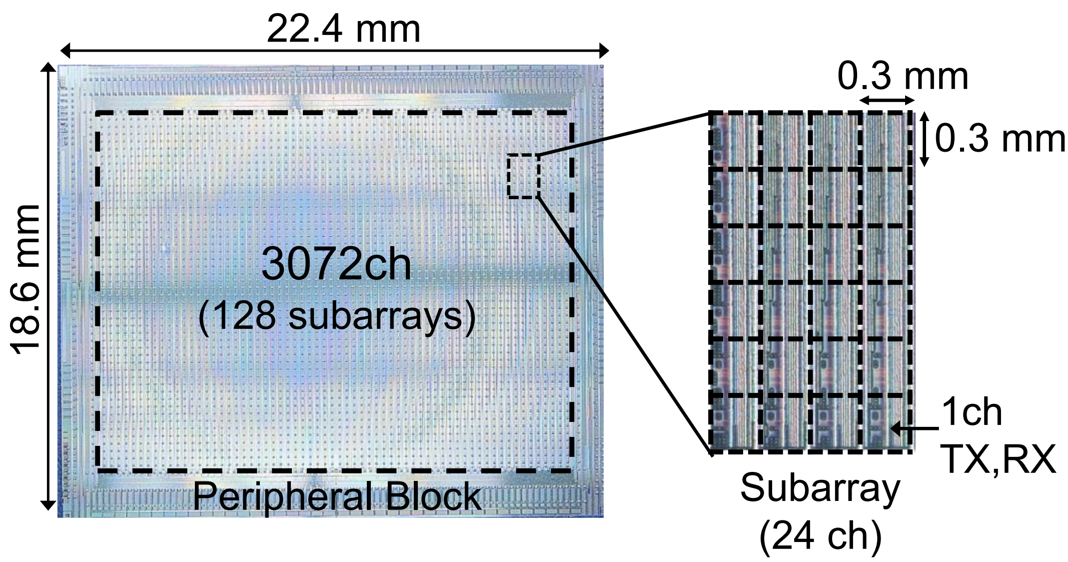


Figure 3.24 Die photograph.

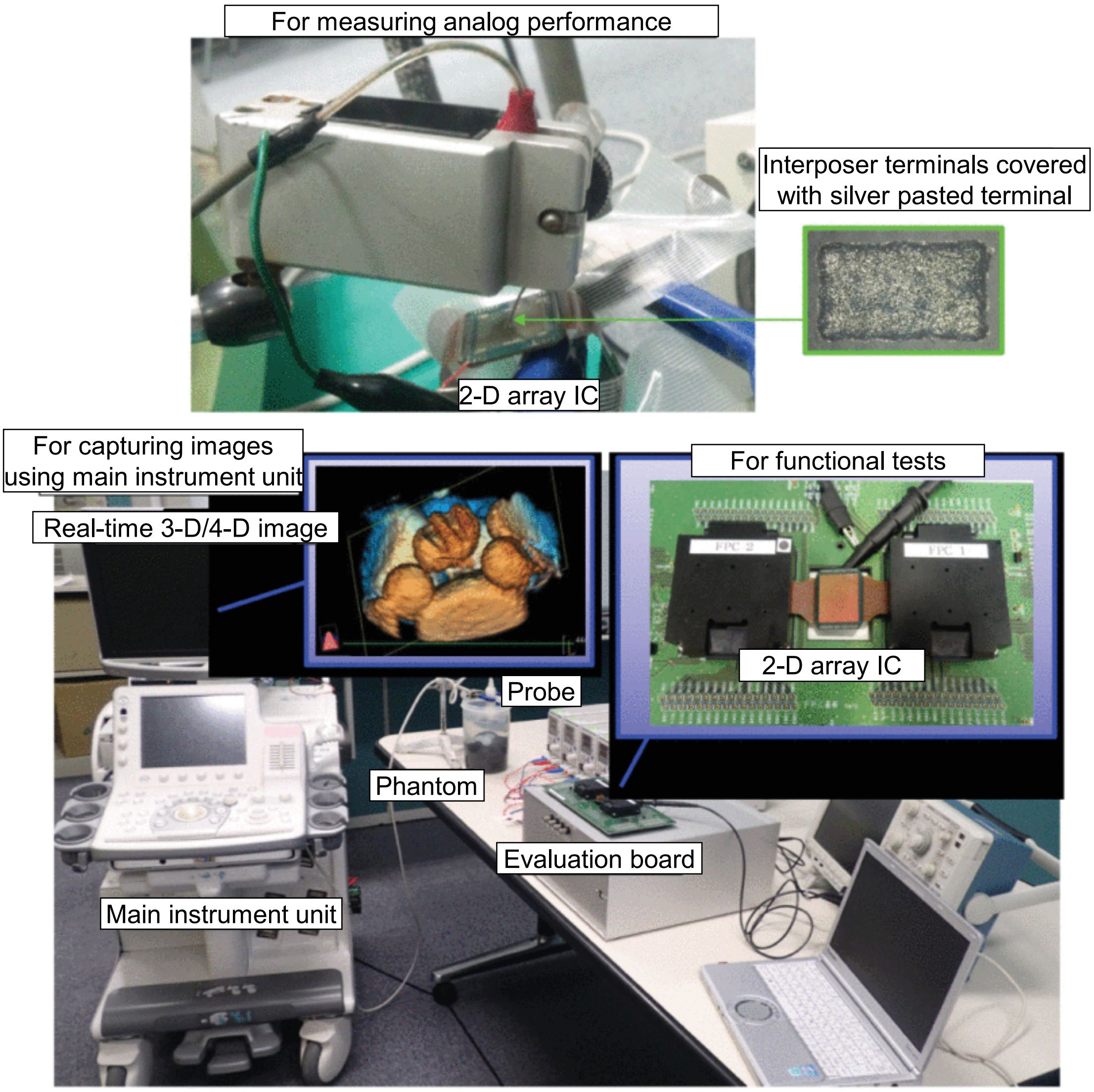


Figure 3.25 Evaluation setups for measuring analog performances (top), capturing images using the main instrument unit (bottom left), and functional tests (bottom right).

3.4.1 Electrical Evaluation

Figure 3.26 shows the measurement results of TX pulser. The maximum amplitude is 138 Vpp under a ±70 V HV supply, the world's largest maximum amplitude for a 2-D array IC. The amplitude control characteristics are shown in the upper right of Figure 3.26, and the slew rate variable characteristics are shown in the lower right. The maximum amplitude characteristics were measured under ±70 V supply, while the amplitude and slew rate variable characteristics were measured under ±30 V supply. The slight shift of the zero level from 0 V is due to the forward voltage of the HV diode in the RZ circuit. The amplitude can be controlled without degrading the waveform, and the high-side and low-side slew rates can be adjusted independently, allowing independent compensation of PMOS and NMOS variations.

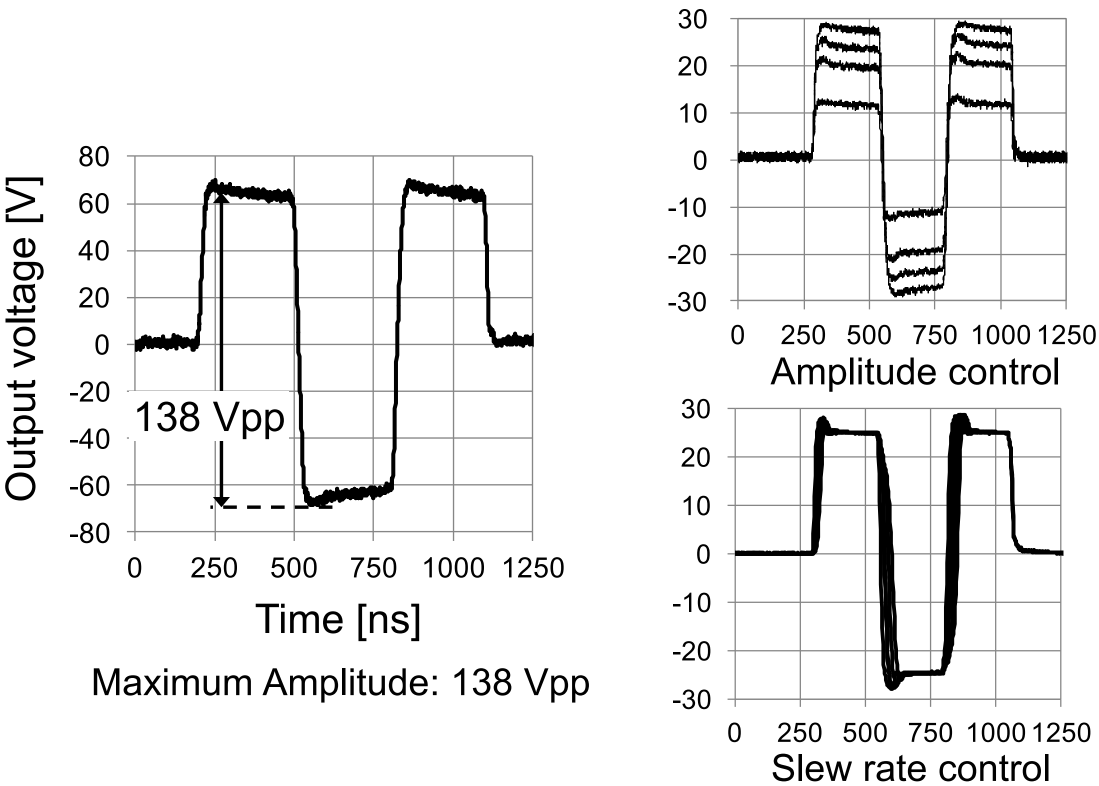


Figure 3.26 Measured TX characteristics: waveform with maximum amplitude (left), amplitude control (top right), and slew rate control (bottom right).

Figure 3.27 shows the measured input and output signals of the RX chain under different delay settings of the BDR-SCD. Two cycles of sinusoidal burst signals at 1.6 MHz were input to an SCh, where 24-ECh pads on the interposer were shorted together using conductive silver paste, as shown in Figure 3.25, top. The output signal without cable load was observed. An overall gain of 6.2 dB was achieved with the expected signal delay. Figure 3.28 shows the RX frequency response with and without cable load. The gain with cable load is -16.5 dB due to the voltage division between the output impedance of the CBUF and the input impedance of the main instrument unit. The upper cutoff frequency (-3 dB) is 1 MHz lower with cable load than without.

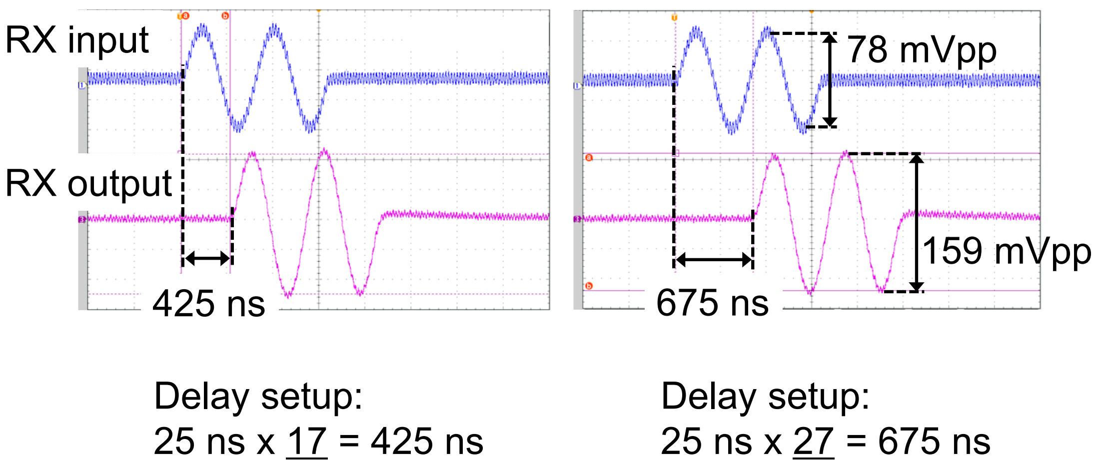


Figure 3.27 Measured RX chain input and output signals with different SCD time delay settings.

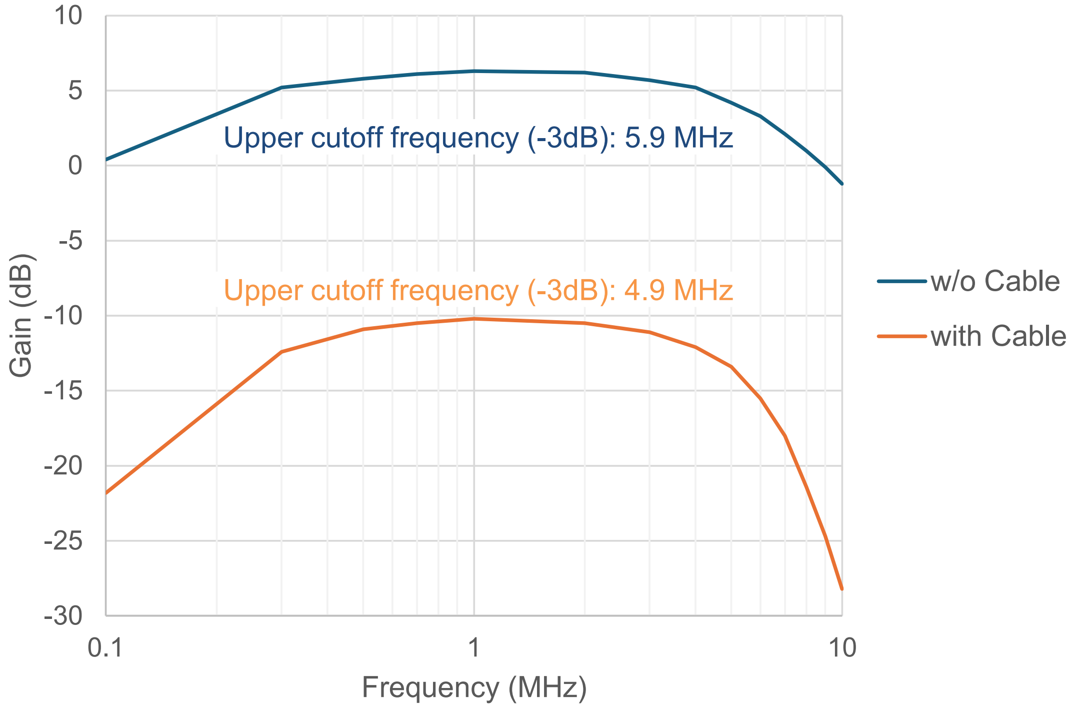


Figure 3.28 Measured RX gain-frequency characteristics with and w/o cable load.

Table 3.2 provides a summary of the measured RX performance. The minimum and maximum input levels are measured with the same LNA input impedance and gain configuration. By utilizing variable input impedance and gain, a DR of 85 dB is achieved. SCh-to-SCh isolation was found to be 43 dB at a frequency of 1.6 MHz and is limited by the adjacent allocated connector pins in the main instrument unit.

Table 3.2 RX performance summary

	Unit	Measured results
Small signal gain	dB	6.3
Minimum input level	dBμV	26
Maxim input level	dBμV	111
Dynamic range	dB	85
Upper cutoff frequency	MHz	4.9
SCh-to-SCh isolation	dB	43

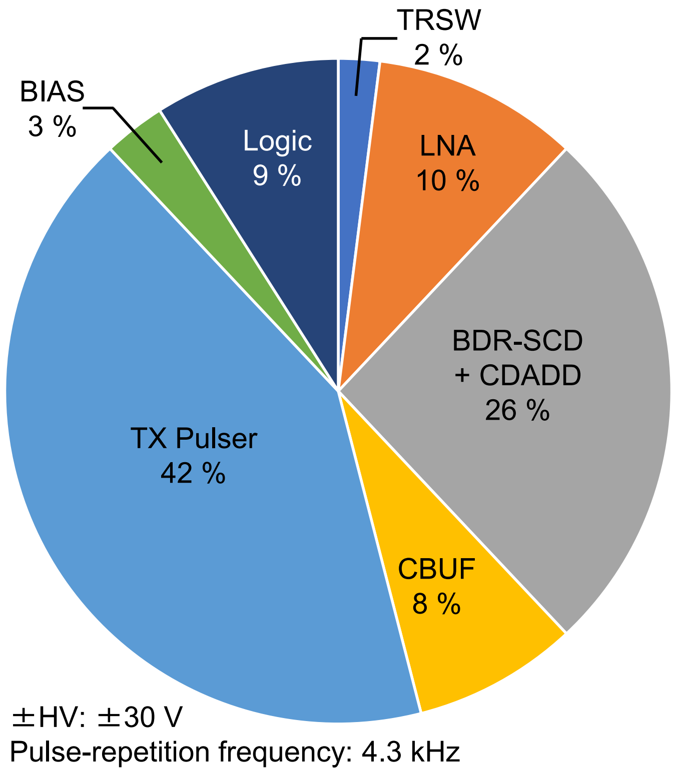


Figure 3.29 Power breakdown in B-mode at 0.74 mW/ECh.

Figure 3.29 illustrates the power breakdown expressed per ECh. The pie chart includes all blocks of the proposed 2-D array IC, including the TX DBF, which is counted as logic, and bias peripherals. In Figure 3.29, the power dissipation of TX pulser encompasses those of all associated analog and digital blocks, including amplitude and slew rate control blocks located outside the ECh area. TX pulser accounts for 42 % of the total power, followed by BDR-SCD + CDADD at 26 %. The total power is 0.74 mW/ECh in B-mode. Therefore, while the proposed 2-D array IC operates with all 3072-ECh transceivers active, the total power is 2.3 W.

3.4.2 Imaging Evaluation

The 2-D array IC was assembled and mounted on the matrix probe. The main instrument unit, equipped with a real-time rendering engine, was optimized and configured for the matrix probe. The proposed ultrasound system is capable of capturing 3-D tissue images within the angle of view (AoV) of this system. Arbitrary 2-D cross-sectional images can be easily extracted from the full-volume 3-D dataset. Specific cross-sections of a dynamic, complex, and micro-shaped heart can be simultaneously displayed and easily retrieved offline. The system's AoV is 90 degrees × 90 degrees, allowing the entire human heart to be viewed during an echocardiographic examination. Figure 3.30 illustrates a 3-D image of a ball phantom (white ball: agar, black ball: mixture of agar and graphite) and a corresponding 2-D image along the indicated cross-section guide. It can be seen that the 3-D image and the cross-sectional 2-D image are clearly displayed.

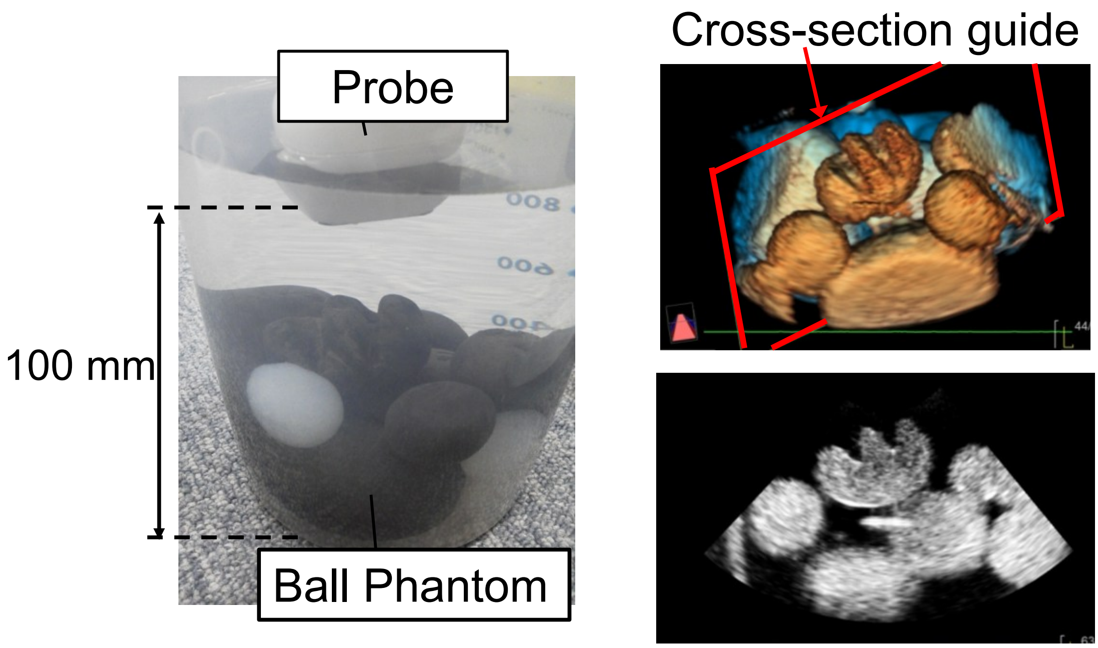


Figure 3.30 Acquired 3-D image (top right) and 2-D cross-section image (bottom right) of ball phantom in water.

Figure 3.31 shows B-mode fundamental and THI images of a multipurpose phantom with a nylon filament point target mimicking tissue. To minimize the acoustic impedance mismatch between the acoustic lens on the matrix probe and the phantom, a few millimeters of space was filled with water between them. Therefore, the depth ruler shown in Figure 3.31 and the position of the nylon filament in the phantom differ, with an offset of approximately 1 cm. The gray cloud in the background is known as speckle noise and is caused by tissue-mimicking material consisting of subwavelength scatterers within the phantom. As mentioned above, the THI image has higher contrast and resolution than the fundamental image. THI image also has less speckle noise. The nylon filaments, 2-3 mm apart, can be identified as separate dots in the fundamental image. However, close targets such as C-D-E in Figure 3.31, which cannot be separated in the fundamental image, are independently identified as separate dots in the THI image.

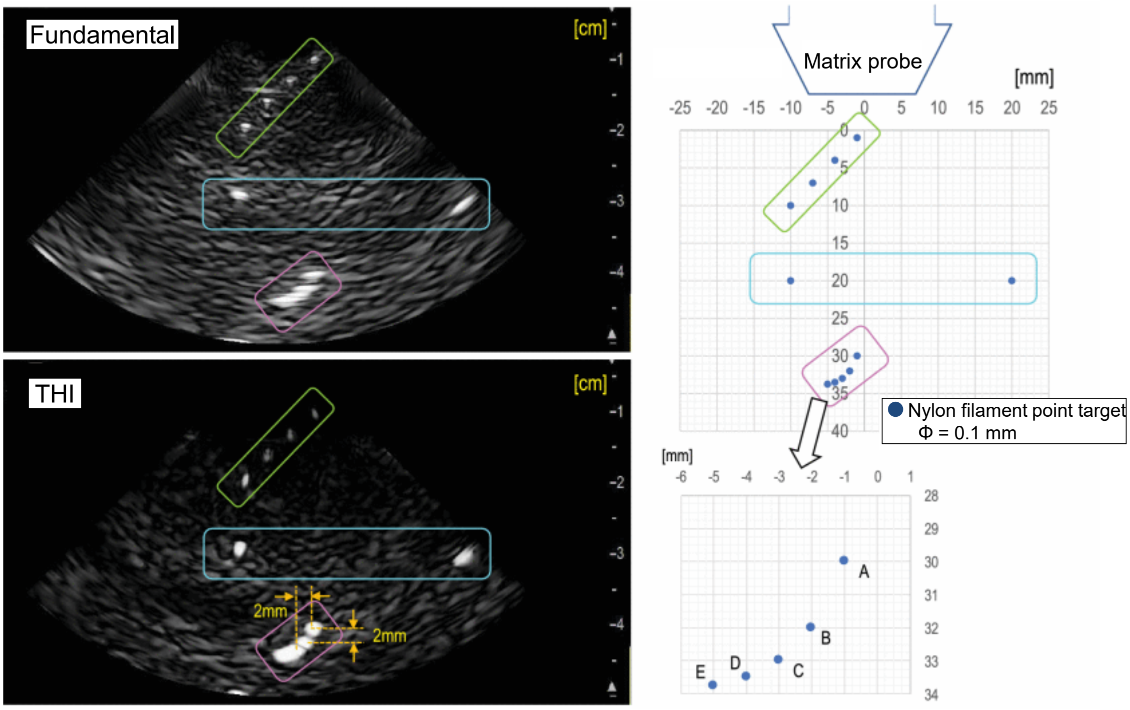


Figure 3.31 Acquired B-mode images using fundamental wave (top left) and THI (bottom left) of a tissue-mimicking phantom with nylon filament targets (right).

Table 3.3 shows a comparison of the 2-D array ICs. Only the 2-D array IC in this study is capable of performing echocardiography, including analog RX and all-digital TX μBF, bipolar TX pulser, and associated peripheral blocks. The silicon area is 0.09 mm^2/ECh and the power dissipation during B-mode operation is 0.74 mW/ECh. The bipolar 138 Vpp TX capability is the largest amplitude ever achieved worldwide. The power dissipation of 0.74 mW/ECh is the lowest in the table, even though all necessary functions are activated. The resulting imaging performance, as shown in Figures 3.30 and 3.31, is adequate for echocardiography applications.

Table 3.3 2-D array IC comparison

	This work	ISSCC2015 [32]	TBioCAS2014 [33]	TBioCAS2013 [34]	JSSC2016 [35]	JSSC2013 [36]	JSSC2017 [37]	ISSCC2018 [38]
Integration	Analog RX/ All-digital TX	RX/TX	Analog+ Digital RX	RX/TX	RX/TX	RX/TX	RX	RX/All-digital TX
Number of EChs	3072	7	64	256	256	4	1024	64
Number of SChs	128	7	1	256	256	4	96	8
Die size (mm^2)	416.64	2	19.4	60.0	33.0	-	37.21	28.6
ECh area (mm^2)	0.09	0.08	0.303	0.234	0.07	0.33	0.022	0.26
Power/Ech (mW/Ech)	0.74[(1)]	18.6	17.8 (no TX)	0.6[(2)]	8.5	66.7	0.27 (no TX)	6.26
Intra-SCh delay resolution (ns)	25	5 (TX only)	6.25	-	-	-	30	5 ns resolution with TDM[(3)] no analog delayer
Intra-SCh Max. delay (ns)	750 (BDR-SCD)	-	1000 (SCD)	-	-	-	210 (SCD)	
Inter-SCh Max. delay (μs)	12.8 (TX DBF)	-	11.2 (RX FIFO)	-	-	-	-	10.235 (TX DBF)
TX Max. amplitude (V_{pp})	138 (Bipolar)	32 (Unipolar)	-	25 (Unipolar)	30 (Unipolar)	30 (Unipolar)	-	60 (Unipolar)
TD type	Bulk piezoelectric material	PMUT	CMUT	CMUT	CMUT	CMUT	PZT	PZT or CMUT
Technology	180-nm HV SOI CMOS	TSMC 180-nm 5V/32V CMOS	130-nm CMOS	1.5-μm HV process	TSMC 180-nm HV CMOS	TSMC 180-nm HV CMOS	180-nm LV CMOS	TowerJazz 180-nm HV BCD

(1) Under B-mode imaging condition

TX: ±HV=±30 V, Center frequency 2 MHz, Pulse-repetition frequency 4.3 kHz,

RX: Input sensitivity 56 mV_{pp}, Dynamic range 85 dB, -3 dB Bandwidth 4.6 MHz

(2) In RX mode, only 16 Echs are deployed.

(3) Time-Division Multiplexing

3.5 Conclusions

In this study, a single-chip 3072-ECh/128-SCh 2-D array IC with analog RX and all-digital TX μBF is proposed for echocardiography. The ECh transceiver includes a three-level TX pulser, TRSW, LNA, BDR-SCD, and a 24-ECh-to-1-SCh CDADD. To fit within the 300 μm × 300 μm ECh target area, as constrained by the grating lobe, frequency, and AoV requirements, a BDR-SCD, which is time-shared between TX and RX, was proposed. The BDR-SCD was applied to both the logic delay of a 2-bit bus signal for the three-level TX pulser and the RX analog signal delay. The CDADD required for the analog μBF performs a passive charge redistribution operation for low power.

The proposed 2-D array IC, which includes a 3072-ECh transceiver, 128-SCh CBUFs, bias peripherals, TX DBF, and control and interface circuitry, was fabricated with a 180-nm HV SOI CMOS technology. Each ECh transceiver consumes only 0.74 mW in B-mode operation and 2.3 W when all 3072 EChs are active, with 85 dB RX DR, 25 ns delay resolution, 750 ns maximum delay for μBF, and 138 Vpp TX capability. The total die area is 417 mm^2. It is connected to the main instrument unit and has been successfully used to render and display 2-D/3-D phantom images.

Chapter 4
T/R Switch Composed of Three HV-MOSFETs

4.1 Background

In the previous chapter, we discussed methods for reducing the area and power dissipation of the 2-D array IC. In particular, we reduced the area of the ABF, which consists of delayers and an adder, by time-sharing the delayers between the TX and RX, thus fitting the circuit area of 1-ECh to 300 μm × 300 μm. The passive charge redistribution operation of the CDADD also contributes to a low power dissipation of 0.74 mW/ECh. Although it does not directly contribute to the TX and RX signal processing, this chapter describes the reduction in area and power dissipation of the TRSW, which is inserted in the RX signal path to protect the LV RX from the HV TX pulse.

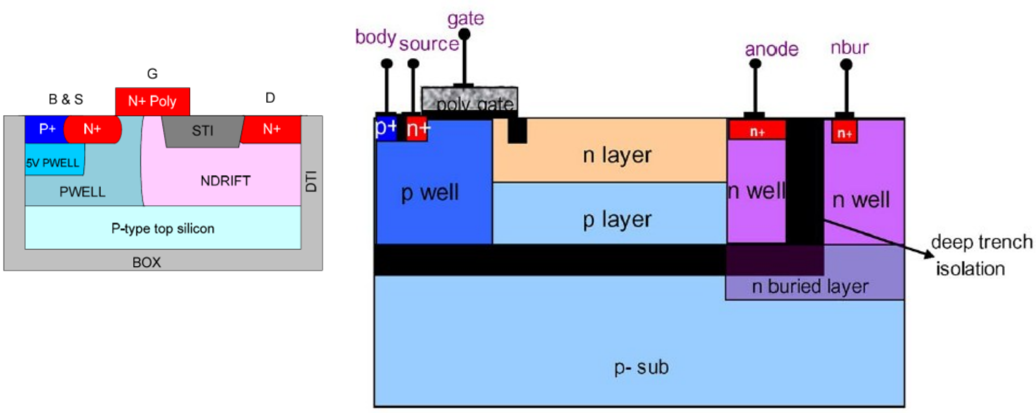
The TX and RX electronics of the 2-D array IC are connected one-to-one to the TDs, and the TX and RX share the TD by time division. The TX uses HV devices and drives the TD with three-level bipolar pulses of approximately 60 Vpp or more to ensure the required sound pressure. Meanwhile, the RX electronic circuit is designed using LV devices. Therefore, the transceiver inherently requires a TRSW with HV devices between the TD and the RX circuit to protect the RX electronics in the LV domain [45],[46].

In conventional 1-D probes, only the TD is mounted on the probe, while the transceivers are mounted on the main instrument unit. In this case, a diode bridge and diode limiter composed of discrete components cover the TX/RX isolation [47]. Recently, bipolar CMOS DMOS (BCD) technology has become available, enabling mixed LV-CMOS and HV double-diffused MOS (DMOS) [48]. Super-junction laterally-diffused

MOS (SJ-LDMOS) has a structure in which current flows through a vertical PN junction, enabling low on-resistance and a breakdown voltage higher than 100 V [49][50][51][52]. The in-probe ASIC mainly uses laterally diffused MOS (LDMOS) based TX electronics and TRSW [46], [53].

LDMOS and SJ-LDMOS are area-hungry because they require a drift length between the drain and gate, as shown in Figure 4.1, to ensure a high breakdown voltage. In the 2-D array IC, the range of ultrasound frequencies and steering angles limits the pitch of the TD, subject to the constraint that no grating lobes are generated within the steering angle. Accordingly, as described in Chapter 2, this study required fitting the ECh circuit into a 300 μm square. One of the keys to realizing the 2-D array IC lies in implementing HV-TX and TRSW with fewer HV-LDMOSs, while keeping them within the target area.

Power dissipation is another constraint for designing the 2-D array IC in the probe. Since the probe head is in continuous contact with the examinee during the examination, the power budget of the 2-D array IC must be set considering the heat dissipation by natural air cooling from the surface of the probe housing, the heat generated by the TD, and the heat generated by the 2-D array IC to prevent burns. The TX pulser requires a certain power to ensure the HV amplitude signal, which involves charging and discharging the TD load. The LNA in the RX also needs some power for low noise. Therefore, we are motivated to develop a TRSW with almost negligible power dissipation.



(a) (b)

Figure 4.1 Cross-sectional view of HV-MOS: (a) LDMOS. (b) SJ-LDMOS. Reproduced from [48], [51].

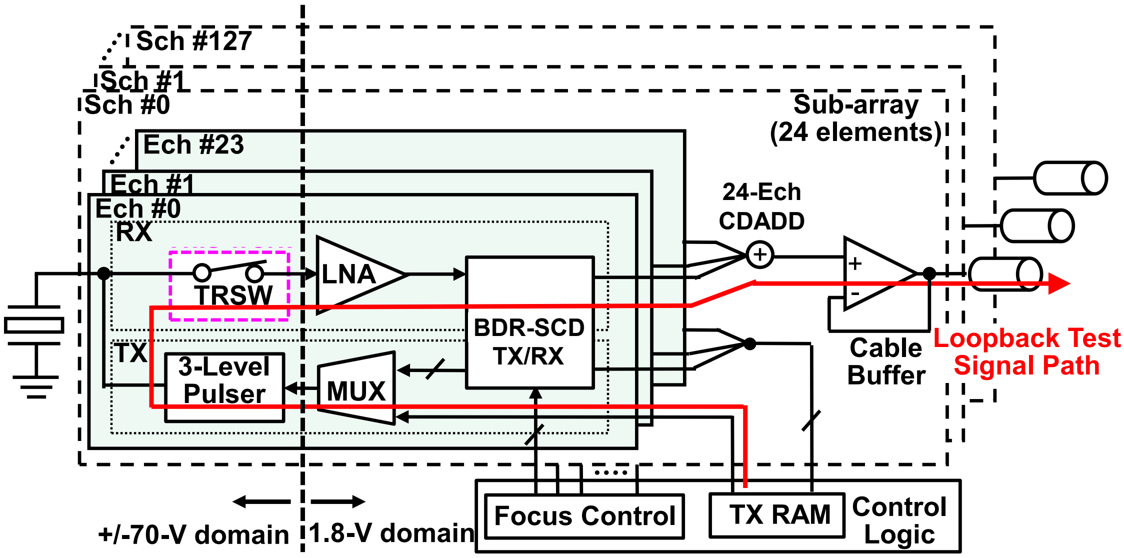


Figure 4.2 Block diagram of 2-D array IC in matrix probe and signal loopback test path (red line).

Reducing switching noise in the TRSW is also an issue: when the TRSW switches from the off state to the on state, i.e., from TX to RX, parasitic capacitive coupling generates a spike of switching noise that affects the image. The TD converts this noise into undesired sound, and the sound pulse is propagated into the body, causing image artifacts. The undesired sound associated with switching must be kept below the lower limit of the DR.

Chip yield is also a concern in this study, as the 2-D array IC contains 3072 transceivers, resulting in a large chip area. All channels should be tested to identify and screen defective ones. However, it is not practical to probe all the dense 3072 electrodes on the 2-D array IC during wafer testing. It is desirable to loop back the signal from TX to RX inside the 2-D array IC and test the AC signal continuity. This test eliminates the need to discard components such as TDs and acoustic backing material after defects are found in the 2-D array IC assembled into the probe. Loopback testing is so far applied to millimeter-wave transceivers [54], ADCs and DACs [55], high-speed serial interfaces [56], serializers/deserializers (SERDES) [57], and mixed-signal circuits including DACs and ADCs [58], [59]. One of the objectives of this study is to utilize the TRSW between TX and RX as an attenuator in the internal loopback test, thereby enabling loopback testing with minimal addition of new resources. In other words, the test function is implemented in an area-efficient manner by looping back the TX waveform inside the IC, attenuating it with the TRSW, and inputting it to the RX LNA, as shown by the red line in Figure 4.2.

This chapter describes the realization of a small-area TRSW to fit the transcever circuit area into a single channel of 300 μm square. Specifically, we constructed a TRSW using a small number of HV-MOSs and realized the world's first true 3-HV-MOS configuration for a bipolar pulse-compatible TRSW. Furthermore, by operating the TRSW at almost zero power, the power dissipation of the 2-D array IC is reduced, thus achieving 0.74 mW/ECh. In addition, the TX/RX switching noise is kept below the lower limit of the DR that does not affect images. Finally, we implemented an AC continuity test function that loops back the AC signal from TX to RX in the 2-D array IC using the TRSW as an attenuator. The following Section 4.2 describes the circuit implementation, Section 4.3 describes the reduction of switching noise in TX/RX switching, Section 4.4 describes the internal loopback test per ECh, Section 4.5 reviews evaluation results, and Section 4.6 presents the conclusions.

4.2 Design of a Small-Area Low-Power T/R switch

In this section, we describe a novel TRSW architecture consisting of only three HV-MOSs. Since power injected into the switches does not contribute to transceiver performance, the architecture is designed to achieve negligible power dissipation compared to the power required for the TX and RX.

4.2.1 Basic Circuit Topology

As already mentioned in the background, the TRSW is turned off during the TX period to protect the LNA in the LV 1.8 V domain; it is turned on during the RX period to allow small signal echoes to pass through. We now define the difference between a high-voltage switch (HVSW) and a TRSW. In this paper, the switch that transfers HV pulses during the TX period is called the HVSW. On the other hand, a switch that transfers only RX small signals is called a TRSW. For example, when multiple TDs share one TX electronics, the HVSW is used as a multiplexer [46], [63], [64], [65], [66], [67], [68], [69], [70], [71]. However, if TX and RX electronic circuits are placed for each ECh, as in this work, it is not necessary to transfer HV pulses, but only RX small signals, as TRSW [46], [53], [72], [73], [74]. In any case, the design of the HVSW and TRSW will basically take the same approach.

Furthermore, TRSW can be classified into two types of switches: one for unipolar HV pulses and one for bipolar HV pulses; TD is normally connected to 0 V. Unipolar TX outputs 0 V to +HV or 0 V to -HV, while bipolar TX outputs +HV to -HV around 0 V. The TRSW for unipolar pulses can be configured with a single HV-MOS [46], [74], while the TRSW for bipolar pulses requires at least two HV-MOSs connected in series to isolate the LNA from both +HV and -HV.

Figure 4.3 shows a simplified schematic of the bipolar pulse-tolerant TRSW expressed using ideal switches (SWs). In this schematic, the two circled HV-NMOSs are connected back-to-back, sharing a common gate and source. During TX period (a), SW_1 is turned off and SW_2 is turned on, and M_1 and M_2 are both off. Here, during +HV transmission, the common gate and common source of M_1 and M_2 remain at 0 V. During -HV transmission, the body diode D_1 becomes forward, and the floating common source and common gate are pulled to -HV. Therefore, the series of M_1 and M_2 is essential to isolate the RX in the LV region from the bipolar HV pulse. During the RX period shown in Figure 4.3(b), M_1 and M_2 are turned on by applying LV-VDD of 5 V in terms of V_{gs} with SW_1 on and SW_2 off. For a small area, the challenge is how to realize the floating on/off control unit shown in Figure 4.3 with fewer HV-MOSs and how to ensure the off state of TRSW during HV transmission. Additionally, to achieve low power dissipation, it is necessary to eliminate the static current path through the HV power supply.

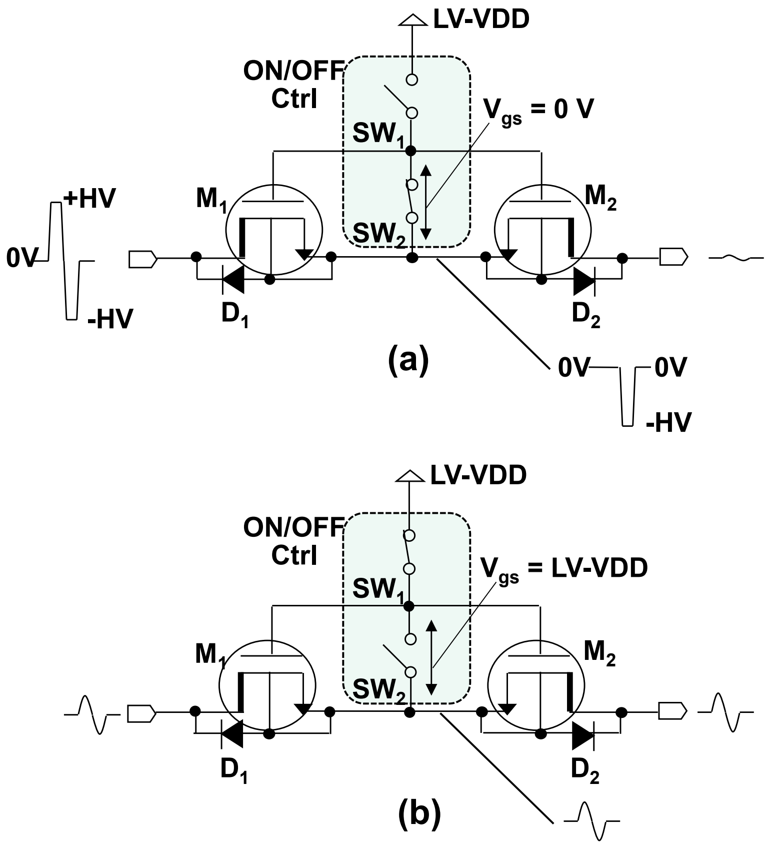


Figure 4.3 Basic bipolar-pulse-acceptable TRSW implementation and operation. in (a) TX: off and (b) RX: on.

Prior TRSW topologies have been proposed that assure the off state of two HV-NMOSs in series even during -HV transmission, as shown in Figure 4.4. All of these topologies consist of four or more HV-MOSs, including two HV-NMOSs in series. It is assumed that the V_{ds} of HV-MOS is HV tolerant; however, only LV can be applied in terms of V_{gs}. First, the Zener diode bias topology, shown in Figure 4.4(a), requires five or more HV-MOS devices. This topology includes a bi-directional current source consisting of an HV-PMOS M_3 that supplies current to D_1 to turn the TRSW on with V_{gs} of Zener voltage and an HV-NMOS M_4 that sinks current through D_1 to turn the TRSW off with the forward D_1. This results in a power penalty because a current path towards the -HV supply is necessarily required. Although Zener diodes have recently become available for use in the regular BCD process [75], the feasibility of this topology is technology dependent.

The level shifter type, shown in Figure 4.4(b), also requires at least five HV-MOSs. During the TX period, LV-PMOS M_5 must be on throughout the -HV transmission to guarantee the off state of TRSW. HV-PMOS M_3 corresponds to SW_1 in Figure 4.3 and provides the on state of the TRSW by pulling up the common gate of HV-NMOSs.

The floating latch type requires four or more HV-MOSs. Since only LV can be applied between the gate-source of M_1 and M_2, a latch consisting of M_5 and M_6 can be constructed using only LV-NMOSs. However, this topology requires two HV-PMOSs to flip the latch, setting or resetting it. The advantage of this architecture is that it has zero static power. However, there is concern about floating V_{gs} drift due to charge loss from leakage, since V_{gs} of M_1 and M_2 must be held in parasitic or additional capacitors.

In this work, we propose the world's first true TRSW for bipolar pulses, utilizing only three HV-MOSs and eliminating the HV current path as well. To reduce the number of HV-MOSs, one strategy is to share the on/off control unit with multiple EChs [73]. However, as a result, they lose on/off control at the ECh granularity, where they lose the ability to capture echoes near the body surface because the TX/RX transition of the entire 2-D array IC must wait until all EChs finish TX. In addition, sharing the unit requires HV wiring over the ECh array, which wastes the limited channel space for wiring in consideration of the spacing between the LV and HV wires, resulting in a loss of wiring efficiency. The proposed TRSW architecture employs a dynamic shunt gate-source switch to ensure the TRSW is in the off state during TX periods and utilizes on/off control using a source-driven single HV-PMOS as described in the next section.

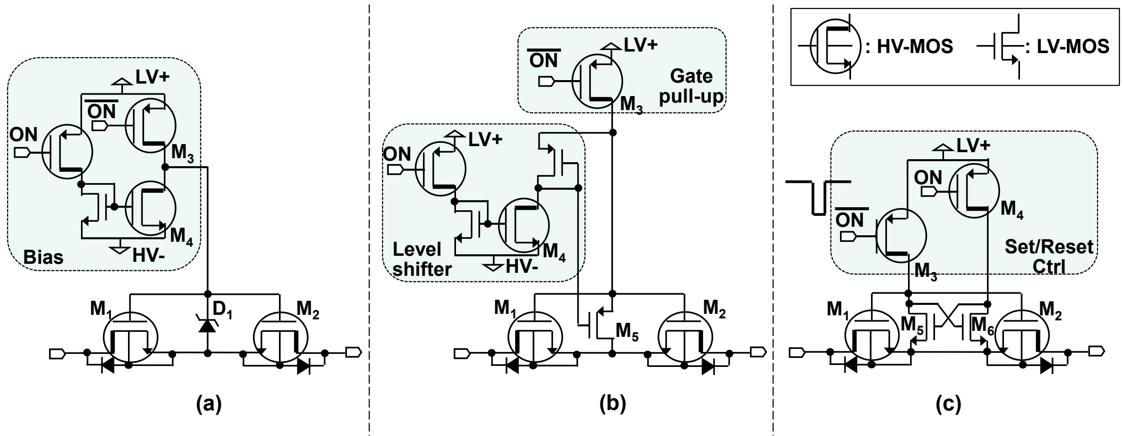


Figure 4.4 Comparison of prior TRSW topologies.(a) Zener diode bias [63], [64].
(b) Level-shifter-controlled gate-source switch [65], [66], [67], [72], [73].
(c) Floating latch [68], [69].

4.2.2 Dynamic Shunt Switch

Figure 4.5 shows a proposed TRSW that can be configured with only three HV-MOSs. Power dissipation is also low, as 12.1 μW for RX and zero for TX. The ideal SW_1 in Figure 4.3 is replaced by an HV-PMOS M_3 and SW_2 by a dynamic shunt SW consisting of a 5 V-NMOS and passive components. Prior to the TX period, where the TRSW is turned off, the voltage level of the 1.8V / 0V logic signal on input port "ON" is level shifted to 5V / 0V, and the source of M_3 is driven to near 0 V to turn M_3 off. During the TX period, the off state of TRSW is guaranteed by the dynamic shunt SW, which detects the transient rise in V_{gs} of M_1 and M_2 and shorts the V_G and V_S nodes.

When TRSW transitions to the RX period, the source of M_3 is driven to 5 V to turn M_3 on, and 5 V is applied between the common gate and source of M_1 and M_2 to keep TRSW on. 5 V / (2 MΩ + R_{in}) of static current is consumed during the RX period. The R_{leak} 2 MΩ resistor implemented using high-resistance poly silicon is a pull-down resistor to prevent the V_{gs} of M_1 and M_2 from drifting upward due to leakage in TX periods.

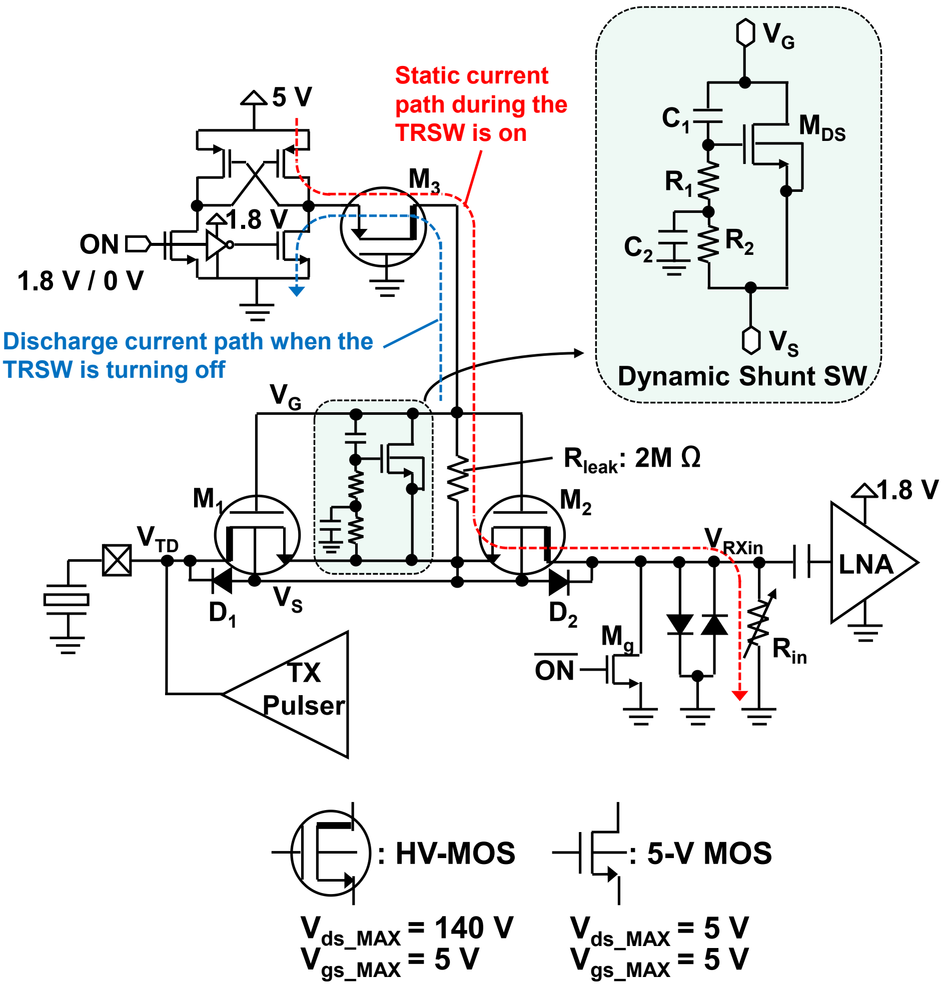


Figure 4.5 Schematic of the proposed TRSW with dynamic gate-source shunt switch.

Simulation waveforms of the proposed TRSW are shown in Figure 4.6. During the off period of the TRSW, the gate V_G and source V_S of M_1 and M_2 are in a floating state, and the M_{DS} gate of the dynamic shunt SW is off because it is pulled down through R_1 and R_2, as shown in Figure 4.5. When the TX pulser transmits -HV, body diode D_1 becomes forward, and the common source V_S is pulled down to -HV. Without a dynamic shunt SW, V_G remains near 0 V, while the V_{gs} of M_1 and M_2 increase, resulting in the TRSW going into the “on” state. However, thanks to the RC network in the dynamic shunt SW, when V_S goes down rapidly, M_{DS} gates try to stay at 0 V via C_2 and R_1, and as a result, the V_{gs} of M_{DS} increases. Then, M_{DS} turns on, and V_G and V_S are shorted to ensure the TRSW is in the “off” state. As shown in the third line in Figure 4.6, the V_{gs} of M_{DS} (dashed waveform) increases on the falling edge of TD voltage, V_{TD} at the top line. In other words, every time HV is transmitted, the dynamic shunt SW is automatically turned on to guarantee the off state of the TRSW. The bottom waveform in Figure 4.6 is the V_{gs} of M_1 and M_2 without the dynamic shunt SW, and M_1 and M_2 are turned on at the time of -HV transmission. Thus, the dynamic shunt SW works to ensure the TRSW is in the off state.

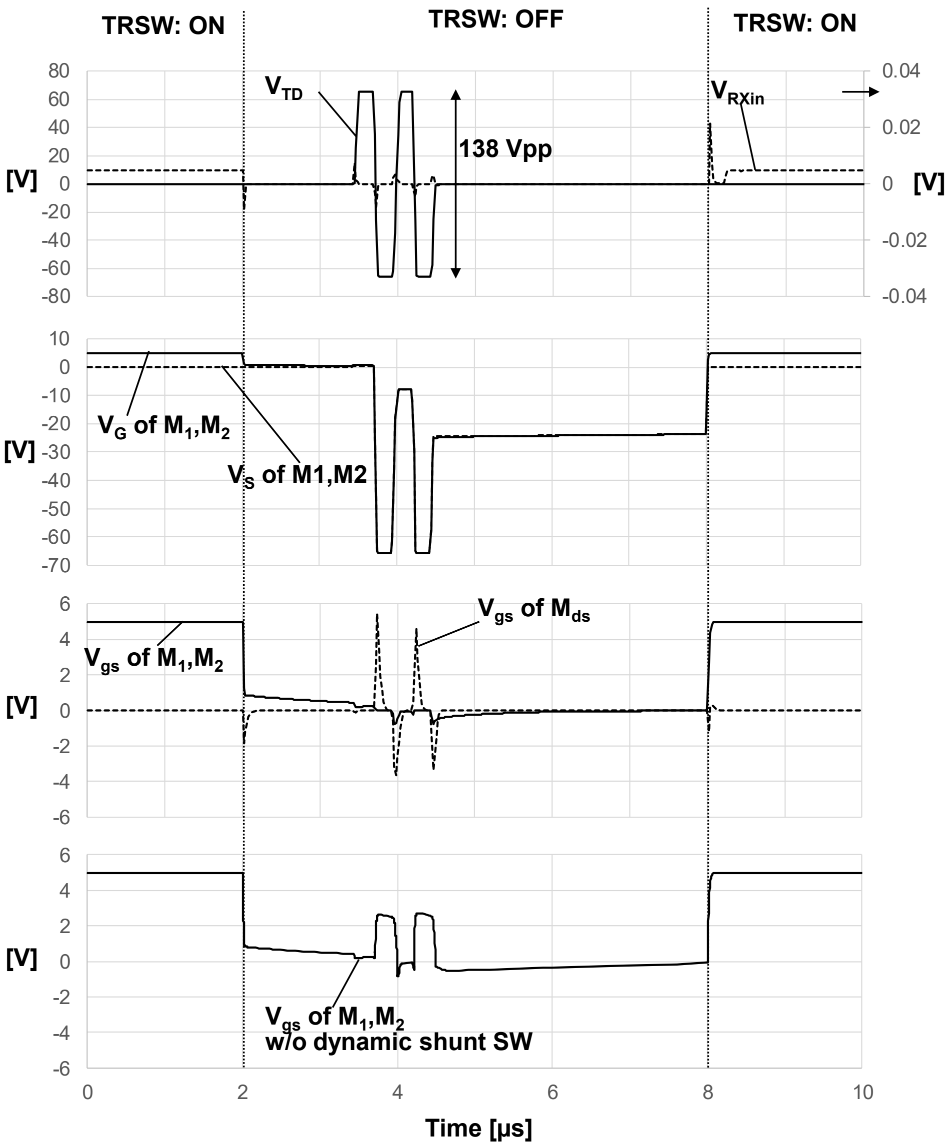


Figure 4.6 Simulated waveforms of the proposed TRSW with dynamic gate-source shunt switch.

We now describe a theoretical analysis of the RC network of the dynamic shunt SW. The dynamic shunt SW should follow the falling edge of the TX pulse, but should not interfere with the turn-on of the TRSW during the transition from TX to RX. In other words, the dynamic shunt SW should follow the source swing of the HV-NMOS M_1 and M_2, but not the gate swing. The transfer function from V_G to V_{gs} of M_{DS} (V_{gsDS}) in Figure 4.5 is expressed as follows, assuming V_S is floating.

$$\frac{V_{gs_{DS}}}{V_G} = \frac{R_1}{R_1 + \frac{C_1 + C_2}{j\omega C_1 C_2}} \tag{4.1}$$

This is the behavior of the M_{DS} with respect to the change in V_G in the transition from TX to RX. The cutoff frequency f_{cG} of this high-pass characteristic, in response to V_G swing, is expressed as follows.

$$f_{c_G} = \frac{C_1 + C_2}{2\pi C_1 C_2 R_1} \tag{4.2}$$

Similarly, the transfer function from V_S to V_{gsDS} is expressed as follows, assuming that V_G is floating

$$\frac{V_{gs_{DS}}}{V_S} = \frac{1}{1 + \frac{1}{j\omega C_2 R_2}} \tag{4.3}$$

The cutoff frequency fcS of the high-pass characteristic, in response to V_S swing, is given by equation (4.4).

$$f_{c_S} = \frac{1}{2\pi C_2 R_2} \tag{4.4}$$

Thus, the cutoff frequency for V_G and V_S swing can be chosen independently. In this design, V_G rises over 50 ns during the transition from TX to RX, which is roughly equivalent to < 7 MHz. In order for the dynamic shunt SW not to interfere with the turn-on, fcG >> 7 MHz in equation (4.2) must be chosen. On the other hand, the fall time of the V_S brought by the TX pulse is < 30 ns, which roughly corresponds to a frequency of > 12 MHz, and in order to follow this frequency, f_{cS} < 12 MHz in equation (4.4) must be chosen. By determining the RC values to simultaneously satisfy the conditions of f_{cG} >> 7 MHz and f_{cS} < 12 MHz, the dynamic shunt SW can follow the slew rate of the TX pulse without disturbing the turn-on. Even if the RC values vary, f_{cG} and f_{cS} can be determined independently under the condition of $f_{cG} > f_{cS}$. This design freedom ensures a design window under RC variability. In fact, we need to choose the design variables with parasitic capacitance in mind.

4.2.3 Source Driven On/Off Control

One of the most critical issues in implementing a TRSW with three HV-MOSs is to realize an on/off control unit using a single HV-MOS. As already described, since the TRSW is off in the state during TX periods due to the dynamic shunt SW, it is necessary to pull the gate up when turning on the TRSW with a single HV-PMOS. However, a PMOS can usually only charge, but not discharge. Therefore, we have made this possible by driving the source of the HV-PMOS, as shown in M_3 of Figure 4.5, so that both charging and discharging can be accomplished using a single HV-PMOS with its gate grounded. The red dotted line in Figure 4.5 is the V_G charge current path and the static current path during RX periods when the TRSW is turned on. On the other hand, the blue dotted line is the V_G discharge current path when the TRSW is turned off. When driving the HV-PMOS source, it is not possible to transfer 0 V, but it is possible to transfer down to about 1 V, which is the Vth of HV-PMOS |Vthp|. Note that HV-LDMOS has high drain-source breakdown voltage, whereas it has a low gate-source breakdown voltage, similar to LV-MOS. Therefore, if an NMOS is used as the HV-MOS for on/off control, the applied V_{gs} cannot be limited to 5 V or less, thus making the use of a PMOS inevitable.

The TRSW turns from on to off at 2 μs in Figure 4.6, at which time the V_{gs} of M_1 and M_2 is pulled down to around a |Vthp| of 1 V, indicating that HV-NMOS M_1 and M_2 are almost turned off. From hereafter, the R_{leak} 2 MΩ resistor in Figure 4.5 reduces the V_{gs} of

M_1 and M_2 to 0 V. Thus, we are able to control on/off using a single source-driven HV-PMOS.

4.3 TX/RX Switching Noise Suppression

Suppression of switching noise during the transition from TX to RX is one of the challenges. To obtain an ultrasound image, a series of TX and RX must form a single beam. This single beam is raster scanned in two or three dimensions. When TRSW is switched from off to on during the switching from TX to RX, a spike-type switching noise voltage is generated at the TD node due to parasitic C_{gd} coupling in M_1, as shown in Figure 4.7(a). This switching noise is converted into undesired sound by the TD and propagates into the body, generating artifacts in the image.

If a countermeasure circuit to reduce switching noise is added to the TD side of the TRSW, it must be configured with extra HV-MOS, which increases the area. Therefore, it is necessary to apply the countermeasure on the output side of the TRSW, which is the LV region. Here, we propose a simple method for suppressing switching noise by fully digital control of the TD node's impedance from the LV-domain side, without the need for additional analog circuits. In the proposed digital impedance control sequence shown in Figure 4.7(b), we simply leave the 5-V NMOS M_g in Figure 4.7(a) on for a certain period after the transition to RX until the V_G rises and settles, and then turn M_g off after the preset delay time. M_g is originally intended to improve the off-isolation by turning it on during the TX period. When the TX to RX transition, the V_G of M_1 and M_2 rises from 0 V to 5 V. The behavior of the voltage V_{TD} at the TD node is similar for delays of 0 (without proposed sequence) and 200 ns (with proposed sequence) until the V_{gs} of M_1 and M_2 exceeds V_{th}, which is approximately 1 V. When the V_{gs} of M_1 and M_2 exceeds V_{th}, M_1 and M_2 begin to turn on, and the series impedance of M_1, M_2, and M_g suppresses the crosstalk suffered at the V_{TD} node from the V_G. When the V_G goes up to 5 V and settles, the M_g is turned off and ready for RX. The delay can be implemented by using an ordinary digital counter. This simple full digital control effectively suppresses the switching noise.

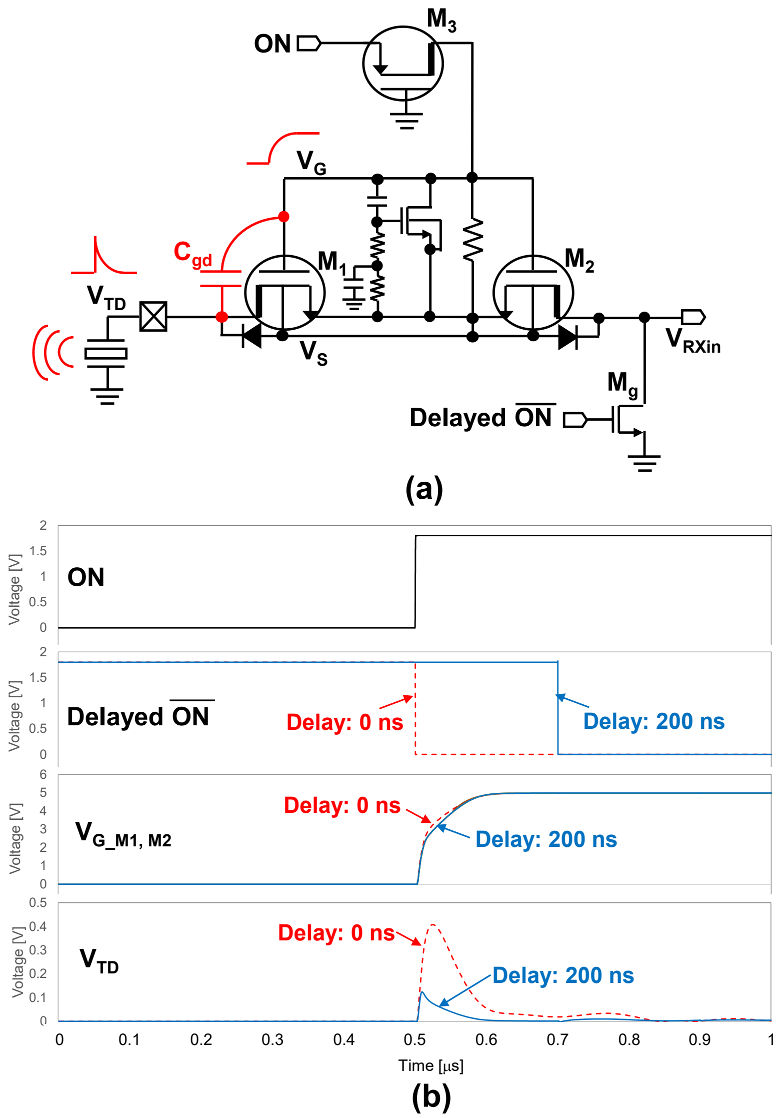


Figure 4.7 (a) Origin of TX to RX switching noise.(b) TX to RX switching noise suppression using the proposed digital impedance control sequence.

4.4 Per-channel Self-Loopback AC Tests

The 2-D array IC has 3072 pads, on which solder bumps are placed and reflowed to connect each transceiver and TD electrically via embedded leads in acoustic backing material. It is not practical to probe the 3072 pads during wafer testing, so we need to perform an AC conduction test by looping the signal back from the TX pulser to the RX internally, using the TRSW as an attenuator. An overview of the loopback test system for wafer testing is shown in Figure 4.8(a). We do not have to probe the 3072 pads, but instead probe only 128 RX output pads, which are SCh output pads where the 24-ECh DAS results are output. Since a tester's pin electronics module usually mounts only a limited number of channels that can sample analog signals, and the signal being looped back is a square wave, the ASIC output signal is handled as a digital signal. The tester's digital pin electronics module receives a loop-backed output signal and compares it with the output high logic level (VOH) and output low logic level (VOL) by setting up a strobe (STRB). The 2-D array IC switches the ECh under testing, and the tester can screen defective ECh by judging the conduction of the AC signal ECh-by-ECh.

We can apply the loopback test not only for wafer tests but also AC conduction tests after probe assembly and field probe diagnostics, as shown in Figure 4.8(b). The 128 RX output signals from the 2-D array IC to the main instrument unit through the flexible printed circuits (FPCs) and cables are amplified, anti-alias filtered by an AFE, and then converted to digital by an ADC. The main instrument unit tests the AC function of the probe by determining whether the amplitude of the sampled signal is above a certain criterion.

Figure 4.9 shows a schematic of the TRSW for the proposed loopback test. The basic idea is to attenuate the signal from the TX pulser during loopback by turning M_1 and M_2 half-on instead of fully on, and also turning M_g on. This enables dividing the signal by the on-resistance of the series of M_1 and M_2 and that of M_g. By inserting a series of diode-connected 5-V NMOSs on the source side of M_3 to lower the V_G, the on-resistance of M_1 and M_2 becomes higher than that of the RX mode. This also avoids the breakdown voltage violation of the V_{gs} of M_1 and M_2 because of the lowered V_{gs} even if the common source V_S is pulled down by negative voltage transmission.

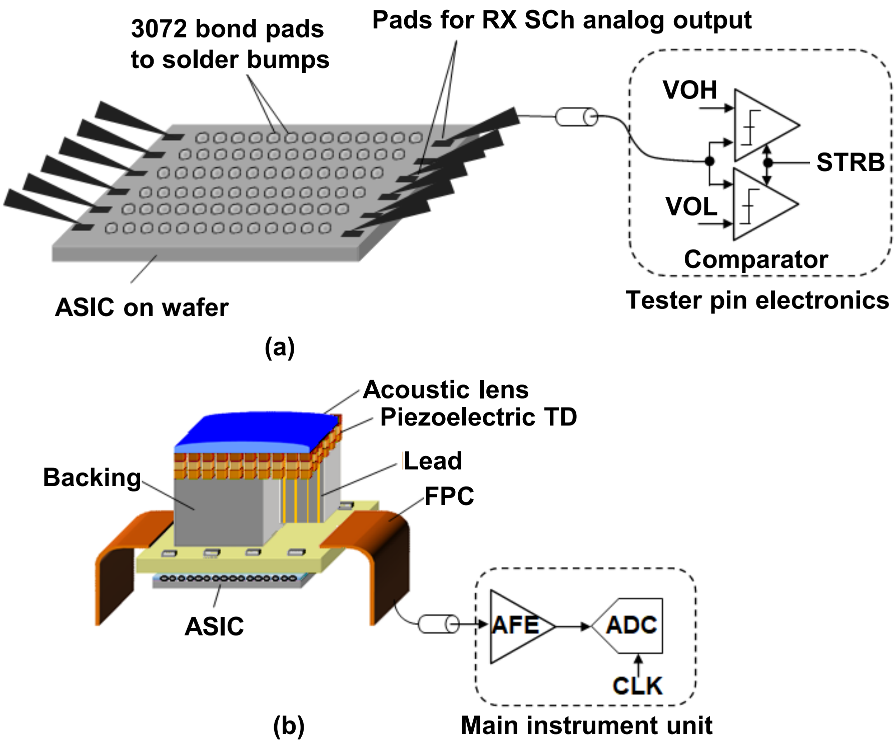


Figure 4.8 AC loopback testing system overview. (a) wafer testing. (b) matrix probe testing after assembly.

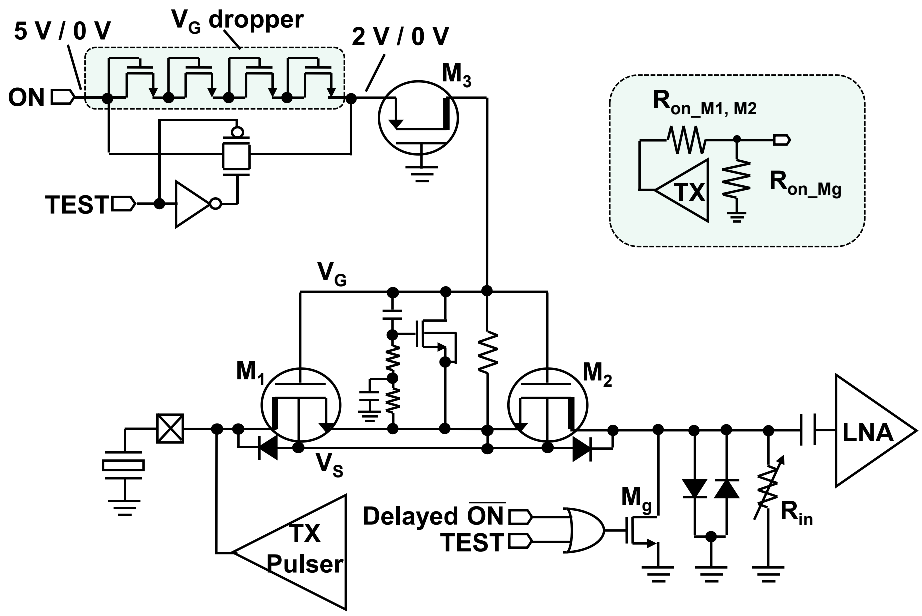


Figure 4.9 Schematic of the proposed TRSW capable of working as an attenuator for TX to RX self-loopback test.

Figure 4.10 shows simulated internal waveforms during a continuous wave loopback test with TD and cable loads, assuming a post-assembly test of a probe. The +HV and -HV supplies are regulated to +5 V and -5 V, respectively. An amplitude of 5.2 Vpp at the TD node is attenuated to 0.28 Vpp by the TRSW and then amplified by the LNA. The LNA output has a kickback of 40 MSample/s from a later stage of the BDR-SCD, which falls outside the RX signal bandwidth (up to 5 MHz). The loopback square-wave signal is delayed through the BDR-SCD and converted from differential to single-ended. In the addition of 24-EChs, only a single ECh is activated and the other 23-EChs in the same SCh do not contribute to the signal summation. Accordingly, the SCh output is obtained at almost 0 dB through the CDADD. The added output signal is divided by the CBUF output impedance and the AFE input impedance, and an amplitude of 0.21 Vpp is obtained at the main instrument unit input. In this test, the signal source is a TX pulser, and the TX pulser generates only a square wave signal, so we cannot perform analog linearity tests. However, the loopback AC function test can contribute to the reliability and cost reduction of the probe in terms of detecting and screening defective EChs prior to the probe assembly.

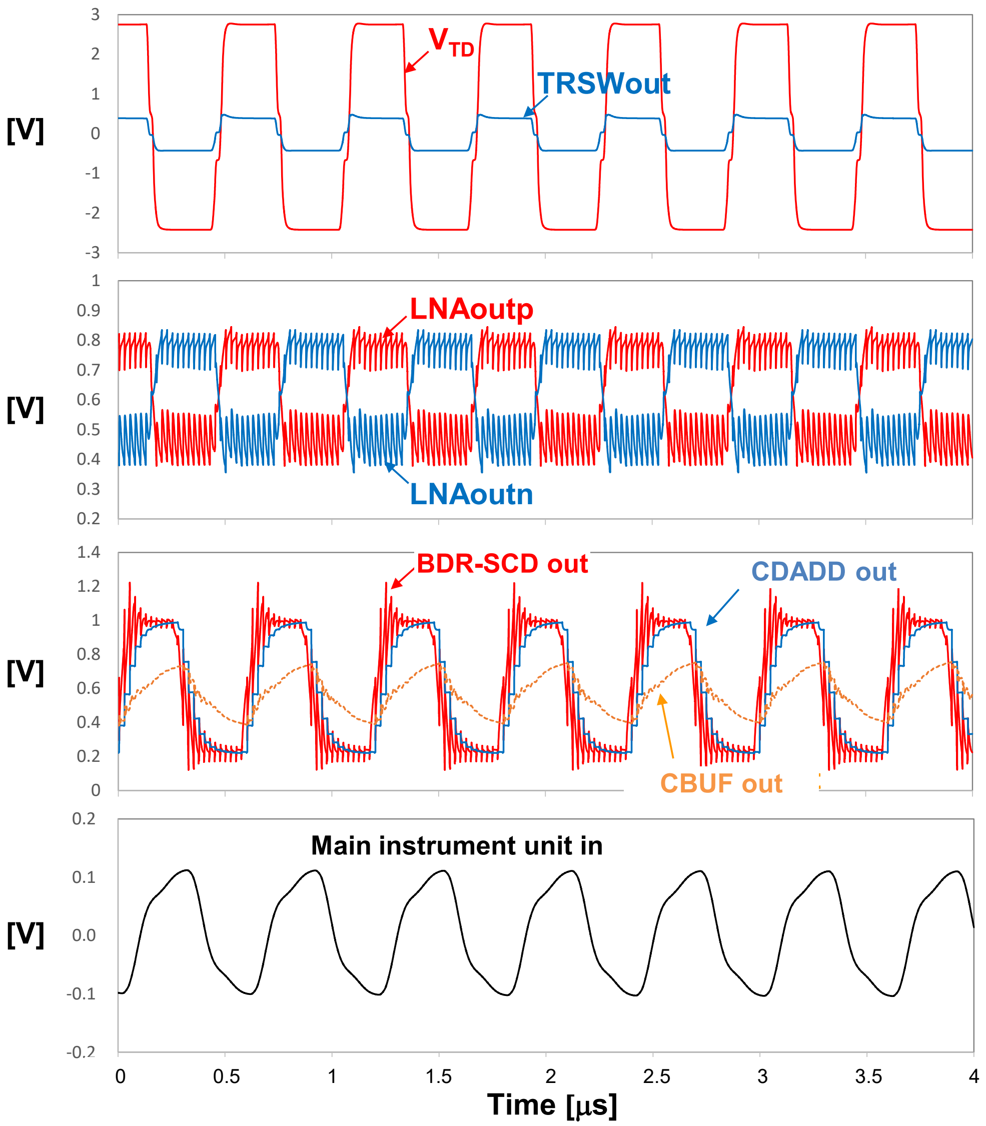


Figure 4.10 Simulated waveforms at each stage in the TX to RX CW loopback test.

4.5 Evaluation

A 2-D array IC with 3072 channels of transceiver was fabricated using 180-nm 140 V HV SOI CMOS technology. Figure 4.11 (a) is a die photograph of the full chip, (b) is a enlarged view of the SCh containing 24 EChs, and (c) is a enlarged view of a single ECh.

The TRSW occupies 11 % of the 0.3 mm square area of a single ECh.

Figure 4.12 is a pie chart showing the area breakdown of the proposed TRSW, with HV-MOSs dominating 70 % of the total TRSW area. This means that minimizing the number of HV-MOS is a reasonable strategy to minimize the area of the TRSW. The total area of the dynamic shunt SW, including RC and gate-to-source 2 MΩ leakage resistor, accounts for only 2.9 % of the total area of the TRSW.

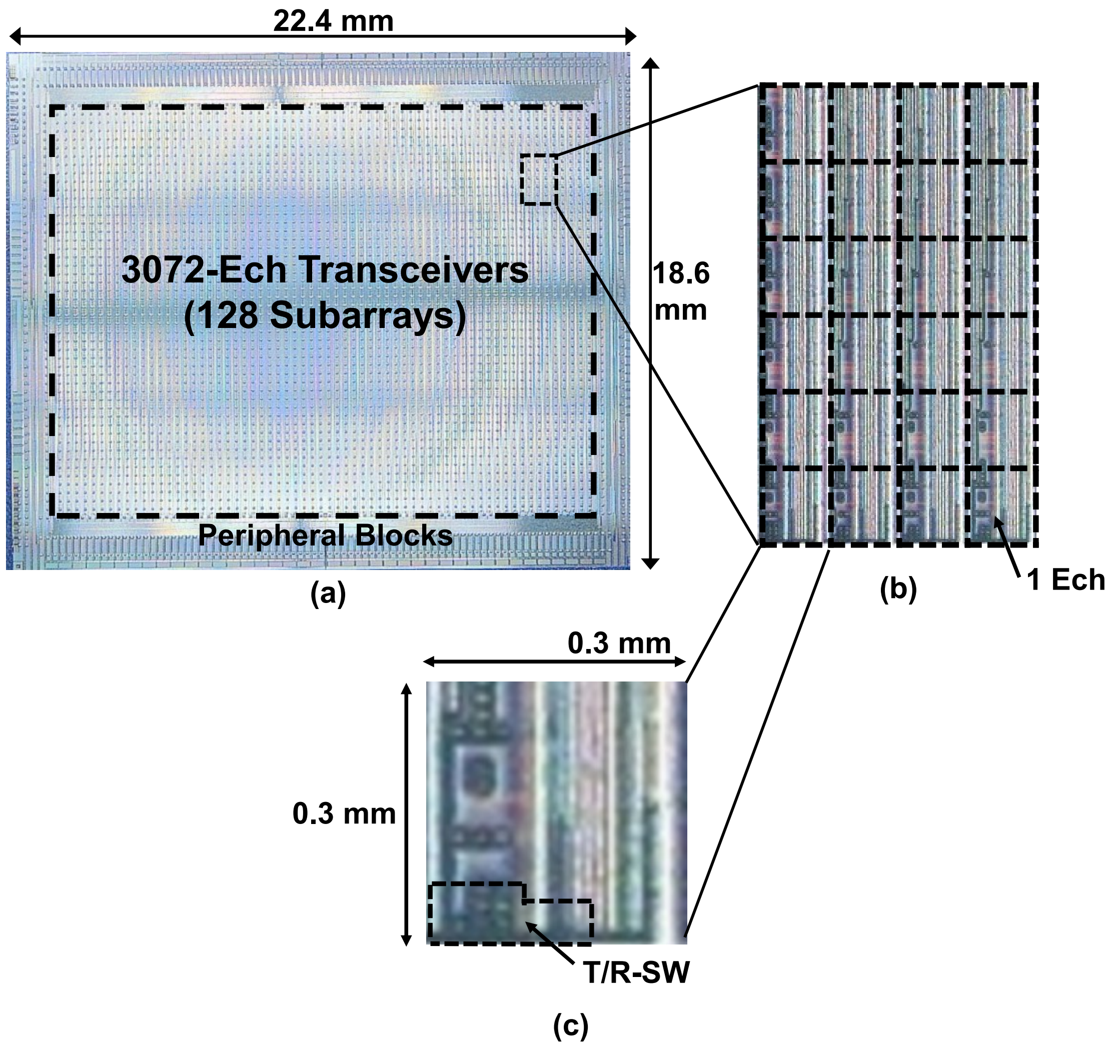


Figure 4.11 (a) Photograph of ASIC, (b) sub-array including 24 ECh's, and (c) single ECh.

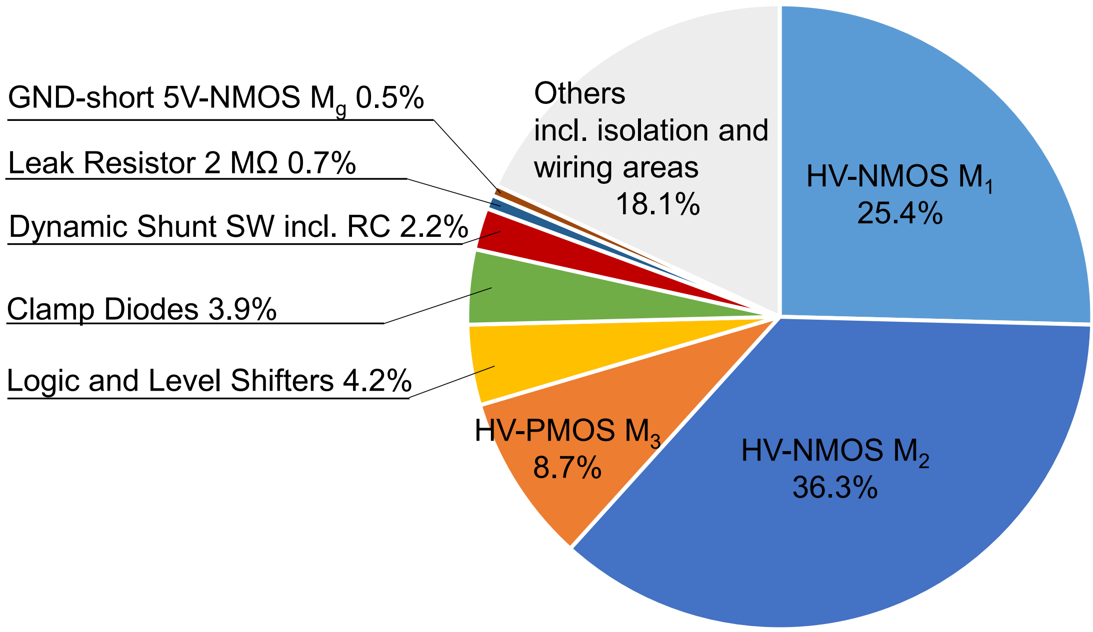


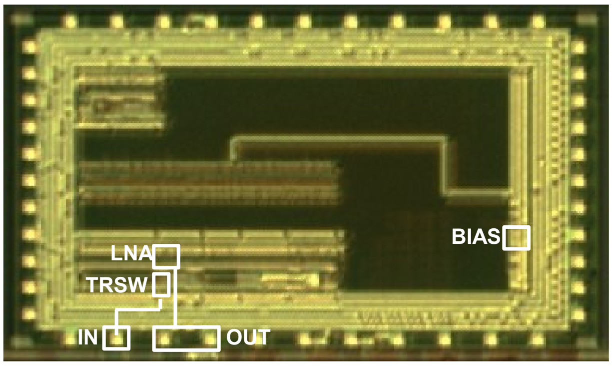
Figure 4.12 Area breakdown of the proposed TRSW.

4.5.1 Electrical Evaluation

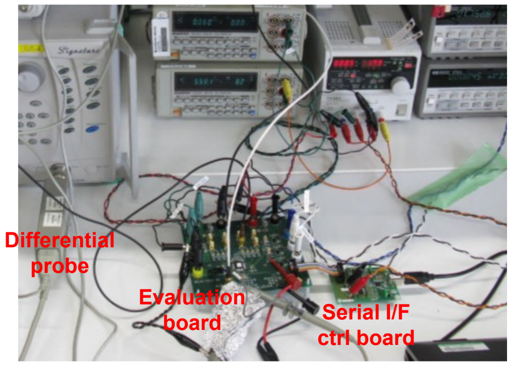
To facilitate the electrical evaluation of the TRSW alone, a test element group (TEG) comprising the TRSW and LNA was prepared [76], and its basic characteristics were evaluated using the TEG. A chip photograph of the TEG is shown in Figure 4.13 (a) and the electrical evaluation system for the TEG is shown in (b). In this system, a network analyzer and a sampling oscilloscope were used to observe the LNA's differential output, buffered by a source follower, using a 1 MΩ-input differential active probe (Agilent 1141A).

Figure 4.14 shows the measured transfer characteristics of the TRSW + LNA. The LNA was active while the TRSW was off, and the off-isolation of the TRSW alone was determined from the ratio of the TRSW's off and on characteristics. The measured off-isolation of -64 dB at 10 MHz was sufficient to attenuate a 138 Vpp pulse with a rise and fall time of 20 ns to less than 1.8 Vpp. Since there are bi-directional clamping diodes at the LNA input, as shown in Figures 4.5 and 4.9, abnormal large-signal echoes during the RX period are clamped by the diode's forward voltage.

TX to RX switching noise was measured electrically and acoustically. Electrical evaluation was performed using a TEG equipped with a TRSW and LNA. Acoustic evaluation was performed by placing the assembled probe on a phantom or in water and generating ultrasound pulses. First, Figure 4.15 displays the electrically evaluated TX-to-RX switching noise waveforms. During the fabrication process of the TD, the bulk piezoelectric material was diced and separated into 3072 channels. Therefore, it was not practical to cut off only one channel of the TD and attach it to the TRSW input. For this reason, the electrical waveforms were measured with a 7-pF input capacitance of the active probe as a load, rather than the TD load, allowing the active probe to contact the TRSW input using a 100 MSample/s oscilloscope. The waveform measured without digital impedance control corresponds to the case of a delay of 0 ns in Figure 4.7, and the waveform measured with digital impedance control corresponds to the case of 200 ns. It was confirmed that the proposed simple control sequence reduced the 388 mV noise peak to 89 mV.



(a)



(b)

Figure 4.13 (a) Chip photograph of TEG, including TRSW and LNA.
(b) Electrical experimental setup.

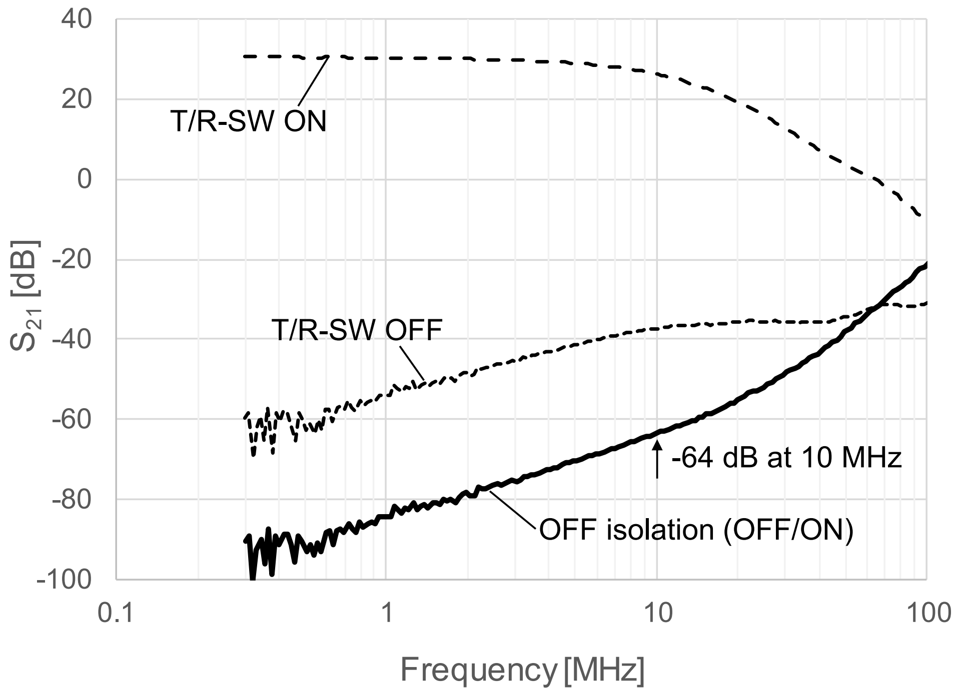


Figure 4.14 Measured transfer and isolation characteristics of TRSW + LNA TEG.

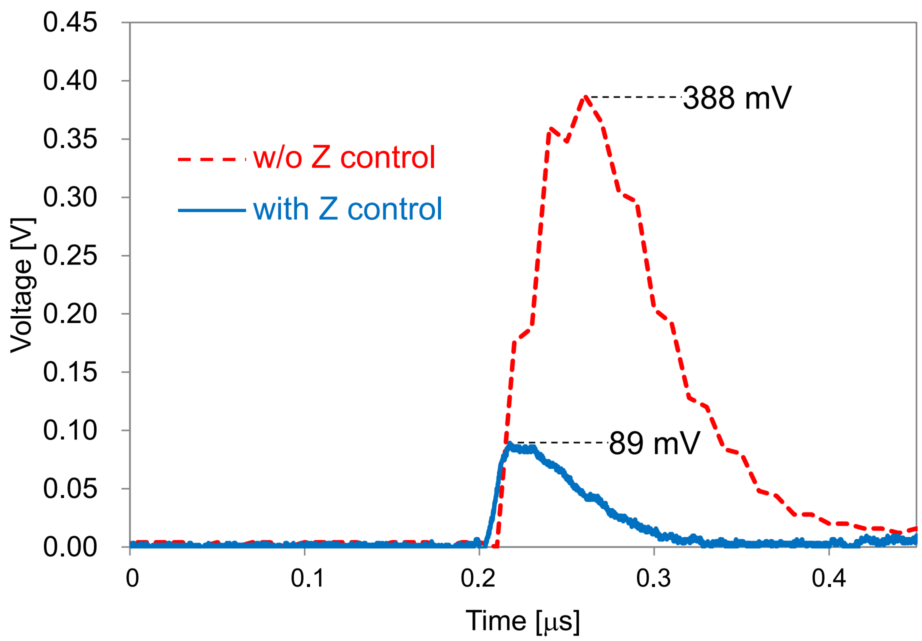


Figure 4.15 Measured TX to RX electric switching noise waveforms with and without digital impedance control sequence.

4.5.2 Acoustic and Imaging Evaluation

Next, we discuss the results for acoustic TX-to-RX switching noise. The acoustic measurement setup is shown in Figure 4.16. First, in the measurement setup shown in Figure 4.16(a), an assembled probe was introduced into water, and only TX-to-RX switching was performed without pulse transmission. The hydrophone directly received acoustic switching noise to measure waveforms. In addition, to observe the impact of switching noise under conditions similar to B-mode imaging of a living body, the artifacts caused by the switching noise were visualized by performing only TX-to-RX switching without pulse transmission with the probe contacting a phantom as shown in Figure 4.16(b). We also acquired images of switching noise artifacts in water by using Figure 4.16(c) setup that is the same as in Figure 4.16(a), except that a hydrophone is not used. The setup in Figure 4.16(c) is for a worst-case measurement because the attenuation of ultrasound waves in water is less than that in phantoms. The switching noise is totally reflected by the metal base under the hydrophone and is received by the probe without attenuation.

Figure 4.17(a) displays the acoustic switching noise waveforms obtained using the setup depicted in Figure 4.16(a). The dotted red line represents the waveform without the proposed digital impedance control, which was measured with M_g always off, as shown in Figure 4.7(a). The blue waveform with the control is the result of M_g being turned off after a delay of 200 ns as shown in Figure 4.7(b). The FFT spectra of Figure 4.17(a) waveforms are shown in Figure 4.17(b). Since the switching noise is in the form of an impulse, it has power over a broad bandwidth. As shown by the arrow in Figure 4.17(b), the proposed digital impedance control achieves an 18.1 dB reduction in acoustic switching noise.

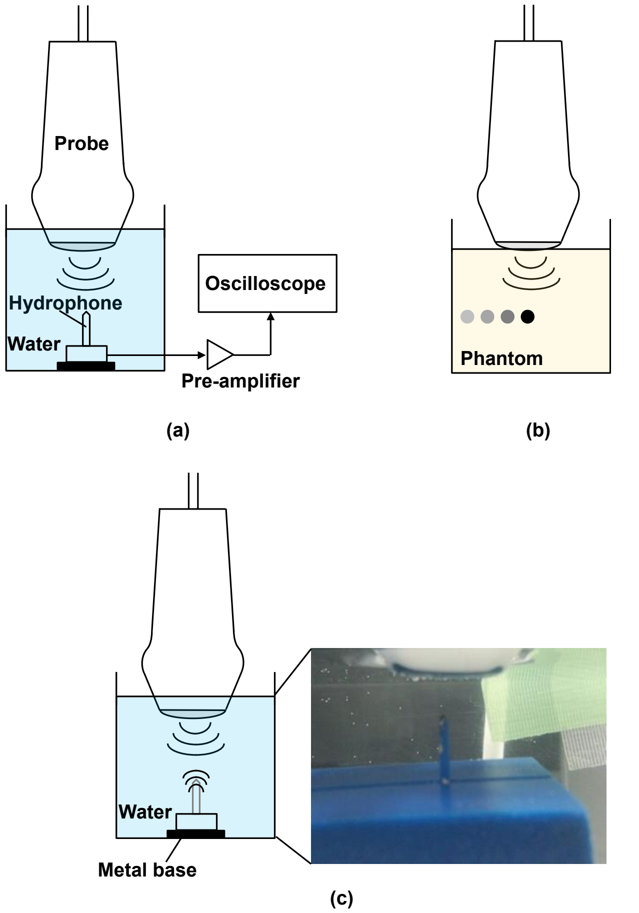
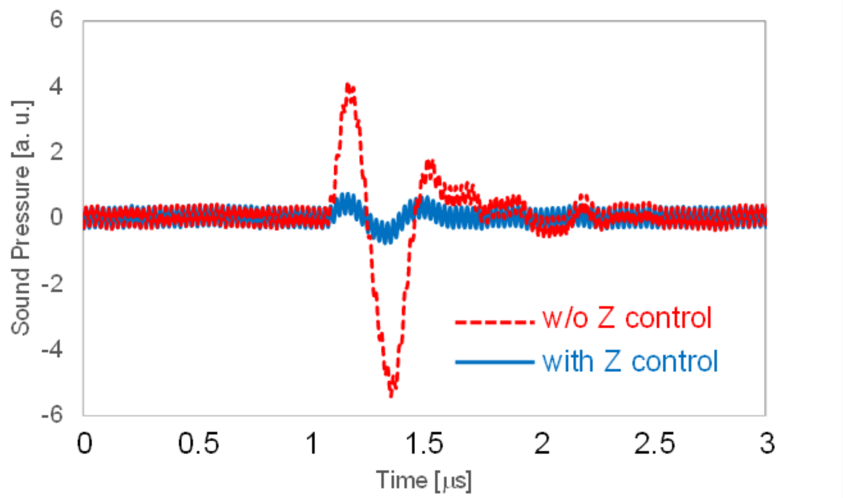
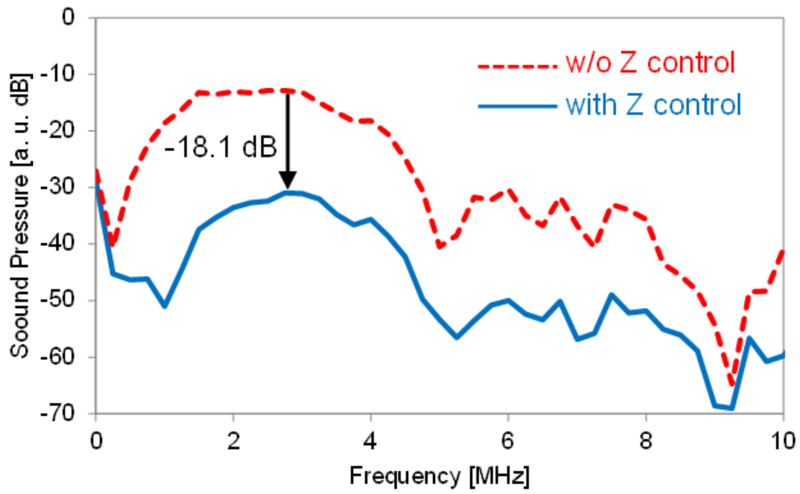


Figure 4.16 (a) Acoustic experimental setup for TX to RX switching noise measurement. (b) Imaging of TX to RX switching noise artifacts using US phantom. (c) Imaging of TX to RX switching noise artifacts in water.



(a)



(b)

Figure 4.17 (a) Measured acoustic TX to RX switching noise waveforms with and without digital impedance control sequence. switching noise spectra with and without digital impedance control sequence.

Figure 4.18(a), (b), (c), and (d) are B-mode images acquired with the setup in Figure 4.16(b) using the phantom. Figure 4.18(e) and (f) are B-mode images with the setup in Figure 4.16(c) in water. Since we have taken images without pulse transmission, only performed TX-to-RX switching, artifacts caused by TX-to-RX switching noise were vizualized. Figure 4.18(a) and (b) are switching-noise-artifact images displayed at a normal B-mode gain that can be changed offline after imaging. Since both (a) without and (b) with the proposed impedance control were completely black, with no impact of switching noise observed, we obtained (c) and (d) by increasing the B-mode gain by +27 dB to the maximum configuration. Background noise due to thermal noise was brightened by increasing the B-mode gain. However, there was still no difference between (c) and (d) with or without the proposed impedance control.

The images with the maximum B-mode gain acquired in water are (e) and (f). In case (f) with the proposed impedance control, the white horizontal lines near the center were significantly weaker than in case (e) without the impedance control. Since all the channels were TX-to-RX switched simultaneously, the switching noise was unfocused and always propagated downward as a plane wave. Therefore, the switching noise artifacts appeared and flowed laterally near the center, regardless of the direction of RX focus steering. Thus, the B-mode images demonstrate that the proposed digital impedance control sequence effectively reduces the effect of TX to RX switching noise artifacts, even though the difference can only be observed in imaging with water, which has less ultrasound attenuation.

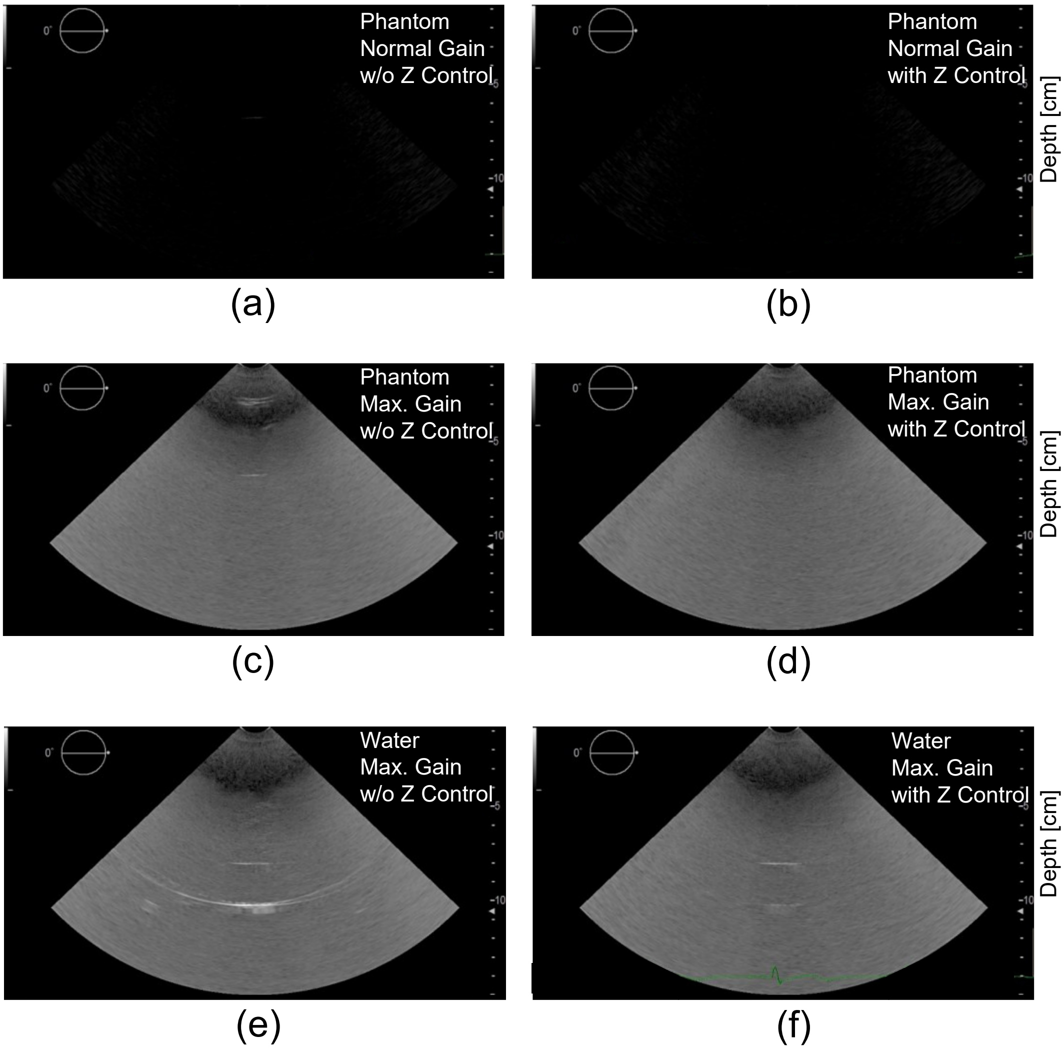


Figure 4.18 Measured TX to RX switching noise artifacts in B-mode images using a phantom and a hydrophone on a metal base in water under different display brightness gain setup.

(a) Image taken using the phantom with normal gain without Z control.

(b) Image taken using the phantom with normal gain with Z control.

(c) Image taken using the phantom with maximum gain without Z control.

(d) Image taken using the phantom with maximum gain with Z control.

(e) Image taken in water with maximum gain without Z control.

(f) Image taken in water with maximum gain with Z control.

4.5.3 Loopback Test Evaluation

Finally, we discuss the measurement results of the per-channel AC loopback test. To sample the loopback output from the 2-D array IC as an analog signal, we assembled the probe head module shown in Figure 4.8(b) and obtained waveforms with an oscilloscope by probing the SCh output of the module. The 1.67 MHz CW signal generated by the on-chip logic was looped back internally from TX to RX. The HV supply of TX was set to +5 V and -5 V, which is the lowest operable voltage for the TX pulser. By switching the active ECh one by one and observing the SCh output, the output amplitude spatial distribution of Figure 4.19(a) was obtained. This map can be represented as a histogram, as shown in Figure 4.19(b). Figure 4.19(c) is the observed CW output signal waveform. Through the RX signal path, the upper limit of signal amplitude is limited by the maximum voltage that the LNA output can swing. Therefore, the variation in amplitude shown in Figure 4.19(a) and (b) represents the variation in the LNA output for the overall chip. Since all ECh outputs are summed in an SCh using DAS μBF and finally bundled into a single beam by the RX DBF in the main instrument unit, random spatial variations are not a problem. However, location-dependent skew and discontinuous steps may degrade the image. The observed histogram followed a nearly normal distribution, and there were no significant skew or steps in the spatial distribution that could compromise image quality. Thus, the per-ECh AC loopback test function is also very useful in terms of identifying trends in variability.

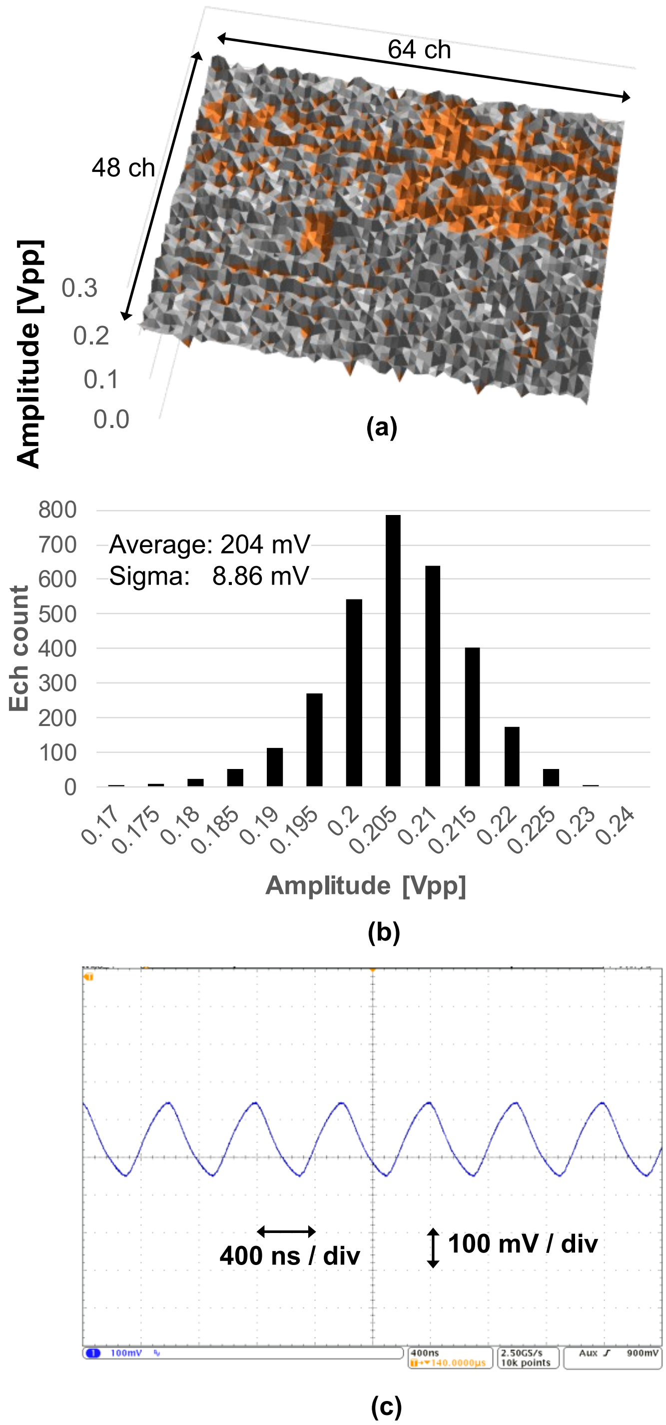


Figure 4.19 (a) Measured spatial distribution map of ac loopback output amplitude. (b) Amplitude histogram over 3072 EChs. (c) Measured CW loopback output waveform.

At the end of this section, this study is summarized in Table 4.1, comparing it to state-of-the-art designs. For a fair comparison, a plot of the tradeoff between maximum TX pulse amplitude allowed by the TRSW and TRSW area is also shown in Figure 4.20. Increasing the drain-source breakdown voltage of an HV-MOS requires a longer drift region between the drain and gate, increasing the area of the HV-MOS device. Thus, there is an inherent trade-off between TX pulse amplitude and TRSW area. Although the area of our TRSW is larger than that of reference [73], it is favorable in the tradeoff between pulse voltage and area, indicating that an architecture that minimizes the number of HV-MOSs is effective.

The dynamic shunt architecture proposed in this research has enabled the world's first implementation of a TRSW that accepts bipolar pulses with only three HV-MOSs without sharing control circuits among multiple EChs. This circuit implementation enables integration of 3072 EChs on a single chip in a 300 μm square area, with power dissipation of 0 μW for TX and 12.1 μW for RX, enabling 3-D imaging with natural air cooling of the probe.

Table 4.1 T/R switch and HV switch comparison

	This work	ISPSD2016 [64]	Elec. Lett.2014 [73]	Trans. US.2018 [67]	ESSCIRC2018 [69]
Architecture	Dynamic shunt	Zener bias	Level shift	Level shift	Floating latch
Number of EChs	3072	16	1	64	512
HV transfer	No	Yes	No	Yes	Yes
Number of HV-MOSs/ECh	3	12	17	≥ 5	5
Supply	5 V	12 V	-25V, 1.8V	±20 V, 3.3 V	-
Area (μm^2)	9920	-	5525	48320	70312
Ron (Ω)	290	18	-	180	-
OFF isolation	-64 dB@10 MHz	-54 dB@5 MHz	-53 dB	-35 dB@10 MHz	-
Static power/ECh	0 μW (TX) 12.1 μW (RX)	4.4 mW	0 mW	-	-
Technology	180-nm 140 V HV SOI CMOS	150 V HV SOI CMOS	180-nm 50 V HV CMOS	350-nm 50 V HV CMOS	LV + 200 V HV-CMOS

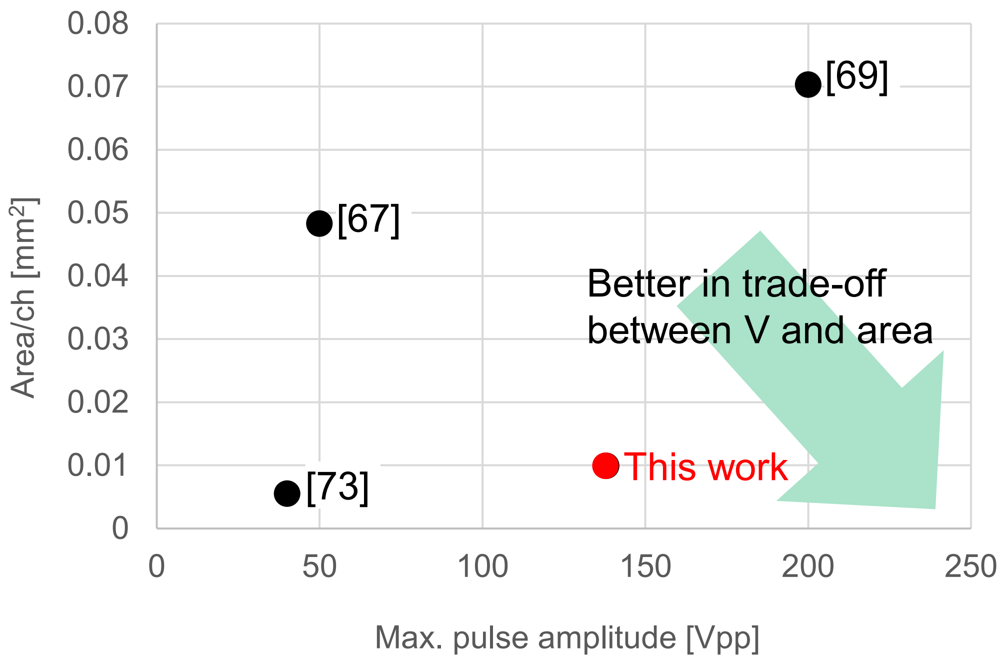


Figure 4.20 Trade-off between the maximum pulse amplitude and the TRSW area.

4.6 Conclusions

In Chapter 4, we proposed an area- and power-efficient TRSW for a 3072-channel 2-D array IC used in ultrasound 3-D/4-D imaging. The proposed TRSW utilizes an LV dynamic shunt switch that guarantees an off state during the TX period without requiring static power or extra HV-MOS. The source-driven HV-PMOS for on/off control enables both charging and discharging with only a single HV-PMOS, which also contributes to area reduction. Thus, the proposed TRSW requires only three HV-MOSs per ECh without sharing circuits among EChs, and consumes zero µW at TX and 12.1 µW at RX. We also demonstrate that the proposed simple digital impedance control sequence can reduce the TX-to-RX switching noise by 18.1 dB. The proposed sequence is shown to be effective in reducing artifacts in underwater B-mode images. Finally, the TX-to-RX internal loopback AC conduction test function for each ECh, made possible by the implementation of the TRSW attenuation mode, allowed for the provisioning of spatial distribution maps of the CW loopback output amplitude without directly probing 3072 electrodes.

Chapter 5
Continuous-Time Pulse Compressor

5.1 Background

In this thesis, Chapters 3 and 4 discuss the reduction of circuit area and power dissipation in a 2-D array IC. Additionally, this chapter describes signal processing techniques that further enhance image performance at the system level. Specifically, to achieve penetration of ultrasound signals, i.e., to ensure the signal level from deep regions of the human body while maintaining spatial resolution of images, we applied the pulse compression (PC) technique used in radar and other applications to ultrasound imaging. Further, the proposed technique has also been oriented for low power dissipation. We verified the effectiveness of this technique through electrical measurements, acoustic measurements, and image evaluation. This technique can be applied not only to matrix probes but also to conventional 1-D probes to improve performance. Since 2-D array ICs in probes have power dissipation limitations determined by heat generation, mounting the pulse compressor on the main instrument unit side, where power dissipation limitations are less restrictive, can indirectly increase system performance without increasing the power of the 2-D ICs in the probes.

The signal enhancement resulting from PC allows the same level of RX signal to be obtained even if the TX voltage is lowered. This not only improves performance but also contributes to circuit area reduction by replacing the HV-MOSs used in the TX pulser and TRSW with MOS devices of lower breakdown voltage. The lower TX voltage can also lead to lower power operation by reducing the dynamic power involved with charging and discharging of TD loads and parasitic capacitance in the TX pulsar circuit.

In terms of application, wireless handheld probes for point of care (POC) have recently emerged, leveraging advanced electronics technology to perform examinations near the patient rather than in the exam room [77], [78], [79], [80], [81]. Use cases for diagnostic imaging devices range from mature healthcare in developed countries to extensive healthcare in developing countries, and from laboratories to home healthcare. Although the performance of handheld probes has not yet reached a level of image quality suitable for routine examinations or advanced diagnostics, the application of PC techniques described in this chapter is expected to improve image performance with a minimal power penalty. In addition, the matrix handheld probes are expected to reduce workflow and examiner skill dependency, enabling non-professional users to quickly manage urination and defecation by monitoring swallowing, bladder, and colon, for example, in elderly care facilities and at home. The lowering of TX voltage and lower power dissipation by applying PC could contribute to the realization of matrix handheld probes.

As a clinical challenge, for example, in the case of a sector probe for cardiology, both penetration and spatial resolution are needed to observe the posterior wall edge of the ventricle. Higher frequency improves axial resolution. However, it also increases acoustic attenuation. Therefore, there is a trade-off between penetration and axial resolution. Increasing the number of cycles of the TX burst pulses can increase the sound pressure. However, in this case, increasing the number of cycles degrades the axial resolution, and this method also suffers from the trade-off between penetration and axial resolution. PC techniques, widely used in radar, can eliminate this tradeoff [82]. Although prior studies have considered its application to ultrasound imaging [83], [84], [85], [86], [87], [88], it has not been widely applied in commercial products due to the narrow bandwidth of TD and physical implementation issues.

One of the key challenges faced by a 2-D array IC in a matrix probe is reducing the circuit area. As discussed, a TX voltage of at least 60 Vpp is typically required to achieve sufficient sound pressure using the piezoelectric effect of ultrasound TDs. Fortunately, 2-D matrix array probes can focus the TX beam not only in the azimuthal direction but also in the elevation direction, thus reducing the TX voltage compared to conventional 1-D array probes. TX electronics described in Chapter 3 and TRSW described in Chapter 4 require area-hungry HV-MOSs [89], [90], [91]. A circuit design that minimizes the number of HV-MOS and a strategy to lower the TX voltage without compromising SNR are needed. Lowering the TX voltage also enables the shortening of the LDMOS channels, thereby increasing current and reducing on-resistance [91]. However, since TX sound pressure is proportional to TX voltage, lowering the TX voltage will lead to signal loss. One promising solution to this problem is the combination of a chirp TX, which increases the average TX power even at low TX voltages, and PC, which maintains the RX peak envelope power and narrow echo pulse width.

The system targeted in this PC study is shown in Figure 5.1. It can enhance the performance of both conventional 1-D probes and matrix probes. Figure 5.1(a) shows a system with a conventional 1-D array probe, where electronics in the cart-type main instrument unit perform TX and RX. The TX electronics transmits a chirp signal instead of burst pulses. The proposed continuous-time pulse compressor (CTPC) is introduced in the main instrument unit to eliminate the trade-off between SNR and axial resolution. Figure 5.1(b) shows a matrix probe connected to a cart-type main instrument unit. Without increasing the power of the 2-D array IC in the matrix probe, PC on the main instrument unit can improve the image performance of the entire system. In both systems, the CTPCs in the main instrument units compress the RX echo to increase the peak signal and narrow the pulse width. Since the proposed CTPC can be implemented using the general components of an antialiasing filter (AAF), it can be implemented in any target system by simply cascading a delay-equalizing all-pass filter (APF) to a passband control low-pass filter (LPF). This configuration enables both AAF and CTPC functions simultaneously with high affinity.

This chapter is organized as follows. Section 5.2 describes the concept of the proposed CTPC and its implementation using discrete OPAs and passive components, compared to a conventional PC operating in the digital domain. In Section 5.3, we present the electrical and acoustic measurement results as well as imaging results using an imaging prototype.

Section 5.4 discusses the implementation of chip integration, and finally, Section 5.5 provides a summary of this chapter.

5.2 Design of Continuous-Time Pulse Compressor

5.2.1 Approximate Linear Delay Equalization

Conventional PC is achieved by transmitting long-duration, frequency- or phase-encoded pulses and matching the RX signal through matched filtering, i.e., cross-correlating the TX reference waveform with the RX signal, as shown in Figure 5.2(a). This technique enables higher pulse peaks and narrower pulse widths through compression, thereby improving axial resolution while transmitting long-duration pulses with low peak power. Conventional PCs use FPGAs or digital signal processor (DSP) logic, incorporating cross-correlators in the discrete-time digital domain. To achieve an effective PC effect, computing devices must perform multi-bit parallel sum-of-products operations with hundreds of filter taps. Performing this in real time requires a significant amount of computing resources [85]. For this reason, some prior art reduces the computational complexity by applying PC to baseband signals rather than RF signals [85], [86].

Surface acoustic wave (SAW) devices are employed in PC, as evident in references [92] and [93]. A SAW dispersion filters extend the pulse and generates a coded chirp signal. This signal is transmitted by a power amplifier (PA). In RX, a SAW correlator compresses the RX signal into a pulse. However, the insertion loss of the SAW filter is as significant as 30 dB [92].

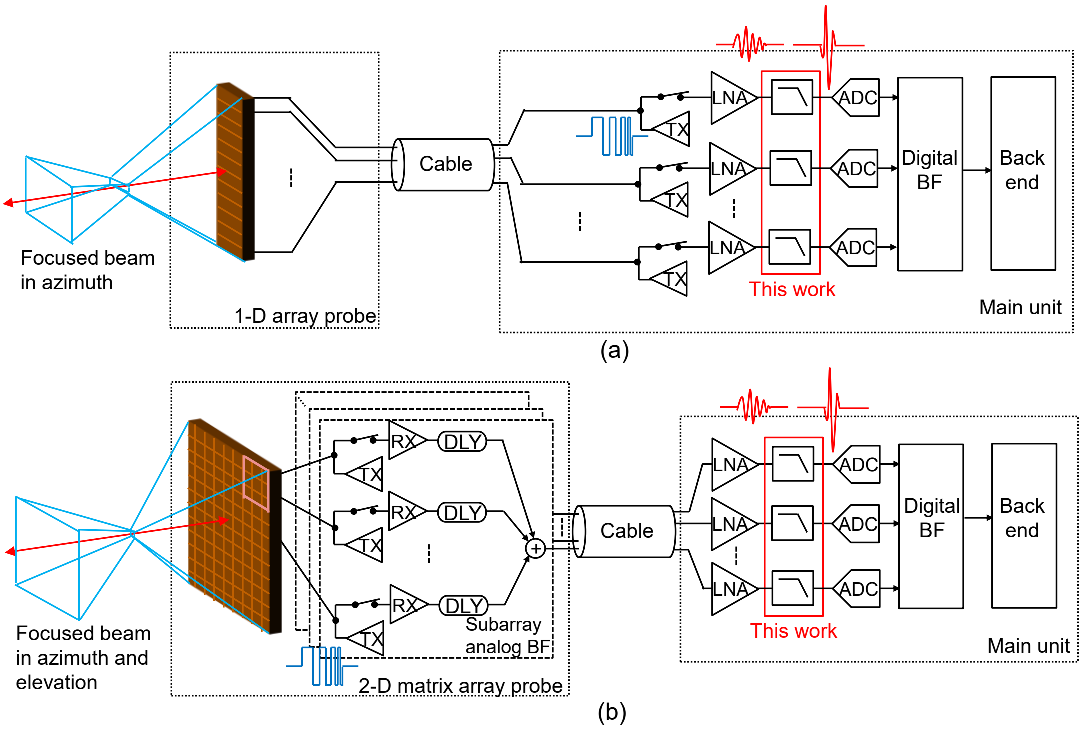


Figure 5.1 Overview of targeted ultrasound imaging systems using the proposed continuous-time pulse compressor. (a) a 1-D array probe connected to a cart-type main instrument unit. (b) a 2-D array matrix probe connected to a cart-type main instrument unit.

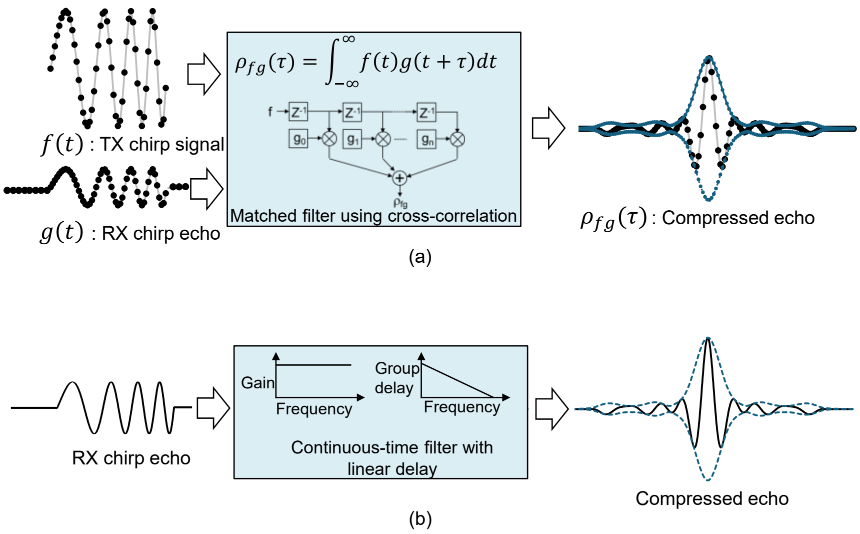


Figure 5.2 Comparison of conventional pulse compression using digital-domain correlator and proposed continuous-time pulse compression.

In this paper, we propose a novel CTPC utilizing a high-order all-pass filter (APF) to address the issues of excessive computing resources in digital domain processing and insertion loss in SAW filter. The proposed CTPC, shown in Figure 5.2(b), directly compresses the frequency-coded chirp signal input by frequency-dependent delay to enhance the RX signal and narrow the pulse width. Since it is difficult to significantly control the group delay (GD) within the bandwidth with an LPF, the proposed CTPC uses APFs. A chirp TX typically requires an HV linear amplifier to amplify arbitrary waveforms from a DAC. However, TX circuits that convert logic signals from the processor directly into high-voltage arbitrary waveforms using HVDACs [94] and pulse-width modulated pulsers that enable chirped TX have been reported [95].

The challenge in implementing CTPC is to achieve a long delay that corresponds to the long chirp period in the ultrasound bandwidth. Another challenge is to linearize the delay with respect to frequency. Therefore, we first use an APF with a relatively high quality factor (Q) to achieve a long delay. Figure 5.3 shows the concept of the proposed CTPC. Here, a bandwidth of 1 MHz to 4 MHz is assumed with a TD centered at 2 MHz. In this bandwidth, for example, a GD of 1.5 μs at 1 MHz is needed to ensure a chirp period of 1.5 μs. As shown in the configuration in Figure 5.3(a) and (e), a GD peak of more than 1 μs is first achieved with the second-order APF#1, which has a high Q of 1.8. However, with only this stage, the GD is not linear with respect to frequency, as shown in the curve of Figure 5.3(e) APF#1, which means that the delay difference from 1 MHz to 4 MHz cannot be utilized efficiently for the chirp signal. Therefore, by cascading APF#2 and APF#3, which have their resonance frequencies arranged at equal intervals while gradually decreasing Q, we perform a delay equalizing that approximates the overall 6th-order GD as a linear function of frequency. In practice, the values of ω and Q for each second-order APF were optimized to minimize the squared error between the actual GD and the desired GD line shown in Figure 5.3(e). As a result, the pole and zero arrangement is as shown in Figure 5.3(b). Since the proposed CTPC is composed of APFs, both poles and zeros are symmetrically arranged. As the frequency increases and the radius increases, the Q value decreases, and the radiation angle becomes larger. Note that low frequencies below 1 MHz are not used for TX, and this work is characterized by ignoring the GD roll-off at lower frequencies to ensure the maximum GD peak. Increasing the order brings the frequency dependence of GD closer to linear. However, it is a trade-off between GD linearity and circuit area or power dissipation. In this work, the approximate linearization of GD was performed within the constraints of a sixth-order APF.

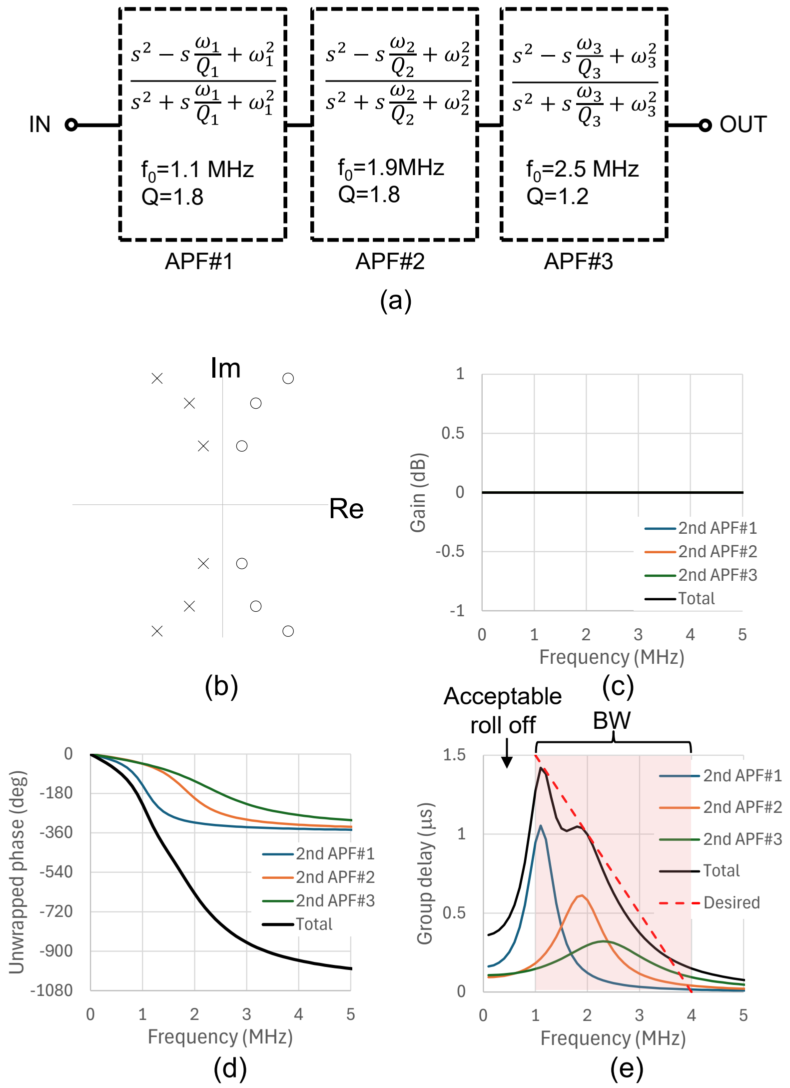


Figure 5.3 Approximate linearization of frequency-dependent delay as a concept for the proposed CTPC: (a) cascaded second-order APFs, (b) poles and zeros arrangement, (c) gain-frequency characteristics, (d) phase-frequency characteristics, and (e) group delay-frequency characteristics.

Although equiripple filters that achieve flat GD characteristics by using high-order APFs [96], [97], and prior works that employ APFs to realize unit delays for BF have been reported [44], [98], [99], [100], limited works have been reported on PC processing in continuous time. Reference [101] describes a method for PC with a seventh-order APF. However, it does not aggressively linearize the GD to frequency. Reference [102] performs pulse expansion rather than compression in an interleaved discrete-time sampling system. If we attempt to perform compression using a similar architecture, we must synchronize the output with a clock having a much higher frequency than that required for Nyquist sampling. Therefore, it is not realistic to apply sampling architecture to PC. An example of a dispersive filter utilizing a high-order APF in the audio band is presented in [103], based on a digital filter. Compared to the prior work, the key feature of our proposed method is that it accepts the GD roll-off outside the low-frequency band and creates a long delay peak with a relatively high-Q APF, while linearizing the GD. We will describe the specific implementation of the proposed CTPC in the next section.

5.2.2 Discrete Implementation with OPA and RC

This section describes the implementation of the proposed CTPC with discrete OPAs. For the implementation of CTPCs on a printed circuit board (PCB) housed in a cart-type main instrument unit, as shown in Figure 5.1, using discrete OPA, resistor (R), and capacitor (C) could be one of the solutions, as the constraints on the mounting area and power dissipation are less strict than those applicable to in-probe ASICs. Figure 5.4 shows a schematic of a lag-lead type second-order APF that can be realized using an OPA and RC as a component of the CTPC. The transfer function, phase, and GD of this circuit are given by the following equations (5.1), (5.2), and (5.3), respectively.

$$H(s) = A \cdot \frac{s^2 - s\dfrac{\omega_0}{Q} + \omega_0^2}{s^2 + s\dfrac{\omega_0}{Q} + \omega_0^2} \tag{5.1}$$

$$\theta(\omega) = -2\, arctan\left\{\frac{1}{Q}\cdot\frac{\frac{\omega}{\omega_0}}{1-\left(\frac{\omega}{\omega_0}\right)^2}\right\} \tag{5.2}$$

$$t_{GD}(\omega) = \frac{2Q}{\omega_0}\cdot\frac{\left(\frac{\omega}{\omega_0}\right)^2+1}{\left(\frac{\omega}{\omega_0}-1\right)^2\left(\frac{\omega}{\omega_0}+1\right)^2 Q^2+\left(\frac{\omega}{\omega_0}\right)^2} \tag{5.3}$$

where the resonant angular frequency ω_0 is expressed in equation (5.4) and Q is expressed in equation (5.5). The GD has a peak at ω_0 that depends on ω_0 and Q.

$$\omega_0 = \frac{1}{\sqrt{C^2R_1R_2}} \tag{5.4}$$

$$Q = \frac{\omega_0 C R_2}{2} = \frac{R_2}{2\sqrt{R_1R_2}} \tag{5.5}$$

The ratio of R_2 to R_3 is fixed to a unique value of 1:4, as shown in equation (5.6).

$$R_3 = Q^2R_1 = \frac{R_2}{4} \tag{5.6}$$

Finally, the voltage gain A is expressed by Equation (5.7). Increasing Q causes R_1 to decrease. Therefore, the gain approaches 0 dB, and decreasing Q causes the gain to decrease.

$$A = \frac{R_3}{R_1+R_3} \tag{5.7}$$

As illustrated in Figure 5.3, by allocating the resonance GD peak frequency of the high-Q APF biquad at approximately 1 MHz, which is the chirp-start frequency, and subsequently adding extra resonance GD peaks with a lower Q, it is possible to achieve a flat gain to frequency and an approximately linearized GD to frequency. Figure 5.5 shows the full schematic of the total eighth-order CTPC, including second-order band-pass filter (BPF). For the commercially available OPA, Analog Devices LTC6254 was selected based on its gain bandwidth product (GBW) of 720 MHz, which met the requirement of more than 40 dB open-loop gain even at 4 MHz, which is the chirp-end frequency. Since the gain of the APF single stage is inevitably less than 0 dB, a preamplifier is placed in the first stage, and the latter three stages constitute a linear GD sixth-order APF. Considering the noise characteristics, the APF biquad with a higher gain was placed in the preceding stage.

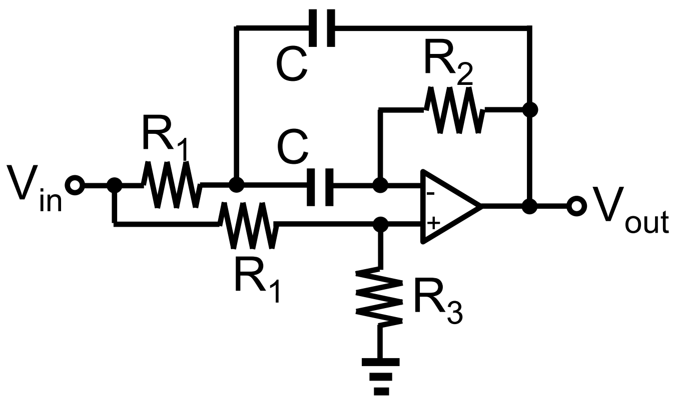


Figure 5.4 Schematic of second-order APF composed of OPA and RC.

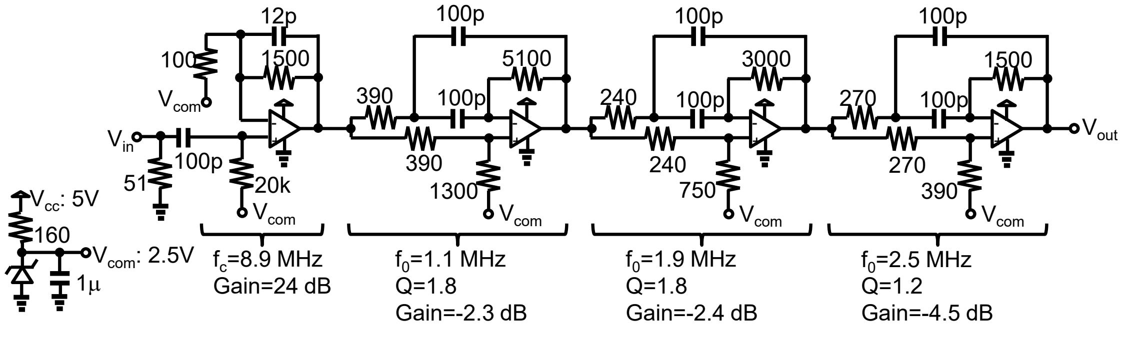


Figure 5.5 Full schematic of the proposed CTPC including a preamplifier, a second-order BPF, and sixth-order APFs with discrete OPA and RC.

5.3 Evaluation

This section presents the electrical measurement results of the CTPC implemented on a PCB using discrete OPAs and RC components. Figure 5.6 shows a photograph of the 16-channel on-board CTPC, the schematic of which is shown in Figure 5.5. Single 5 V is supplied to the OPAs, and a 2.5 V signal common voltage is generated for each channel using the Analog Devices ADR5041 shunt voltage reference. The measured power dissipation is 70 mV/channel.

5.3.1 Electrical Evaluation

The measured AC characteristics are shown in Figure 5.7. Due to the non-ideal characteristics of the OPAs and the deviation from the desired resistance caused by the limitations of the E series of available chip resistors, the gain characteristics show a dip around 1 MHz, where the GD has a peak. The -3 dB bandwidth is up to 8.72 MHz. The GD has almost the expected characteristics, decreasing approximately linearly from 1.66 μs in the range of 1.12 MHz to 4 MHz. The input-referred noise voltage is 16.2 μVrms within the -3 dB bandwidth, and the input-referred noise density is 4.4 nV/√Hz at 2 MHz and 2.7 nV/√Hz at 4 MHz. Using the specifications of commercially available RX AFE ICs for ultrasound imaging as a reference, the noise figure (NF) of the CTPC is 0.7 dB when assuming that the input-referred noise of the LNA is 1 nV/√Hz, the gain is 20 dB, and the noise of the TD is 0.9 nV/√Hz.

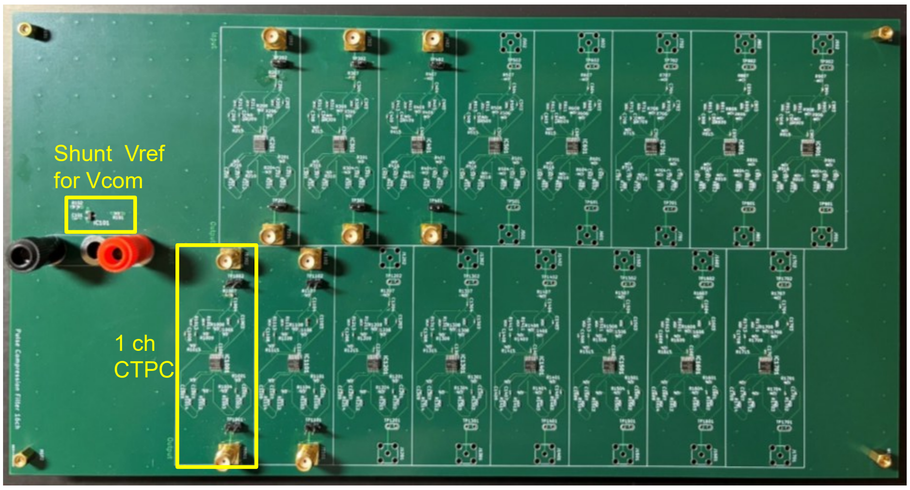


Figure 5.6 Photograph 16-ch CTPC on PCB.

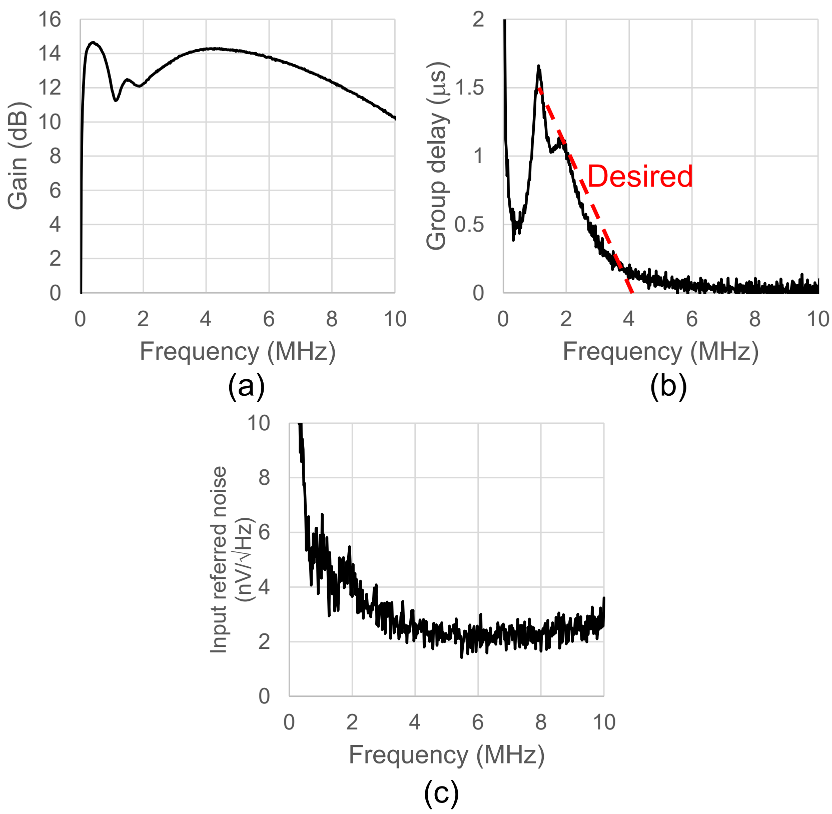


Figure 5.7 Measured AC characteristics: (a) gain, (b) group delay, and (c) input-referred noise voltage.

Figure 5.8 shows the transient response when a linear chirp signal is input with a frequency sweep from 1 MHz to 4 MHz in 1.5 μs. As shown in Figure 5.8(a), the chirp signal is compressed in the time domain to produce a narrow pulse as expected. In Figure 5.8(b), the input signal is the sum of two linear chirp signals that last for 1.5 μs and are shifted by 0.75 μs. Even though the chirp periods overlap, the CTPC can separate the two pulses and output them.

Figure 5.9 shows the measured large-signal characteristics of the CTPC. Figure 5.9(a) shows the relationship between the peak-to-peak input and output signals when a linear chirp signal of 1 MHz to 4 MHz in 1.5 μs is input to the CTPC and when a 2 MHz CW is input. The larger peak-to-peak output amplitude when a chirp signal is input, compared with CW input, is due to signal enhancement through compression, and the peak-to-peak signal is enhanced by 6.7 dB in this way.

The fundamental tone, second harmonic, and third harmonic for a 2 MHz CW input are shown in Figure 5.9(b). The proposed CTPC has a frequency characteristic in which the GD changes drastically within the bandwidth, and this also affects the behavior of distortion. Therefore, the growth of harmonics in response to increased input differs from that of commonly used circuits. For this reason, the harmonics in Figure 5.9(b) do not follow a straight line up to an input of -20 dBV. The 1-dB gain compression point (1dBGCP) is -17.3 dBV, and the third-order input intercept point (IIP3) is -8.3 dBV.

As described above, we have discussed the electrical characteristics of the proposed CTPC. It is possible to input the ideal chirp signal in an electrical setup. However, when performing acoustic measurements using an actual TD, the TD bandwidth and nonlinear propagation in the medium affect the signal in complex ways. The following section describes the results of the acoustic measurements.

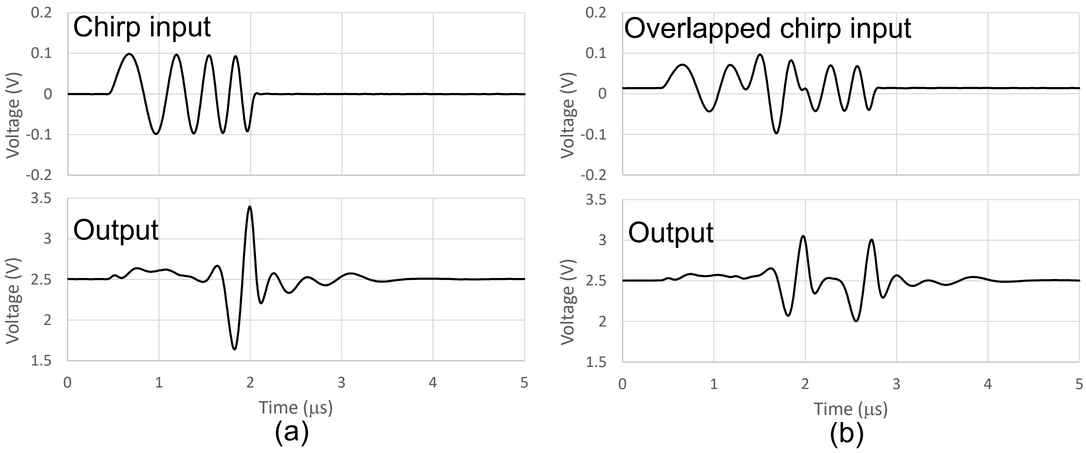


Figure 5.8 Measured waveforms: (a) response to linear chirp signal from 1 MHz to 4 MHz in 1.5 μs, (b) pulse separation response to overlapped linear chirp signals with 0.75 μs shift.

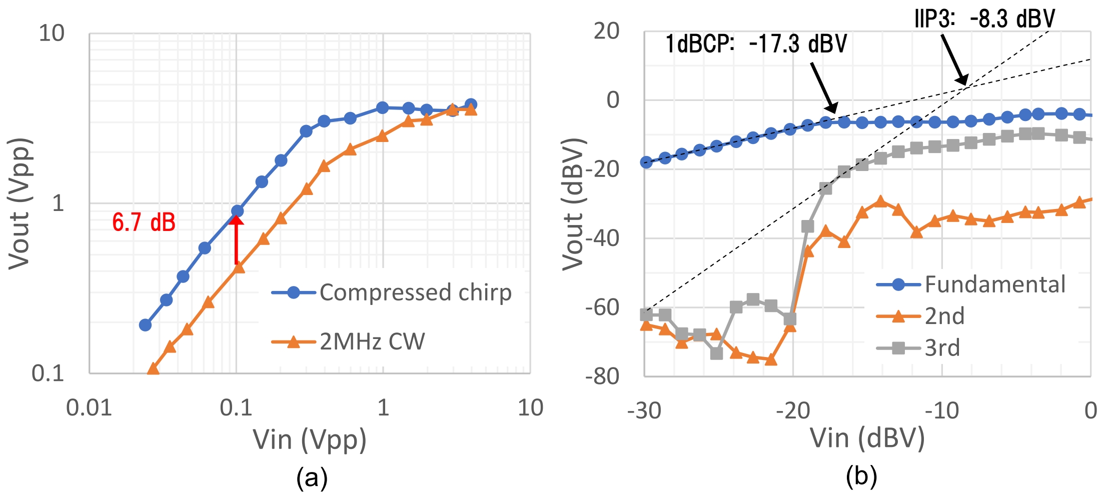
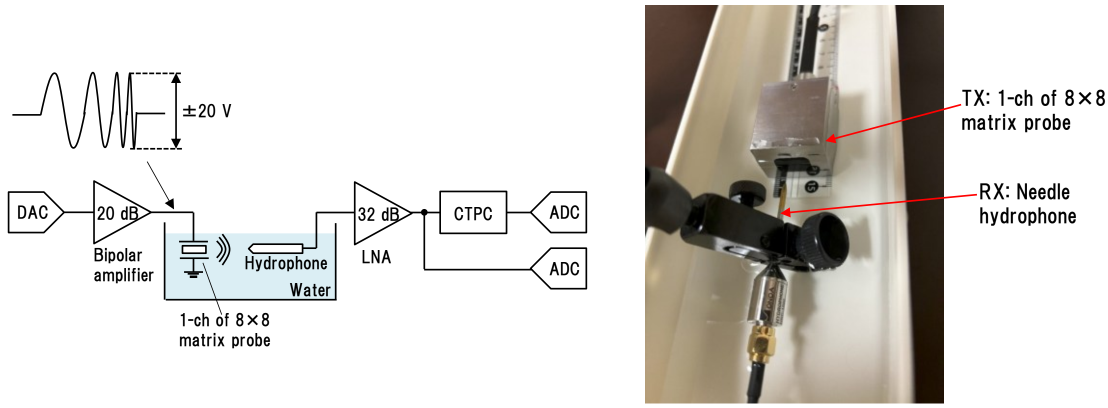


Figure 5.9 Measured large-signal characteristics: (a) input vs output peak-to-peak voltage for 1 MHz to 4 MHz linear chirp signal input and 2 MHz CW input, (b) measured input vs output characteristics for fundamental, second-harmonic, and third-harmonic for 2 MHz CW input.

5.3.2 Acoustic and Imaging Evaluation

In this acoustic experiment, we converted the voltage Achirp signal into sound pressure using a custom-made ultrasound probe. Then, we converted the sound pressure chirp signal into an electrical waveform and evaluated the compression effect using the CTPC. For the experiment, we used a piezoelectric matrix probe with a 1.5-meter-long cable featuring 64-channel TDs in an 8 × 8 channel 2-D array, a center frequency of 2 MHz, and a -6 dB fractional bandwidth of 51 % through TX and RX. However, the probe TD bandwidth is narrow for the desired 1 MHz to 4 MHz chirp TX and RX, and the TD bandwidth limits the performance of subsequent measurements. In imaging, the same TDs are used for both TX and RX in time division, however in this acoustic experiment, to alleviate the constraint of the narrow TD bandwidth, we used only one channel TD of the matrix probe for TX and used a needle-type hydrophone with a wide bandwidth (-6 dB fractional bandwidth > 200 %) for RX, and constructed the evaluation system shown in Figure 5.10(a). The total bandwidth of TX and RX is limited by the narrow TX band of a TD in the matrix probe. A 1 MHz to 4 MHz chirp signal is output from the DAC, and then a ±20 V waveform is output from the PA to drive the single-channel TD. The matrix probe and the hydrophone are arranged 10 mm apart in water, facing each other, as shown in Figure 5.10(b). The hydrophone receives the acoustic chirp signal that has directly propagated through the water from the single-channel TD of the matrix probe. The hydrophone output is then amplified by an LNA with a 32 dB gain, and the LNA output is fed into the CTPC. The input/output waveform of the CTPC is sampled, and the compression effect is evaluated.

In the experiments, 2 MHz burst waveforms of 0.5, 1, 1.5, 2, … 3.5, 4 cycles and chirp signals of 1 MHz to 4 MHz with various chirp periods from 1.25 μs to 6 μs were transmitted. Figure 5.11 is an example of a measured waveform when a 1 MHz to 4 MHz in 2.75 μs chirp is transmitted. This waveform plot includes the input waveform to the CTPC, which is a 32 dB amplified hydrophone output signal, the output waveform of the CTPC, and their envelopes. The acoustic signal is amplitude-modulated (AM) as it propagates through the water. As described later, the RX electrical signal is compressed in the time domain, and the peak intensity is enhanced beyond the circuit's gain.



(a) (b)

Figure 5.10 Setup of acoustic experiments to observe pulse propagated from the 1-ch of 8 × 8 channel matrix probe to the needle hydrophone: (a) setup illustration, Me(b) photograph.

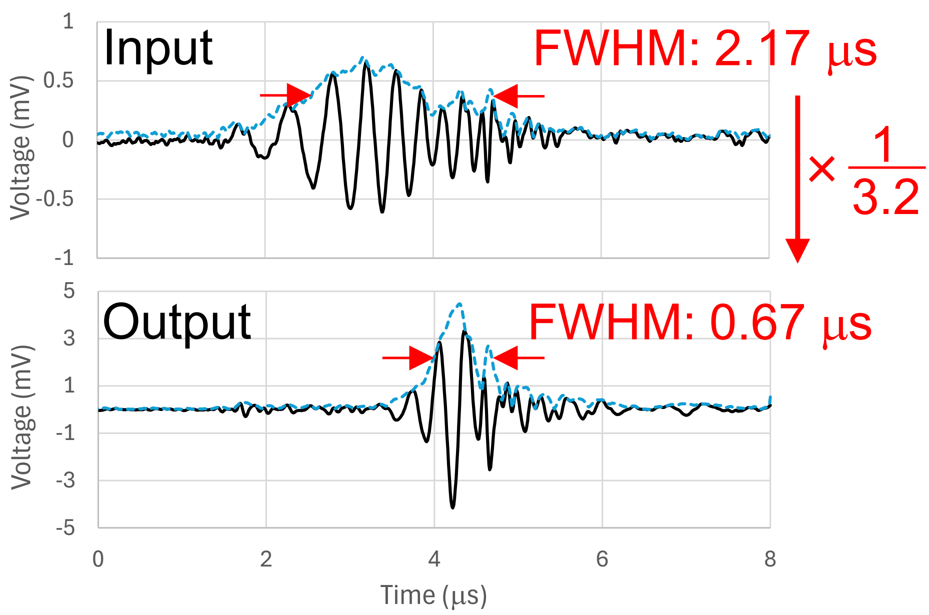


Figure 5.11 Measured CTPC input, output, and envelope waveforms using 1 MHz to 4 MHz in 2.75 μs chirp TX in acoustic measurements.

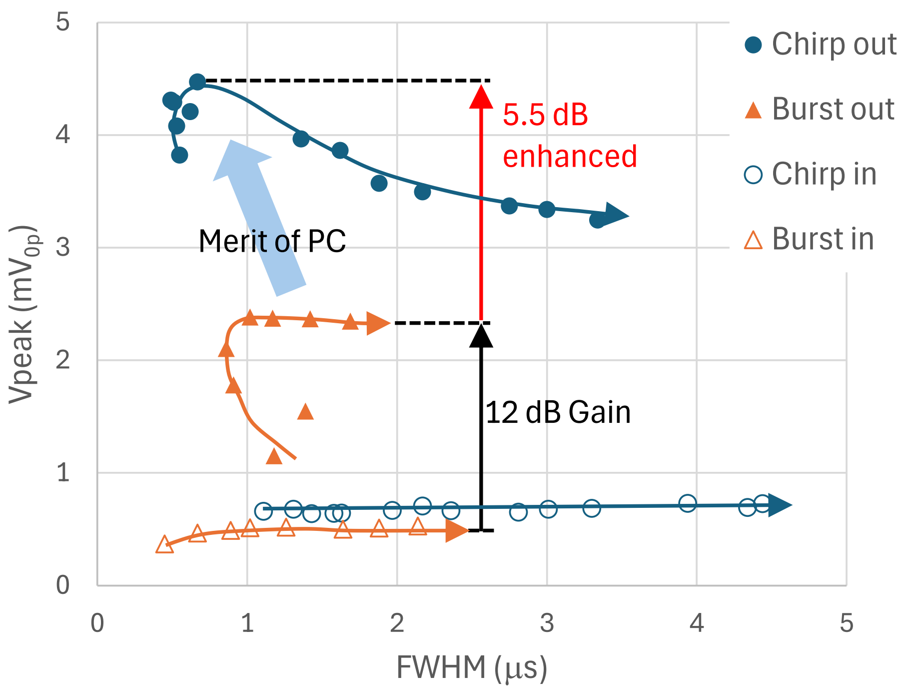


Figure 5.12 Relationship between FWHM and peak voltage of envelopes for 2 MHz burst wave with various cycles and 1 MHz to 4 MHz chirp signal in various chirp periods from 1.25 μs to 6.0 μs in acoustic measurements.

Figure 5.12 shows the effect of the CTPC from a holistic perspective. First, in the case of burst wave TX, the TX sound pressure generally increases as the number of TX burst cycles increases. However, as the number of cycles increases, the time width of the envelope of the RX pulse signal widens; therefore, the axial resolution in the direction of propagation is degraded. In this way, there is a trade-off between signal intensity and axial resolution in burst wave TX. Here, we will evaluate the axial resolution in the propagation direction using the full width at half maximum (FWHM) of signal envelopes. The orange triangles in Figure 5.12 show the relationship between the FWHM of the signal envelope and the CTPC output peak voltage obtained by sweeping the number of cycles during a 2 MHz burst TX. The hollow triangles show the CTPC input, i.e., before compression, and the filled triangles show the CTPC output, i.e., after compression. As shown by the arrowed orange curve along the hollow triangles in Figure 5.12, as the number of cycles increases in the direction of the arrow, the signal peak voltage increases, and the trade-off between signal intensity and axial resolution mentioned earlier becomes apparent. Increasing the number of cycles beyond 2.5 will only increase the FWHM and degrade the axial resolution. The CTPC circuit has a gain of 12 dB at 2 MHz; therefore, when the number of cycles is increased and TX is carried out in a narrow bandwidth around 2 MHz, the CTPC output is 12 dB higher than the input.

In similar measurements, the results for the TX chirp signal swept from 1 MHz to 4 MHz in the period from 1.25 μs to 6.0 μs are also shown in blue in Figure 5.12. The hollow circles represent the CTPC input, and the filled circles represent the CTPC output as well. The blue arrowed curves indicate that the chirp period increases in the direction of the arrows. Here, the signal peak voltage of the burst waveform with a cycle number of 2.5 or more remains almost the same as that of the chirp signal at the CTPC input. However, for the CTPC output, the chirp signal is compressed and then enhanced by up to 5.5 dB compared to the burst signal, which is a merit of the combination of chirp TX and CTPC. In addition, the FWHM of the signal envelope is also 1/3.2 times smaller before and after the compression of the chirp RX signal, as shown in the waveforms in Figure 5.11. Thus, the compression factor, including the characteristics of the TD, can be evaluated as 3.2. In other words, rather than transmitting a signal with a higher number of burst cycles to achieve the desired signal intensity, transmitting a chirp signal and then compressing it using CTPC allows both signal enhancement and improved axial resolution to be achieved. As described above, the effectiveness of the proposed CTPC was observed in acoustic measurements using a single-channel TD and a hydrophone, even though using a narrowband TD.

In this work, a piezoelectric probe with a fractional bandwidth of 51 % limits the compression effect. However, in recent years, broadband TDs using MEMS technology, including CMUT and PMUT, have been developed as described in Chapter 1. We expect that combining these broadband TDs, wideband chirp TX, and the proposed CTPC will provide further signal enhancement and narrow pulses.

Finally, we have demonstrated the merit of the CTPC on sector scan B-mode images using a developed ultrasound imaging prototype. Figure 5.13 introduces the imaging prototype developed using a commercially available TX/RX ASIC and FPGA board. Figure 5.13(a) illustrates the block diagram of the prototype. The 8 × 8 channel 2-D matrix array probe with 2 MHz center frequency, 0.5 mm TD pitch, -6 dB fractional bandwidth of 51 % is used, the same as used in the aforementioned acoustic measurement. Eight Analog Devices MAX14813s were used as TX pulsers, and eight Texas Instruments AFE5812s were used as RX AFE. Both have eight channels, and the former has built-in TX BF logic.

Initial configuration for TX pulsers and RX AFEs, as well as TX delay settings for each sector scan line, is made via serial peripheral interface (SPI) communication from XILINX ZCU102 FPGA board, which is connected to a personal computer. The FPGA receives 62 RX channel data via the low voltage differential signal (LVDS) interface (2 diagonal corner channels out of 64 are assigned to the clock). RX channel data is transferred to the computer via Ethernet. TX/RF BF calculation and signal processing were implemented in the software on the computer using MATLAB. RX signal processing includes RX BF, BPF, TGC, envelope detection, logarithmic compression, and scan conversion to convert from polar to Cartesian coordinates for sector scanning. Note that this prototype is software BF-oriented and specialized for still image acquisition.

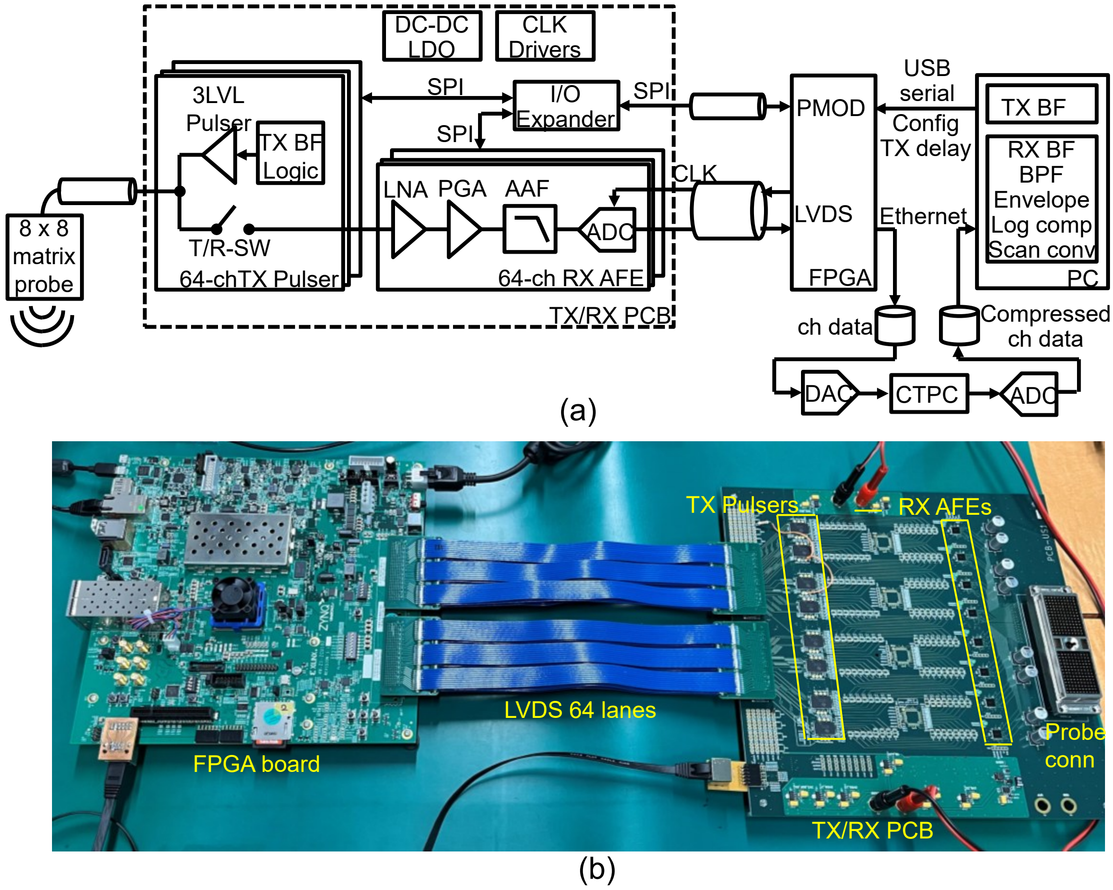


Figure 5.13 Imaging prototype employing commercially available TX/RX ASICs and FPGA for 8 × 8 channel 2-D matrix array probe: (a) block diagram of the prototype, (b) photograph of the prototype PCB.

B-mode image acquisition using chirp TX was performed with the prototype described above. Since the grating lobe angle, determined from the center frequency and TD pitch, is ±32 degrees, sector scanning was performed within this AoV. The TX voltage was ±20 V, and 101 scanning lines were acquired for a frame. Figure 5.14 shows images of the nylon target of the general-purpose ultrasound phantom. Figure 5.14(a) is an image with chirp TX. The waveform is 1 MHz to 4 MHz swept in 3 μs approximated by a 3-level square wave. In practice, due to the limitations of the TX pulser specifications, the TX waveform can only be set up to 8 symbols, and it is not possible to generate a waveform with a long chirp period, such as a slow sweep of frequency over time. Therefore, the desired chirp signal was divided into three sections, and by adding the channel data of the three frames, a signal equivalent to transmitting the desired chirp signal was obtained.

Figure 5.14(b) is the image after compression with the CTPC. Instead of mounting a 64-channel CTPC on the TX/RX PCB, the 62-channel, 101-scan line channel data acquired in Figure 5.14(a) was output from the DAC and input to the CTPC. In this manner, the image shown in Figure 5.14(b) was constructed offline from the data sampled by the ADC from the CTPC output. In both Figure 5.14 (a) and (b), the azimuthal aperture is as small as eight channels; therefore, this constrains the lateral resolution. Consequently, the nylon targets are not imaged as points but are instead blurred laterally. Since the proposed CTPC is effective in terms of axial resolution in the depth direction, the profile of Figure 5.14 (b) after compression shows a single object with a reduction of multiple artifacts along the depth direction for each nylon target, compared to Figure 5.14(a). Figure 5.14(c) and (d) are enlarged views of the nylon target at a depth of 20 mm in Figure 5.14(a) and (b), respectively. Comparing these enlarged images, it can be seen that the multiple artifacts in the depth direction have been reduced, and the signal has been compressed. In conclusion, we demonstrated the compression merit of CTPC in sector-scanned B-mode images, even though we used narrow-band TDs.

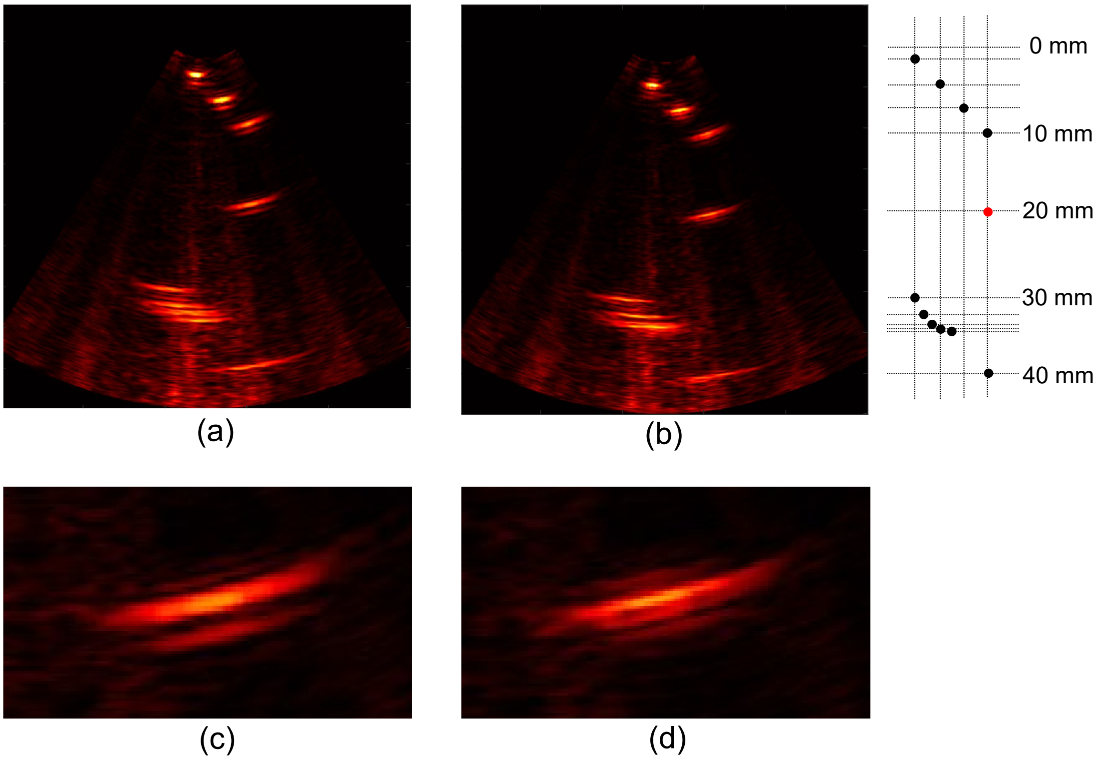


Figure 5.14 Uncompressed and compressed B-mode sector scan images of the nylon wire targets obtained using the imaging prototype and a multi-purpose phantom: (a) uncompressed image, (b) compressed image, (c)(d) enlarged images of nylon targets at a depth of 20 mm for (a) and (b) respectively.

At the end of this section, we summarize this study in Table 5.1 by comparing it to prior art. Since a few prior studies have performed PC in the analog domain and in continuous time, Table 5.1 also includes prior studies on pulse expansion. These are all GHz-band applications, including ultra-wideband (UWB) [105], [107], and optical communications [106]. These studies employ APF-based implementations, which combine BPFs and active dispersive delay lines (DDLs), as well as chirped electromagnetic bandgap (EBG) structures in microstrip lines and passive optical fibers with wavelength-dependent delay. All of them have achieved frequency-dependent delays.

Since the targeted band of prior works differs from this work, the maximum delay × bandwidth and the compression factor or the expansion factor, which is the ratio of the pulse width before and after compression or expansion, are evaluation metrics for comparison. The advantage of this work over prior works is that it can be implemented using commercially available OPA devices without using any special device structures. Furthermore, the APF biquad, with a relatively high Q of 1.8, is used to peak the GD, achieving a long delay with relatively small circuit resources. This allows us to achieve relatively significant maximum delay × bandwidth and a large compression factor. Thus, we have successfully implemented a practical CTPC in the ultrasound band using a simple circuit configuration and confirmed its effectiveness through electrical evaluation, acoustic experiments, and B-mode imaging using sector scans.

Table 5.1 Continuous-time pulse compressor/expander comparison

	This work	TCAS2018 [101]	MTT2012 [104]	MTT2007 [105]	TCAS2005 [106]	RWS2008 [107]
Function	Compression	Expansion Compression	Expansion	Expansion	Expansion	Compression
Technology	Discrete	130 nm	130 nm	Discrete	Discrete	Discrete
Carrier	Chirp TX	Not required	Chirp carrier	Chirp carrier	Chirp carrier	Chirp carrier
Architecture	Cascaded APF	Ladder APF	BPF + Dispersive delay line	Chirped electromagnetic-bandgap (microstrip)	Passive optical filter	Chirped electromagnetic-bandgap (microstrip)
Bandwidth	3 MHz	0.87 GHz	1 GHz	8 GHz	4 GHz	1.5 GHz
Max. delay	1.66 us	2.83 ns	2 ns	5 ns	-	3 ns
Max. delay × BW	5.0	2.47	2	40	-	4.5
Compression factor	3.2 (Acoustic mesurement)	1.7	-	-	-	2.8
Expansion factor factor	-	1.8	2	5	1.5	-

5.4 Study on Chip Integration

5.4.1 Integrated Implementation with gm-C Integrator

In the previous sections, we demonstrated the concepts of the onboard CTPC with discrete OPA and RC. From here on, we will discuss implementation strategies for chip integration. When integrating CTPC into a chip, using OPA requires sufficiently low output impedance for the closed-loop configuration. Furthermore, choosing area-allowable on-chip capacitance requires using high resistance in the range of tens of kΩ to 100 kΩ for the desired RC constants. Thus, this is affected by the parasitic capacitance of the resistors. In contrast, implementation using transconductor-capacitor (gm-C) integrators allows for the design of high-resistance gm outputs. In addition, all capacitors can be grounded in gm-C, which suppresses the effects of parasitic capacitance. Furthermore, circuit characteristics can be easily calibrated by adjusting the bias current of gm.

This section investigates the implementation of the gm-C-based CTPC using TSMC 180-nm RF technology. In the CTPC configuration with the cascade connection of second-order APFs, we have several options for the APF implementation [108], [109]. The topology shown in Figure 5.15 [109] enables stable operating points and achieves arbitrary Q. The transfer function for this topology is expressed by equation (5.8).

$$H(s) = \frac{s^2 - s\frac{\omega_0}{Q} + \omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} = \frac{s^2 - s\frac{gm}{C_2} + \frac{gm^2}{C_1C_2}}{s^2 + s\frac{gm}{C_2} + \frac{gm^2}{C_1C_2}} \tag{5.8}$$

The resonance angular frequency ω_0 is given by equation (5.9).

$$\omega_0 = \sqrt{\frac{gm^2}{C_1C_2}} \tag{5.9}$$

Q can also be adjusted by the ratio of C_1 to C_2, as shown below.

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{5.10}$$

The APF topology in Figure 5.15 can be configured to have a 0-dB voltage gain. However, with high Q, the intermediate nodes will gain more than 0 dB. Therefore, considering the large-signal characteristics in a 1.8 V supply, the lower Q stage should be placed in the front stage, and the higher Q one should be placed in the post stage, as a low Q first strategy. To obtain the desired APF frequency characteristic, the output resistance of the gm must be increased to the order of ten MΩ. In this study, high output resistance was achieved by the folded cascode topology shown in Figure 5.16. Furthermore, the linear input range was expanded by incorporating resistive source degeneration in the input differential stage. Figure 5.17 shows the schematic of the gm-C-based CTPC, which comprises a sixth-order APF and a third-order LPF. Only the first LPF stage gains 16 dB by using a 6× gm as a post amplifier in an AFE.

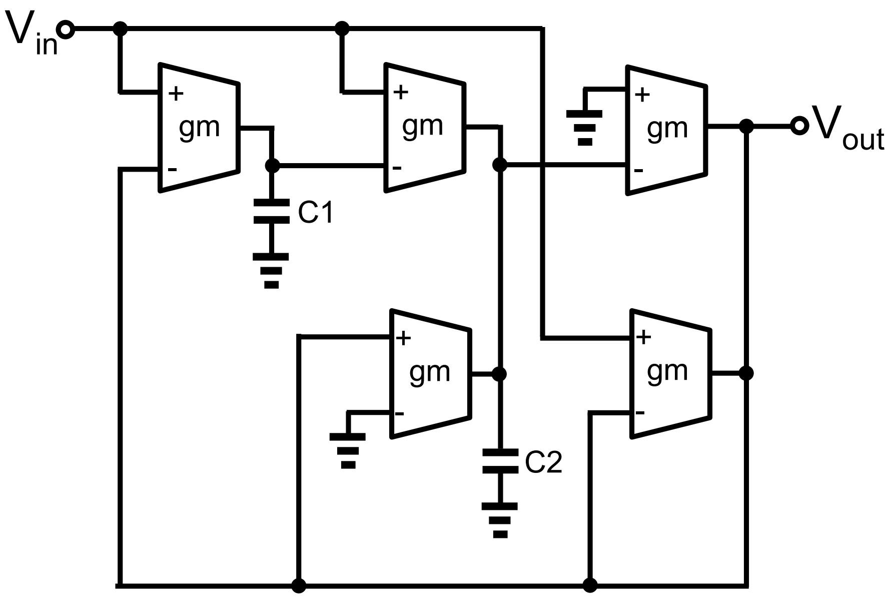


Figure 5.15 Schematic of second-order APF using gm-C.

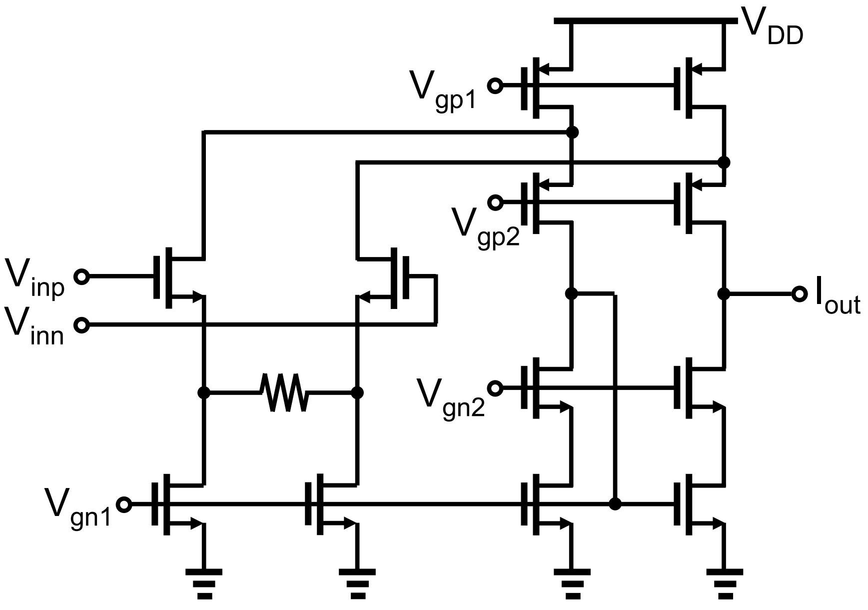


Figure 5.16 Schematic of folded cascode gm with source degeneration.

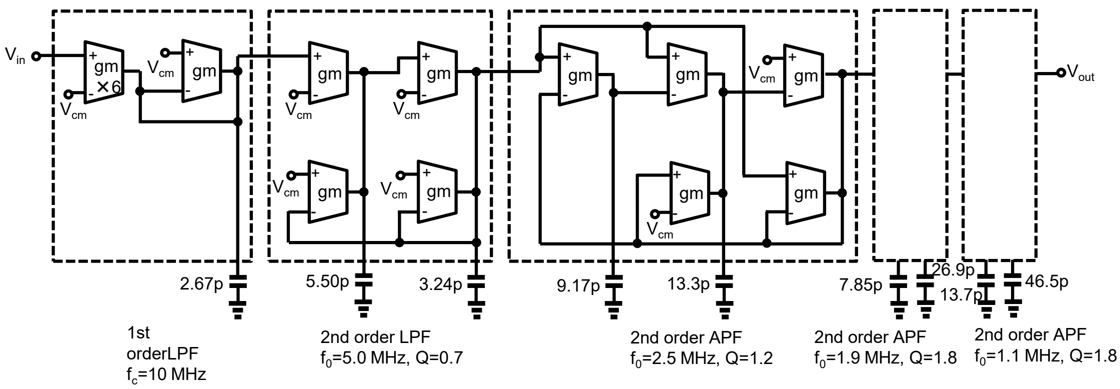


Figure 5.17 Full schematic of the proposed CTPC with gm-C including third-order LPF and sixth-order APF.

5.4.2 Mismatch Considered Simulation

Next, we will show the simulation results of the gm-C CTPC for chip integration. Figure 5.18 shows the AC characteristics of the gm-C CTPC, based on 200 Monte Carlo trial analyses assuming calibration for process variation and considering device mismatch. The gain characteristic in Figure 5.18(a) peaks around 2 MHz due to the non-ideality of the gm frequency characteristics. The GD in Figure 5.18(b) is approximately linear from 1 MHz to 4 MHz, as desired, even under device mismatch. Furthermore, by inputting a CW test waveform with a known frequency into the CTPC and trimming the bias current of gm so that the desired delay (phase difference) is obtained between the input and output, it is possible to calibrate the characteristics against global process variations.

Figure 5.19 shows the results of a mismatch-considered 200 Monte Carlo trial analysis of the transient response for a chirp signal input of 1 MHz to 4 MHz in 1.5 μs. Although the DC common potential varies due to the mismatch, the pulse peak-to-peak voltage and pulse shape do not vary significantly, as expected from the Monte Carlo AC characteristics, and the impact is acceptable.

Figure 5.20 shows the large-signal characteristics of the gm-C CTPC. Similar to Figure 5.9, which presents the measurement result of the OPA-and-RC-based CTPC, Figure 5.20(a) displays the input signal and output signal when a 1 MHz to 4 MHz linear chirp signal is applied to the gm-C CTPC in 1.5 μs and a 2 MHz CW signal. The signal enhancement merit due to compression is 5.30 dB.

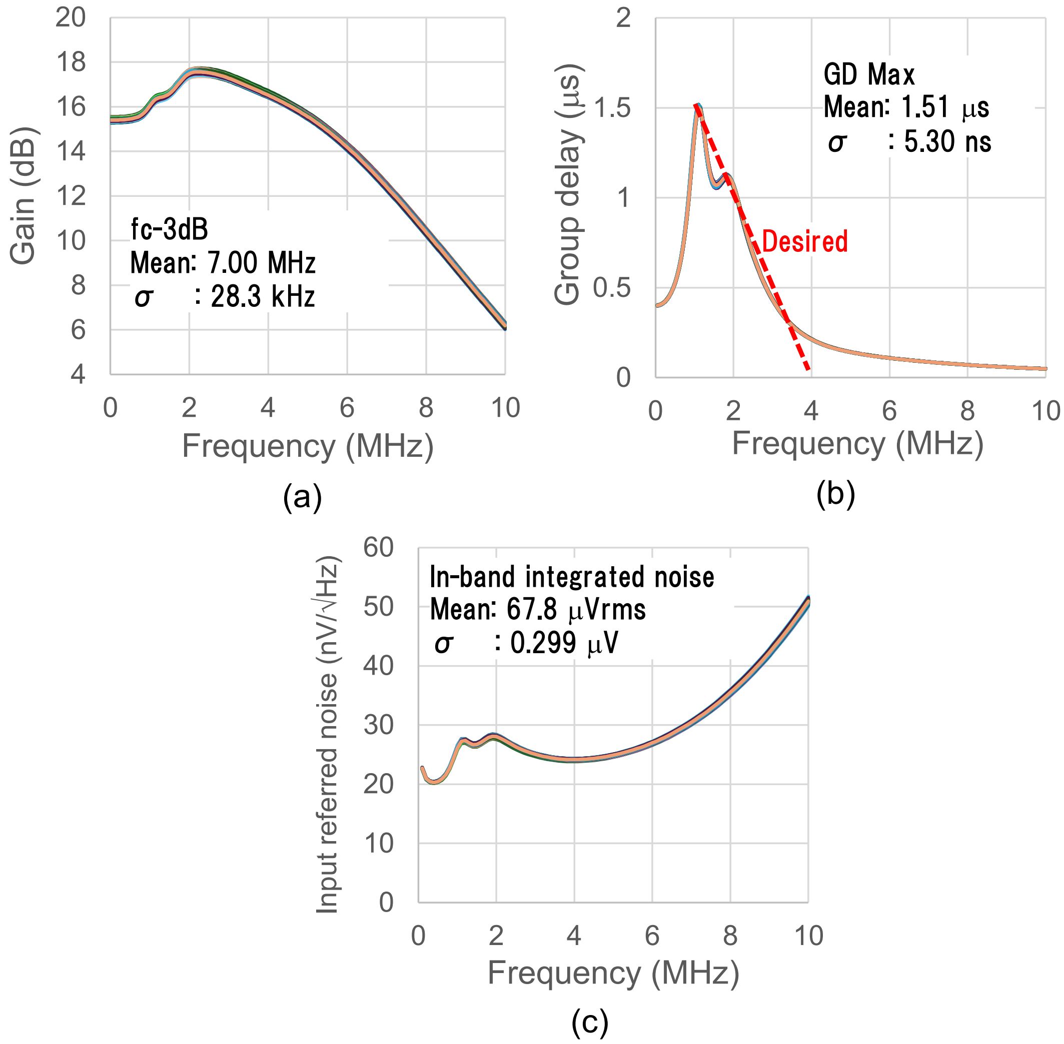


Figure 5.18 Simulated AC characteristics of gm-C CTPC across 200 Monte Carlo trials considering mismatch: (a) gain, (b) group delay, (c) input referred noise voltage.

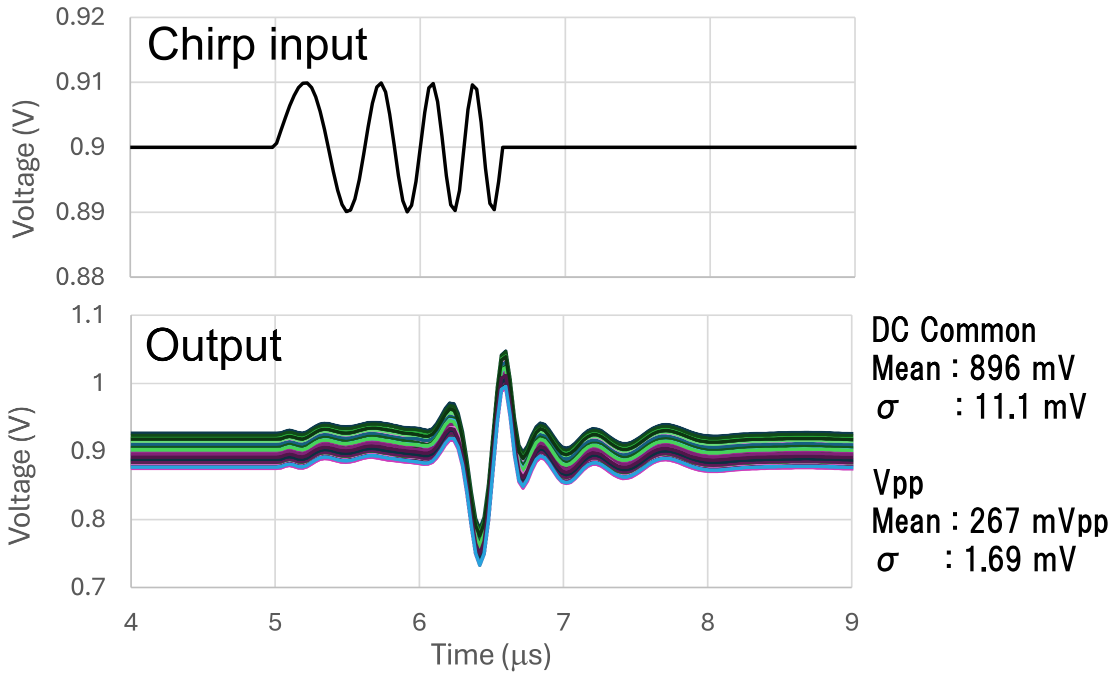


Figure 5.19 Simulated transient waveforms of gm-C CTPC across 200 Monte Carlo trials considering mismatch.

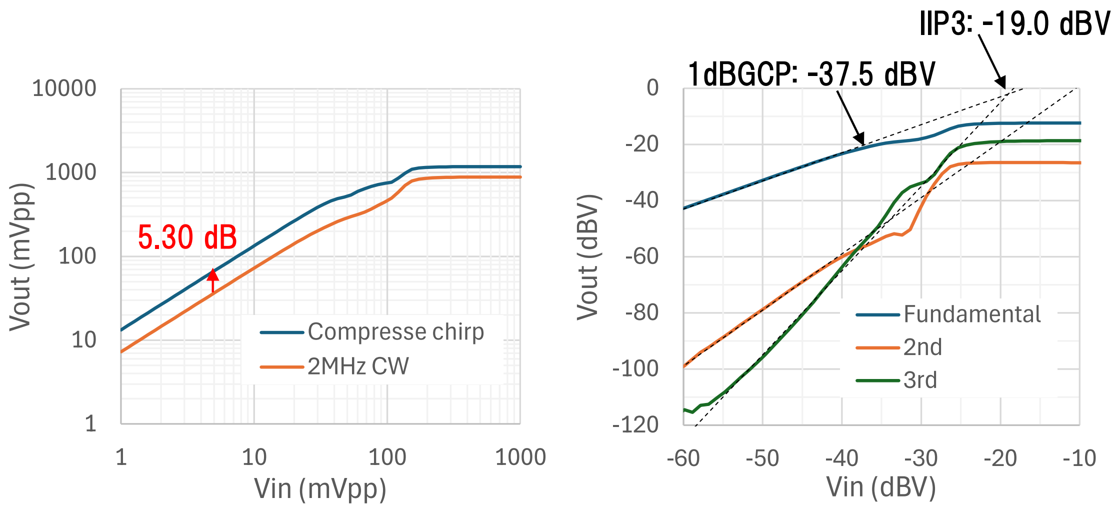


Figure 5.20 Simulated large-signal characteristics: (a) input vs output peak-to-peak voltage for 1 MHz to 4 MHz linear chirp signal input and 2 MHz CW input, (b) simulated input vs output characteristics for fundamental, second-harmonic, and third-harmonic for 2 MHz CW input.

At the end of this section, Table 5.2 compares the power dissipation and circuit area of the PC implemented with TSMC 180-nm RF technology in analog and digital configurations. Assuming 14-bit digitized RX data and 20 MSample/s sampling, a 77-tap matched filter is required to cover a chirp period of the CTPC input waveform in Figure 5.11. When compared using 180-nm technology, the analog implementation using metal-insulator-metal (MIM) capacitors consumes less power and occupies an order of magnitude smaller area than the digital implementation, as shown in Table 5.2. The area calculation assumes the total active regions of parameterized cells (PCell) and standard cells for both analog and digital implementations, excluding wiring margin area. Thus, we can estimate that the proposed analog CTPC implementation has power and area advantages over digital implementation, albeit in a mature technology. Analog implementation is less susceptible to the benefits of scaling, and concerns include increased variation due to process shrinkage and dynamic range degradation caused by lowered VDD. Some degree of power saving can be expected through an increase in gm achieved by thinning the gate oxide. On the other hand, digital implementation benefits from scaling; therefore, power dissipation and area were also estimated for 65-nm digital implementation. Using 65-nm technology, the power dissipation of digital implementation can be reduced to 10 mW; however, even so, 180-nm analog is still superior, and the area is comparable between 180-nm analog and 65-nm digital. Even with the shrinkage of digital circuits, it is not possible to eliminate AAF before digitization. Therefore, we believe that the advantages of the proposed CTPC, which can be easily integrated with AAF, will remain in the future over digital implementation using fine technologies.

Table 5.2 Comparison of analog and digital implementations of pulse compressor

Implementation	Analog 180-nm	Digital 180-nm	Digital 65-nm
Architecture	gm-C CTPC: 3rd LPF + 6th APF	14-bit, 77-tap matched filter	14-bit, 77-tap matched filter
Power	6.0 mW	68 mW	10 mW
Area	0.227 mm^2	2.11 mm^2	0.201 mm^2
Resources	gm × 21 Total MIM capacitance: 129 pF	14-bit 77-tap shift register, 14-bit × 14-bit Multiplier × 77, 35-bit full adder × 77	14-bit 77-tap shift register, 14-bit × 14-bit Multiplier × 77, 35-bit full adder × 77

5.5 Conclusions

We have proposed a novel CTPC that performs continuous-time pulse compression in the analog domain. The implementation using discrete OPA and RC was investigated. Electrical measurements verified the following performance. Using chirp signals from 1 MHz to 4 MHz, we obtained a signal enhancement effect of 6.7 dB electrically. This merit can be achieved by employing ideal broadband TDs in a medium where frequency-dependent attenuation is negligible. We can also allocate this benefit to TX voltage lowering in the system design.

Additionally, in acoustic characterization, we experimentally explored the optimal chirp period, achieving a signal enhancement effect of 5.5 dB and a compression factor of 3.2. The B-mode image of the square wave chirp TX was obtained using a sector scan, and the CTPC also verified using a compressed B-mode image. The compression by the CTPC improved the axial resolution in the depth direction in the B-mode image.

We also studied chip integration and estimated that a gm-C CTPC implementation using 180-nm technology would consume about an order of magnitude less power and area than a matched filter implementation in the digital domain using the same technology.

Chapter 6
Conclusion

6.1 Summary

Medical ultrasound diagnostic systems are required to improve examination workflow and reduce dependence on the skills of the examiners who operate the probes. Demand for use cases outside the laboratory is also expected to increase in the future, such as examination in off-site clinics in developing countries and home healthcare in an aging society. To meet this demand, a matrix probe with a two-dimensional array of transducers is indispensable, as it can acquire arbitrary cross-sectional images by volume imaging without requiring the probe to be moved while it is placed on the body surface. Furthermore, the miniaturization of the matrix probe into a wireless handheld device will significantly expand its use. To achieve a compact matrix probe, it is essential to integrate an ASIC with a beamformer function into the probe. It is also essential to suppress the heat generation of the ASIC (2-D array IC) in the probe, i.e., to reduce power dissipation, in order to prevent low-temperature burns on the examinee who comes into direct contact with the probe during the examination. Additionally, the transceiver circuit of one channel must fit within the area of the transducer pitch, which is determined by the grating lobe and scanning angle requirements. Therefore, it was essential to reduce the circuit's area. In this study, we investigated low-power technologies to limit the power dissipation of the ASIC to approximately 2 W, which can be dissipated through natural air cooling of the probe. Additionally, we explored small-area technologies to maintain the circuit area of one channel within the target of 300 μm × 300 μm. The following conclusions were reached.

(1) The 32-tap switched-capacitor delayer circuit in each ECh of the 2-D array IC used for beamforming is area-hungry. This circuit, implemented in a reconfigurable manner using 180-nm HV SOI CMOS technology, achieved time-sharing operation for TX and RX, thereby fittng the area of the analog delay circuit and adder circuit to 30,600 μm^2. This represents 34 % of the ECh area. Additionally, by employing a passive-operation charge domain adder, the power dissipation of the delay + adder circuit achieved 192 μW/ECh. This represents 26 % of the power dissipation per ECh. Furthermore, by assembling the probe, real-time 3-D imaging was successfully achieved, and practical spatial resolution was confirmed in phantom images, including THI imaging using harmonics.

(2) The TRSW in each ECh of the 2-D array IC is also area-hungry because it uses multiple HV-MOSs. Additionally, it typically consumes power that does not contribute to performance due to the constant flow of static current through the HV supply path. In this study, we adopted an architecture that combines a dynamic shunt switch and source driven on/off control, and implemented the world's first circuit composed of only three HV-MOS devices as a bipolar pulse-compatible TRSW. The circuit area was fit to 9900 μm^2. This is 11 % of the ECh area. The power dissipation is zero μW for TX and only 12.1 μW for RX. Furthermore, the proposed TX-to-RX switching sequence control reduced undesired noise generation due to switching by 18.1 dB. Additionally, the signal was looped back from TX to RX inside the 2-D array IC, and the TRSW functioned as an attenuator to enable on-wafer and field testing.

(3) Continuous-time pulse compression in the analog domain was investigated to enhance image quality performance further and achieve both improved penetration and axial spatial resolution. Conventional pulse compression processing in the digital domain requires a multi-bit, long-tap matched filter to correlate the RX signal with the TX waveform template, consuming computing resources. We designed a continuous-time pulse compressor with linear group delay with respect to frequency by using four OPAs

and RC and implemented it on a PCB. Combining this with chirp TX, we showed that a signal enhancement of 6.7 dB can be achieved through compression. In addition, a compression factor of 3.2 for acoustic measurements and improved spatial resolution on B-mode images were confirmed. Chip integration using 180-nm technology was also investigated by simulation. In the case of chip integration, the use of a gm-C integrator can be implemented with a smaller capacitance value than using OPAs and RC. Comparing the proposed analog implementation with the digital implementation, the analog implementation is expected to consume 8.8 % of the power and 13 % of the area of the digital implementation. Although the digital implementation offers greater scaling benefits when using fine technologies, the analog implementation is superior in terms of power and area by one order of magnitude at 180-nm. It is also possible to allocate the proposed pulse compression technology to lower power and smaller area as a reduction of TX voltage rather than enhanced performance.

In conclusion, we have demonstrated that a 2-D array IC with a power of 2.3 W and an ECh area of 300 μm × 300 μm can be realized using the technology studied in this research, and that a practical matrix probe can be achieved. Furthermore, we have successfully enhanced image performance by utilizing the pulse compression technique.

6.2 Future Research Directions

This study examined low-power and small-area ASICs in matrix probes. For validation, image acquisition in Chapters 3 and 4 was performed using a system in which the probe was connected to a cart-type main instrument unit and the RX analog signals after subarray μBF were transmitted via a cable. In Chapter 5, image acquisition was performed using an imaging prototype PCB connected to a cable-mounted matrix probe and a CTPC PCB. The ultimate goal is to develop a wireless handheld matrix probe system where RX volume signals are digitized and processed in the probe, transmitted to a smartphone via WiFi, and displayed as images on the smartphone. The 2-D array IC technology developed in this study, particularly the reduction of resources for the subsequent ADCs and digital circuits through channel reduction using μBF in analog domain, combined with pulse compression to lower the TX voltage, is effective for realizing such systems. Unlike DBF, which can use RX data stored in memory, analog μBF loses RX data with ECh granularity after signal summation. Although this has the disadvantage of making flexible ECh-level processing such as synthetic aperture impossible, the effect of reducing resources in the latter stages is immeasurable.

This study does not address ADCs, which are essential for digitization and power hungry. In recent years, successive approximation register (SAR) ADCs have been reported that save power by sharing most significant bit (MSB) among four channels (2×2) based on signal similarity between adjacent channels for ultrasound applications [110]. Such hardware sharing is effective for reducing the area and power dissipation of RX circuits. In TX circuits, research is progressing on multilevel pulsers [111] and high-power-efficient charge-recycling pulsers [36], [110]. Since harmonics of square waves, whose frequencies are outside the TD bandwidth, do not contribute to acoustic power, arbitrary waveforms are preferable. However, linear amplifiers capable of transmitting arbitrary waveforms consume static power. A pulser capable of transmitting 7-level pulses that closely resemble arbitrary waveforms while utilizing the low power dissipation of pulsers has been reported [111]. There might be room for reducing TX power by utilizing charge recycling that takes advantage of multi-level pulsing.

By combining the results of this study with the above-mentioned low-power ADC and multi-level low-power pulser, it is expected that a compact wireless handheld matrix probe that even non-experts can use will be realized. If this becomes a reality, an ultrasound probe will undoubtedly be a standard household item, enabling ultrasound examinations to be performed anytime, anywhere.

References

[1] D. Kumar, B. Pratap, N. Boora, R. Kumar, and N. K. Sah, "A comparative study of medical imaging modalities," *International Journal of Radiology Sciences*, vol. 3, no. 1, pp. 9-16, Oct. 2021.

[2] K. T. Dussik, "Über die Möglichkeit, hochfrequente mechanische Schwingungen als diagnostische Mittel zu verwerten," *Zeitschrift für die gesamte Neurologie und Psychiatrie*, vol. 174, pp. 153-168, Dec. 1942.

[3] I. Edler and C. H. Hertz, "The Use of Ultrasonic Reflectoscope for the Continuous Recording of the Movements of Heart Walls," *Kungl Fysiografiska Sällskapets I Lund Förhandlingar*, vol. 24, no. 5, pp. 40-58, 1954.

[4] D. H. Howry, G. Posakony, C. R. Cushman, and J. H. Holmes, "Three-Dimensional and Stereoscopic Observation of Body Structures by Ultrasound," *Journal of Applied Physiology*, vol. 9, no. 2, Sep. 1956.

[5] S. Satomura, "Ultrasonic Doppler Method for the Inspection of Cardiac Functions," *The Journal of the Acoustical Society of America,* vol. 29, no. 11, pp. 1181-1185, Nov. 1957.

[6] I. Donald, J. Macvicar, and T. G. Brown, "Investigation of abdominal masses by pulsed ultrasound, " *The Lancet*, vol. 271, no. 7032, pp. 1188-1195, Jun. 1958.

[7] M. K. Eyer, M. A. Brandestini, D. J. Phillips, and D. W. Baker, "Color digital echo/Doppler image presentation," *Ultrasound in Medicine & Biology*, vol. 7, no. 1, pp. 21-31, 1981.

[8] A. P. Sarvazyan, O. V. Rudenko, S. D. Swanson, J. B. Fowlkes, and S. Y Emelianov, "Shear wave elasticity imaging: a new ultrasonic technology of medical diagnostics," *Ultrasound in Medicine & Biology*, vol. 24, no. 9, pp. 1419-1435, Dec. 1998.

[9] D. P. Skinner, R. E. Newnham, and L. E. Cross, "Flexible composite transducers," *Materials Research Bulletin*, vol. 13, no. 6, pp. 599-607, Jun. 1978.

[10] M. I. Haller and B. T. Khuri-Yakub, "A surface micromachined electrostatic ultrasonic air transducer," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 43, no. 1, pp. 1-6, Jan. 1996.

[11] P. Muralt, D. Schmitt, N. Ledermann, J. Baborowski, P. K. Weber, W. Steichen, S. Petitgrand, A. Bosseboeuf, N. Setter, and P. Gaucher. "Study of PZT coated

membrane structures for micromachined ultrasonic transducers [medical imaging]," in *IEEE Ultrasonics Symposium*, pp. 907-911, Oct. 2001.

[12] C. Bantignies, P. Mauchamp, G. Férin, S. Michau, and R. Dufait, "Focused 20 MHz single-crystal piezocomposite ultrasound array," in *IEEE International Ultrasonics Symposium*, pp. 2722-2725, Sep. 2009.

[13] W. Buschmann, "New equipment and transducers for ophthalmic diagnosis," *Ultrasonics*, vol. 3, no. 1, pp. 18-21, Mar. 1965.

[14] J. C. Somer, "Electronic sector scanning for ultrasonic diagnosis," *Ultrasonics*, vol. 6, no. 3, pp. 153-159, Jul. 1968.

[15] W. J. Fry, G. H. Leichner, D. Okuyama, F. J. Fry, and E. K. Fry, "Ultrasonic Visualization System Employing New Scanning and Presentation Methods," *The Journal of the Acoustical Society of America*, vol. 44, pp. 1324-1338, Nov. 1968.

[16] F. J. Harris, "On the use of windows for harmonic analysis with the discrete Fourier transform," *Proceedings of the IEEE*, vol. 66, no. 1, pp. 51-83, Jan. 1978.

[17] K. Nagai, "A New Synthetic-Aperture Focusing Method for Ultrasonic B-Scan Imaging by the Fourier Transform," *IEEE Transactions on Sonics and Ultrasonics*, vol. 32, no. 4, pp. 531-536, Jul. 1985.

[18] B. Ward, A. C. Baker, and V. F. Humphrey, "Nonlinear propagation applied to the improvement of resolution in diagnostic medical ultrasound," *The Journal of the Acoustical Society of America*. 101, pp. 143-154, Jan. 1997.

[19] S. W. Smith, W. Lee, E. D. Light, J. T. Yen, P. Wolf, and S. Idriss, "Two dimensional arrays for 3-D ultrasound imaging," in *IEEE Ultrasonics Symposium*, pp. 1545 -1553, Oct. 2002.

[20] D. H. Turnbull and F. S. Foster, "Beam steering with pulsed two-dimensional transducer arrays," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 38, no. 4, pp. 320-333, Jul. 1991.

[21] G. Montaldo, M. Tanter, J. Bercoff, N. Benech, and M. Fink, "Coherent plane-wave compounding for very high frame rate ultrasonography and transient elastography," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 56, no. 3, pp. 489-506, Mar. 2009.

[22] Y. Lee, W. Y. Lee, C.-E. Lim, J. H. Chang, T.-K. Song, and Y. Yoo, "Compounded direct pixel beamforming for medical ultrasound imaging," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 59, no. 3, pp. 572-582, Mar. 2012.

[23] T. Chernyakova and Y. C. Eldar, "Fourier-domain beamforming: the path to compressed ultrasound imaging," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 61, no. 8, pp. 1252-1267, Aug. 2014.

[24] R. J. G. van Sloun, R. Cohen, and Y. C. Eldar, "Deep Learning in Ultrasound Imaging," *Proceedings of the IEEE*, vol. 108, no. 1, pp. 11-29, Jan. 2020.

[25] "LISENDO 880LE," *FUJIFILM Corporation*. [Online]. Available: https://www.fujifilm.com/jp/ja/healthcare/ultrasound/lisendo/lisendo-880le

[26] "LISENDO-compatible probes," *FUJIFILM Corporation*. [Online]. Available: https://www.fujifilm.com/jp/ja/healthcare/ultrasound/lisendo/probes

[27] "Wireless ultrasound diagnostic system iViz air," *FUJIFILM Corporation*. [Online]. Available: https://www.fujifilm.com/jp/ja/healthcare/ultrasound?tag=1497

[28] C. Chen and M. A. P. Pertijs, "Integrated Transceivers for Emerging Medical Ultrasound Imaging Devices: A Review," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 1, pp. 104-114, Sep. 2021.

[29] Y. Zhang and A. Demosthenous, "Integrated Circuits for Medical Ultrasound Applications: Imaging and Beyond," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 5, pp. 838-858, Oct. 2021.

[30] Y. -S. Kim, M. J. Park, H. Rhim, M. W. Lee, and H. K. Lim, "Sonographic Analysis of the Intercostal Spaces for the Application of High-Intensity Focused Ultrasound Therapy to the Liver," *American Journal of Roentgenlology*, vol. 203, no. 1, pp. 201-208, Jul. 2014.

[31] S. Bae, H. Song, and T. -K. Song, "Analysis of the Time and Phase Delay Resolutions in Ultrasound Baseband I/Q Beamformers," *IEEE Transactions on Biomedical Engineering*, vol. 68, no. 5, pp. 1690-1701, May 2021.

[32] H. -Y. Tang, Y. Lu, S. Fung, D. A. Horsley, and B. E. Boser, "Integrated ultrasonic system for measuring body-fat composition," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, pp. 210-211, Feb. 2015.

[33] J. -Y. Um Y. -J. Kim, S. -E. Cho, M. -K. Chae, J. Song, B. Kim, S. Lee, J. Bang, Y. Kim, K. Cho, B. Kim, J. -Y. Sim, and H. -J. Park," An Analog-Digital Hybrid RX Beamformer Chip With Non-Uniform Sampling for Ultrasound Medical Imaging With 2D CMUT Array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 8, no. 6, pp. 799-809, Dec. 2014.

[34] A. Bhuyan, J. W. Choe, B. C. Lee, I. O. Wygant, A. Nikoozadeh, Ö. Oralkan, and B. T. Khuri-Yakub, "Integrated Circuits for Volumetric Ultrasound Imaging With 2-D

CMUT Arrays," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 6, pp. 796-804, Dec. 2013.
[35] K. Chen, H.-S. Lee, and C. G. Sodini, "A column-row-parallel ASIC architecture for 3-D portable medical ultrasonic imaging," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, pp. 738-751, Mar. 2016.
[36] K. Chen, H.-S. Lee, A. P. Chandrakasan, and C. G. Sodini, "Ultrasonic imaging transceiver design for CMUT: A three-level 30-Vpp pulse-shaping pulser with improved efficiency and a noise-optimized receiver," *IEEE Journal of Solid State Circuits*, vol. 48, no. 11, pp. 2734-2745, Nov. 2013.
[37] C. Chen, Z. Chen, D. Bera, S. B. Raghunathan, M. Shabanimotlagh, E. Noothout, Z. -Y. Chang, J. Ponte, C. Prins, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong, and M. A. P. Pertijs, " A front-end ASIC with receive-array beamforming integrated with a 32×32 PZT matrix transducer for 3-D transesophageal echocardiography ", *IEEE Journal of Solid State Circuits*, vol. 52, no. 4, pp. 994-1006, Apr. 2017.
[38] G. Jung, M. W. Rashid, T. M. Carpenter, C. Tekes, D. M. J. Cowell, S. Freear, F. L. Degertekin, and M. Ghovanloo, "Single-chip reduced-wire active catheter system with programmable transmit beamforming and receive time-division multiplexing for intracardiac echocardiography", in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, pp. 188-190, Feb. 2018.
[39] M. A. Averkiou, D. N. Roundhill, and J. E. Powers, "A new imaging technique based on the nonlinear properties of tissues," in *IEEE Ultrasonics Symposium Proceedings*, pp. 1561-1566, Oct. 1997.
[40] M. A. Averkiou, "Tissue harmonic imaging," in *IEEE Ultrasonics Symposium Proceedings*, pp. 1563-1572, Oct. 2000.
[41] T. L. Szabo and P. A. Lewin, "Ultrasound transducer selection in clinical imaging practice," *Journal of Ultrasound in Medicine*, vol. 32, no. 4, pp. 573-582, Apr. 2013.
[42] J. Chen and R. Panda, "Review: Commercialization of piezoelectric single crystals for medical imaging applications," in *IEEE Ultrasonics Symposium Proceedings,* pp. 235-240, Sep. 2005.
[43] Y. Mo, T. Tanaka, S. Arita, A. Tsuchitani, K. Inoue, and Y. Suzuki, "Pipelined delay-sum architecture based on bucket-brigade devices for on-chip ultrasound beamforming," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, pp. 1754-1757, Oct. 2003.
[44] G. Gurun, J. S. Zahorian, A. Sisman, M. Karaman, P. E. Hasler, and F. L. Degertekin, "An Analog Integrated Circuit Beamformer for High-Frequency Medical Ultrasound

Imaging," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 6, no. 5, pp. 454-467, Oct. 2012.

[45] D. Wildes, W. Lee, B. Haider, S. Cogan, K. Sundaresan, D. M. Mills, C. Yetter, P. H. Hart, C. R. Haun, M. Concepcion, J. Kirkhorn, and M. Bitoun, "4-D ICE: A 2-D array transducer with integrated ASIC in a 10-Fr catheter for real-time 3-D intracardiac echocardiography," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 63, no. 12, pp. 2159-2173, Dec. 2016.

[46] E. Kang, Q. Ding, M. Shabanimotlagh, P. Kruizinga, Z. -Y. Chang, E. Noothout, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong, and M. A. P. Pertijs, " A reconfigurable ultrasound transceiver ASIC with 24×40 elements for 3-D carotid artery imaging ", *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 2065-2075, Jul. 2018.

[47] E. Boni, L. Bassi, and A. Cellai, "High frequency GaN-based pulse generator with active T/R switch circuit," in *IEEE Ultrasonics Symposium Proceedings*, pp. 1595-1598, Sep. 2014.

[48] Y. Hao, Sim. P.C, B. Toner, M. Frank, M. Ackermann, A. Tan, U. Kuniss, E. Kho, J. Doblaski, Hee. E.G, M. Liew, A. Hoelke, S. Wada, and T. Oshima," A 0.18μm SOI BCD technology for automotive application,", in *IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, pp. 177-180, May 2015.

[49] A. Hölke, D. K. Pal, Y. Hao, K. K. Yaw, E. Kho, G. Kittler, U. Kuniss1, and J. Gessner, " A 200 V partial SOI 0.18mm CMOS technology ", in *IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, pp. 257-260, Jun. 2010.

[50] A. Hölke, M. Antoniou, and F. Udrea, "Partial SOI as a HV platform technology for Power Integrated Circuits," in *IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, pp. 435-438, Sep. 2020.

[51] E. C. T. Kho, A. D. Hoelke, S. J. Pilkington, D. K. Pal, W. A. W. Z. Abidin, L. Y. Ng, M. Antoniou, and F. Udrea, "200-V lateral superjunction LIGBT on partial SOI," *IEEE Electron Device Letters,* vol. 33, no. 9, pp. 1291-1293, Sep. 2012.

[52] N. He, S. Zhang, X. Zhu, X. Li, H. Wang, W. Zhang, and B. He, "A 0.25 μm 700 V BCD technology with ultra-low specific on-resistance SJ-LDMOS ", in *IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, pp. 419-422, Sep. 2020.

[53] M. Tan, E. Kang, J. -S. An, Z. -Y. Chang, P. Vince, T. Matéo, N. Sénégond, and M. A. P. Pertijs, "A 64-channel transmit beamformer with ±30-V bipolar high-voltage

pulsers for catheter-based ultrasound probes," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 7, pp. 1796-1806, Jul. 2020.

[54] T. Mahzabeen and B. Banerjee, "A high isolation CMOS switch for loopback built-in self-test in a millimeter-wave transceiver," in *Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS)*, pp. 1-3, Apr. 2013.

[55] X.-L. Huang and J.-L. Huang, "An ADC/DAC loopback testing methodology by DAC output offsetting and scaling," in *VLSI Test Symposium (VTS)*, pp. 289-294, Apr. . 2010.

[56] S. S. Lee, "External loopback testing on high speed serial interface," in *Asia Symposium on Quality Electronic Design (ASQED)*, pp. 148-154, Aug. 2013.

[57] S. Arora, A. Aflaki, S. Biswas, and M. Shimanouchi, "SERDES external loopback test using production parametric-test hardware," in *IEEE International Test Conference (ITC)*, pp. 1-7, Nov. 2016.

[58] B. Kim and J. A. Abraham, "Dynamic performance characterization of embedded single-ended mixed-signal circuits," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 5, pp. 329-333, May 2014.

[59] B. Kim and J. A. Abraham, "Transformer-coupled loopback test for differential mixed-signal dynamic specifications," *IEEE Transactions on Instrumentation and Measurement*, vol. 60, no. 6, pp. 2014-2024, Jun. 2011.

[60] C. Chen, Z. Chen, D. Bera, E. Noothout, Z, -Y. Chang, M. Tan, H. J. Vos, J. G. Bosch, M. D. Verweij, N. de Jong, and M. A. P. Pertijs, "A pitch-matched front-end ASIC with integrated subarray beamforming ADC for miniature 3-D ultrasound probes," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3050-3064, Nov. 2018.

[61] J. Li, Z. Chen, M. Tan, D. van Willigen, C. Chen, Z. -Y. Chang, E. Noothout, N. de Jong, M. Verweij, and M. A. P. Pertijs, "A 1.54 mW/element 150μm-pitch-matched receiver ASIC with element-level SAR/shared-single-slope hybrid ADCs for miniature 3D ultrasound probes," in *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. C220-C221, Jun. 2019.

[62] M. -C. Chen, A. P. Perez, S. -R. Kothapalli, P. Cathelin, A. Cathelin, S. S. Gambhir, and B. Murmann, "A pixel pitch-matched ultrasound receiver for 3-D photoacoustic imaging with integrated delta-sigma beamformer in 28-nm UTBB FD- SOI," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 11, pp. 2843-2856, Nov. 2017.

[63] B. Dufort, T. Letavic, and S. Mukherjee, "Digitally controlled high-voltage analog switch array for medical ultrasound applications in thin-layer silicon-on-insulator process," in *IEEE International SOI Conference*, pp. 78-79, Oct. 2002.

[64] F. Yamashita, J. Aizawa, and H. Honda, "A new compact low on resistance and high off isolation high voltage analog switch IC without using high voltage power supplies for ultrasound imaging system," in *IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, pp. 415-418, Jun. 2016.

[65] Y.-M. Li, R. Wodnicki, N. Chandra, and N. Rao, "An integrated 90 V switch array for medical ultrasound applications," in *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 269-272, Sep. 2006.

[66] S. Dai, R. W. Knepper, and M. N. Horenstein, "A 300-V LDMOS analog-multiplexed driver for MEMS devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 12, pp. 2806-2816, Dec. 2015.

[67] H. Jung, R. Wodnicki, H. G. Lim, C. W. Yoon, B. J. Kang, C. Yoon, C. Lee, J. Y. Hwang, H. H. Kim, H. Choi, M. S. -W. Chen, Q. Zhou, and K. K. Shung, "CMOS high-voltage analog 1-64 multiplexer/demultiplexer for integrated ultrasound guided breast needle biopsy," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 65, no. 8, pp. 1334-1345, Aug. 2018.

[68] K. Hara, J. Sakano, M. Mori, S. Tamano, R. Sinomura, and K. Yamazaki, " A new 80 V 32×32ch low loss multiplexer LSI for a 3D ultrasound imaging system ", in *IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, pp. 359-362, May 2005.

[69] G. Ricotti and V. Bottarel, "HV floating switch matrix with parachute safety driving for 3D echography systems," in *European Solid State Circuits Conference (ESSCIRC)*, pp. 271-273, Sep. 2018.

[70] R. Wodnicki, H. Kang, D. Li, Y. Sun, L. Jiang, R. Chen, Z. Chen, H. Jong, J. Foiret, Y. Liu, V. Chiu, D. N. Stephens, Q. Zhou, and K. W. Ferrara, "Tiled large element 1.75D aperture with dual array modules by adjacent integration of PIN-PMN-PT transducers and custom high voltage switching ASICs," in *IEEE Ultrasonics Symposium Proceedings*, pp. 1955-1958, Oct. 2019.

[71] D. Van Willigen,J. Janjic, E. Kang, Z. Y. Chang, E. Noothout, M. Verweijl, N. Dejong, and M. Pertijs, "ASIC design for a single-cable 64-element ultrasound probe," in *IEEE Ultrasonics Symposium Proceedings*, pp. 1-4, Oct. 2018.

[72] J. Borg and J. Johansson, "An ultrasonic transducer interface IC with integrated push-pull 40 Vpp 400 mA current output 8-bit DAC and integrated HV multiplexer," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 2, pp. 475-484, Feb. 2011.

[73] S.-J. Jung, S.-K. Hong, and O.-K. Kwon, "Area-efficient high-voltage switch using floating control circuit for 3D ultrasound imaging systems," *Electronics Letters*, vol. 50, no. 25, pp. 1900-1902, 2014.

[74] M. Sautto, A. S. Savoia, F. Quaglia, G. Caliano, and A. Mazzanti, "A comparative analysis of CMUT receiving architectures for the design optimization of integrated transceiver front ends," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 64, no. 5, pp. 826-838, May 2017.

[75] M. Liew, N. I. Bolhan, L. Lim, P. C. Sim, H. Yang, and A. Holke, "Integrated zener diodes for smart power ICs," in *IEEE International Nanoelectronics Conferences (INEC)*, pp. 1-5, Jul. 2019.

[76] Y. Nakamura, S. Kajiyama, Y. Igarashi, T. Oshima, and T. Yamawaki, "A low-power current-reuse LNA for 3D ultrasound beamformers," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. 104, no. 2, pp. 492-498, Feb. 2021.

[77] N. Sanchez, K. Chen, C. Chen, D. McMahill, S. Hwang, J. Lutsky, J. Yang, L. Bao, L. K. Chiu, G. Peyton, H. Soleimani, B. Ryan, J. R. Petrus, Y. -J. Kook, T. S. Ralston, K. G. Fife, and J. M. Rothberg, "An 8960-Element Ultrasound-on-Chip for Point-of-Care Ultrasound," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, pp. 480-482, Feb. 2021.

[78] Y. Lee, J. Kang, S. Yeo, J. Lee, G. -D. Kim, Y. Yoo, and T. -K. Song, "A new smart probe system for a tablet PC-based point-of-care ultrasound imaging system: feasibility study," in *IEEE Ultrasonics Symposium Proceedings*, pp. 1611-1614, 2014.

[79] J. Kang, C. Yoon, J. Lee, S. -B. Kye, Y. Lee, J. H. Chang, G. -D. Kim, Y. Yoo, and T. -K. Song, "A System-on-Chip Solution for Point-of-Care Ultrasound Imaging Syst.: Architecture and ASIC Implementation," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 2, pp. 412-423, Apr. 2016.

[80] D. Cacko, M. Walczak, and M. Lewandowski, "Low-Power Ultrasound Imaging on Mixed FPGA/GPU Systems," in *Joint Conference - Acoustics*, pp. 1-6, Sep. 2018.

[81] S. S. Corbett, R. W. Schutz, and J. E. Okies "A finger-worn ultrasound probe for point-of-care applications," in *IEEE Healthcare Innovation Conference (HIC)*, pp. 79-82, Oct. 2014.

[82] A. S. Mudukutore, V. Chandrasekar, and R.J. Keeler, "Pulse compression for weather radars," *IEEE Transactions on Geoscience and Remote Sensing*, vol. 36, no. 1, pp. 125-142, Jan. 1998.

[83] M. L. Oelze, "Bandwidth and resolution enhancement through pulse compression," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 54, no. 4, pp. 768-781, Apr. 2007.

[84] Y. M. Benane, D. Bujoreanu, R. J. Lavarello, F. Varray, J. -M. Escoffre, A. Novell, C. Cachard, and O. Basset. "Experimental Implementation of a Pulse Compression Technique Using Coherent Plane-Wave Compounding," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 65, no. 6, pp. 1025-1036, Jun. 2018.

[85] C. Yoon, W. Lee, J. H. Chang, T. -k. Song, and Y. Yoo, "An efficient pulse compression method of chirp-coded excitation in medical ultrasound imaging," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 60, no. 10, pp. 2225-2229, Oct. 2013.

[86] J. Kang, Y. Kim, W. Lee, and Y. Yoo, "A New Dynamic Complex Baseband Pulse Compression Method for Chirp-Coded Excitation in Medical Ultrasound Imaging," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 64, no. 11, pp. 1698-1710, Nov. 2017.

[87] B. -H. Kim, S. Lee, Y. Kim, K. Cho, T. Jeon, K. Kim, and J. Song, "An experimental study on coded excitation in CMUT arrays to utilize Simultaneous Transmission Multiple-zone Focusing method with Freq. divided sub-band chirps," in *IEEE Ultrasonics Symposium Proceedings*, pp. 1428-1431, Jul. 2013.

[88] N. Wang, C. Yang, J. Xu, W. Shi, W. Huang, Y. Cui, and X. Jian, "An Improved Chirp Coded Excitation Based on the Compression Pulse Weighting Method in Endoscopic Ultrasound Imaging," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 68, no. 3, pp. 446-452, Mar. 2021.

[89] Y. Machhiwar, G. Gill, K. N. Kaushal, N. R. Mohapatra, and H. Agarwal, "Compact Modeling of LDMOS Transistors Over a Wide Temperature Range Including Cryogenics," *IEEE Transactions on Electron Devices*, vol. 71, no. 1, pp. 77-83, Jan. 2024.

[90] B. Toner, S. Eisenbrandt, M. Frank, R. Granzner, L. Steinbeck, D. Davis, G. M. Dolny, T. J. Johnson, and W. R. Richards, "No-Snapback LDMOS Using Adaptive RESURF and Hybrid Source for Ideal SOA," *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 902-908, 2021.

[91] B. Toner, C. Ellmers, S. Eisenbrandt, L. Zhengchao, D. Davis, G. Dolny, T. Johnson, and W. Richards, "Addressing the challenges of sub-50nm channel LDMOS," in

IEEE International Symposium on Power Semiconductor Devices & IC's (ISPSD), pp. 291-294, Jun. 2021.

[92] D. R. Gallagher, N. Y. Kozlovski, and D. C. Malocha, "Ultra-wideband communication system prototype using orthogonal frequency coded SAW correlators," *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 60, no. 3, pp. 630-636, Mar. 2013.

[93] J. Liu and J. Yao, "Wireless RF Identification System Based on SAW," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 2, pp. 958-961, Feb. 2008.

[94] P. -C. Ku, K. -Y. Shih, and L. -H. Lu, "A High-Voltage DAC-Based Transmitter for Coded Signals in High Frequency Ultrasound Imaging Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 9, pp. 2797-2809, Sep. 2018.

[95] N. N. M. Rozsa, Z. Chen, T. Kim, P. Guo, Y. M. Hopf, J. Voorneveld, D. Simoes dos Santos, E. Noothout, Z. -Y. Chang, C. Chen, V. A. Henneken, N. de Jong, H. J. Vos, J. G. Bosch, M. D. Verweij, and M. A. P. Pertijs, "A 2000-volumes/s 3-D Ultrasound Probe With Monolithically-Integrated 23 × 23-mm² 4096 -Element CMUT Array," *IEEE Journal of Solid-State Circuits*, vol. 60, no. 4, pp. 1397-1410, Apr. 2025.

[96] I. Mondal and N. Krishnapura, "A 2-GHz Bandwidth, 0.25-1.7 ns True-Time-Delay Element Using a Variable-Order All-Pass Filter Architecture in 0.13 mm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2180-2193, Aug. 2017.

[97] I. Mondal and N. Krishnapura, "Effects of AC Response Imperfections in True-Time-Delay Lines," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 4, pp. 1173-1177, Apr. 2021.

[98] S. K. Garakoui, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, "Compact Cascadable gm-C All-Pass True Time Delay Cell With Reduced Delay Variation Over Frequency," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 3, pp. 693-703, Mar. 2015.

[99] P. Ahmadi, M. H. Taghavi, L. Belostotski, and A. Madanayake, "A 0.13-μm CMOS Current-Mode All-Pass Filter for Multi-GHz Operation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 23, no. 12, pp. 2813-2818, Dec. 2015.

[100] P. Ahmadi, B. Maundy, A. S. Elwakil, L. Belostotski, and A. Madanayake, "A New Second-Order All-Pass Filter in 130-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 3, pp. 249-253, Mar. 2016.

[101] I. Mondal and N. Krishnapura, "Expansion and Compression of Analog Pulses by Bandwidth Scaling of Continuous-Time Filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 9, pp. 2703-2714, Sep. 2018.

[102] H. G. Han, B. G. Yu, and T. W. Kim, "A 1.9-mm-Precision 20-GHz Direct-Sampling Receiver Using the Time-Extension Method for Indoor Localization," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 6, pp. 1509-1520, Jun. 2017.

[103] J. S. Abel, V. Valimaki, and J. O. Smith, "Robust, Efficient Design of Allpass Filters for Dispersive String Sound Synthesis," *IEEE Signal Processing Letters*, vol. 17, no. 4, pp. . 406-409, Apr. 2010.

[104] B. Xiang, A. Kopa, Z. Fu, and A. B. Apsel, "Theoretical Analysis and Practical Considerations for an Integrated Time-Stretching System Using Dispersive Delay Line (DDL)," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 11, pp. 3449-3457, Nov. 2012.

[105] J. D. Schwartz, J. Azana, and D. V. Plant, "A Fully Electronic System for the Time Magnification of Ultra-Wideband Signals," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 2, pp. 327-334, Feb. 2007.

[106] Y. Han and B. Jalali, "Continuous-time time-stretched analog-to-digital converter array implemented using virtual time gating," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 52, no. 8, pp. 1502-1507, Aug. 2005.

[107] J. D. Schwartz, J. Azana, and D. V. Plant, "An electronic temporal imaging system for compression and reversal of arbitrary UWB waveforms," in *IEEE Radio and Wireless Symposium*, pp. 487-490, 2008.

[108] A. Raj, D. R. Bhaskar, and P. Kumar, "Multiple-Input Single-Output Universal Biquad Filter Using Single Output OTAs," in *IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, pp. 1237-1240, Oct. 2018.

[109] S. -F. Wang, H. -P. Chen, Y. Ku, and Y. -C. Lin, "A novel voltage-mode universal second-order filter using five single ended OTAs and its quadrature sinusoidal oscillator application," *Measurement and Control*, vol. 55, no. 9-10, pp. 927-934, Aug. 2022.

[110] J. Lee, K. -R. Lee, B. E. Eovino, J. H. Park, L. Y. Liang, L. Lin, H. -J. Yoo, and J. Yoo, "A 36-Channel Auto-Calibrated Front-End ASIC for a pMUT-Based Miniaturized 3-D Ultrasound System," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 6, pp. 1910-1923, Jun. 2021.

[111] K. -J. Choi, H. G. Yeo, H. Choi, and D. -W. Jee, "A 28.7V Modular Supply Multiplying Pulser With 75.4% Power Reduction Relative to CV^2f," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 3, pp. 858-862, Mar. 2021.

Published Papers

Journal Papers Related to Thesis

[1] Yutaka Igarashi, Shinya Kajiyama, Yusaku Katsube, Takuma Nishimoto, Tatsuo Nakagawa, Yasuyuki Okuma, Yohei Nakamura, Takahide Terada, Taizo Yamawaki, Toru Yazaki, Yoshihiro Hayashi, Kazuhiro Amino, Takuya Kaneko, and Hiroki Tanaka, "Single-Chip 3072-Element-Channel Transceiver/128- Subarray-Channel 2-D Array IC With Analog RX and All-Digital TX Beamformer for Echocardiography," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 9, pp. 2555-2567, Sep. 2019. (Chapter 3)

[2] Shinya Kajiyama, Yutaka Igarashi, Toru Yazaki, Yusaku Katsube, Takuma Nishimoto, Tatsuo Nakagawa, Yohei Nakamura, Yoshihiro Hayashi, Takuya Kaneko, Hiroki Ishikuro, and Taizo Yamawaki, "T/R Switch Composed of Three HV-MOSFETs With 12.1-μW Consumption That Enables Per-Channel Self-Loopback AC Tests and -18.1-dB Switching Noise Suppression for 3-D Ultrasound Imaging With 3072-Ch Transceiver," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 30, no. 2, pp. 153-165, Feb. 2022. (Chapter 4)

[3] Shinya Kajiyama, Mizuki Mori, Yuki Koroyasu, Tomonari Nagata, Takahisa Mitsui, Nobuhiko Nakano, and Hiroki Ishikuro, "A Continuous-Time Pulse Compressor with Linear Frequency-Dependent Delay Achieving 1.66-μs Maximum Delay and Received Echo Enhancement by 6.7-dB for Ultrasound Imaging," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, vol. E109-A, no.1, pp. TBD, Jan. 2026. (Chapter 5)

Presentations at Conferences Related to Thesis

[1] Yusaku Katsube, Shinya Kajiyama*, Takuma Nishimoto, Tatsuo Nakagawa, Yasuyuki Okuma, Yohei Nakamura, Takahide Terada, Yutaka Igarashi, Taizo Yamawaki, Toru Yazaki, Yoshihiro Hayashi, Kazuhiro Amino, Takuya Kaneko, and Hiroki Tanaka, "Single-chip 3072ch 2D array IC with RX analog and all-digital TX beamformer for 3D ultrasound imaging," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, pp. 458-459, Feb. 2017.

[2] Shinya Kajiyama*, Yutaka Igarashi, Toru Yazaki, Yusaku Katsube, Takuma Nishimoto, Tatsuo Nakagawa, Yohei Nakamura, Yoshihiro Hayashi, and Taizo Yamawaki, "T/R-Switch Composed of 3 High-Voltage MOSFETs with 12.1 μW Consumption that can Perform Per-channel TX to RX Self-Loopback AC Tests for 3D Ultrasound Imaging with 3072-channel Transceiver," in *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 305-308, Nov. 2019.

Other Journal Papers

[1] Shinya Kajiyama, Kazuo Miyamura, and Yohichi Gohshi, "Investigation of Molybdenum Disulphide Using a Scanning Tunneling Microscope under Irradiation of Monochromated UV-VIS," *Analytical Sciences,* vol. 13, no. 5, pp. 803-806, Oct. 1997.

[2] Hideaki Kurata, Kazuo Otsuga, Akira Kotabe, Shinya Kajiyama, Taro Osabe, Yoshitaka Sasago, Shunichi Narumi, Kenji Tokami, Shiro Kamohara, and Osamu Tsuchiya, "Random Telegraph Signal in Flash Memory: Its Impact on Scaling of Multilevel Flash Memory Beyond the 90-nm Node Osamu Tsuchiya, "Random Telegraph Signal in Flash Memory: Its Impact on Scaling of Multilevel Flash Memory Beyond the 90-nm Node ," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1362-1369, Jun. 2007.

[3] Shinya Kajiyama, Kenichiro Sonoda, Kazuo Otsuga, Hideaki Kurata, and Kiyoshi Ishikawa, "A Design of Constant-Charge-Injection Programming Scheme for AG-

AND Flash Memories Using Array-Level Analytical Model," *IEICE Transactions*, vol. E91-C, no. 4, pp. 526-533, Apr. 2008. -533, Apr. 2008.

[4] Shinya Kajiyama, Masamichi Fujito, Hideo Kasai, Makoto Mizuno, Takanori Yamaguchi, and Yutaka Shinagawa, "A 300 MHz Embedded Flash Memory with Pipeline Architecture and Offset-Free Sense Amplifiers for Dual-Core Automotive Microcontrollers," *IEICE Transactions on Electronics*, vol. E92-C no. 10, pp. 1258-1264, Oct. 2009.

[5] Yohei Nakamura, Shinya Kajiyama, Yutaka Igarashi, Takashi Oshima, and Taizo Yamawaki, "A Low-Power Current-Reuse LNA for 3D Ultrasound Beamformers," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences,* vol. E104-A, no. 2, pp. 492-498, Feb. 2021.

Other International Conferences

[1] Hideaki Kurata*, Kazuo Otsuga, Akira Kotabe, Shinya Kajiyama, Taro Osabe, Yoshitaka Sasago, Shunichi Narumi, Kenji Tokami, Shiro Kamohara, and Osamu Tsuchiya, "The Impact of Random Telegraph Signals on the Scaling of Multilevel Flash Memories," in *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, pp. 112-113, Jun. 2006.

[2] Shinya Kajiyama*, Masamichi Fujito, Hideo Kasai, Makoto Mizuno, Takanori Yamaguchi, and Yutaka Shinagawa, "A 300 MHz Embedded Flash Memory with Pipeline Architecture and Offset-Free Sense Amplifiers for Dual-Core Automotive Microcontrollers," in *IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pp. 257-260, Nov. 2008.

[3] Joan Giner*, Yuhua Zhang, Takashi Shiota, Daisuke Maeda, Kazuo Ono, Shinya Kajiyama, Takashi Oshima, Taizo Yamawaki, and Tomonori Sekiguchi, "A concentrated springs architecture for single-digit frequency symmetry in Si MEMS gyroscope," in *IEEE SENSORS*, pp. 1-3, Oct. 2016.

Awards

R&D 100 Awards "Fully Automatic Heart Function Measurement System Using Real-time 3D Ultrasound Imaging Technology," *R&D WORLD*, 2019.

Patents

[1] "Ultrasound probe and ultrasound imaging apparatus using the same," United States Patent No.: US 10,613,206 B2, Apr. 2020.

[2] "Ultrasonic-wave probe, ultrasonic-wave diagnosis apparatus, and test method of ultrasonic-wave probe," United States Patent No.: US 10,595,822 B2, Mar. 2020.

[3] "Switch circuit, ultrasound probe using the same, and ultrasonic diagnosis apparatus," United States Patent No.: US 10,517,570 B2, Dec. 2019.

[4] "Ultrasonic probe, ultrasonic diagnostic apparatus, and ultrasonic transmission/reception switching method," United States Patent No.: US 11,660,076 B2, May 2023.