*Keio University*

# Thesis Abstract

No.

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Title of Thesis:

Distributed Quantum Computing Utilizing Multiple Codes on Imperfect Hardware
（不完全なハードウェア上での複数の符号を用いる分散量子計算）


Summary of Thesis:

Quantum bits have technological imperfections. Additionally, the capacity of a component that can be implemented feasibly is limited. Therefore, distributed quantum computation is required to scale up quantum computers able to solve usefully large problems.

This dissertation presents the design of components of quantum CPUs and of quantum memories taking into account imperfections. Quantum CPUs employ a quantum error correcting code which has faster logical gates and quantum memories employ a code which is superior in space resource requirements. This new quantum computer architecture aimed to realize distributed computation by connecting quantum computer each of which consists of multiple quantum CPUs and multiple quantum memories.

This dissertation focuses on quantum error correcting codes, giving a practical, concrete method for tolerating static losses such as faulty devices for the surface code. To validate this method, I analyzed the resource consumption of cases where faulty devices exist and quantified the increase of resource consumption by numerical simulation with practical assumptions. I found that a yield of functional qubits of 90% is marginally capable of building large-scale systems, by culling the poorer 50% of chips during post fabrication testing. Yield 80% is not usable even when discarding 90% of generated lattices.

For the internal connections between quantum CPU and memory components in a quantum computer and for connections of quantum computers, this dissertation gives a fault-tolerant method to connect quantum components that employ heterogeneous quantum error correcting codes. I have validated this method and quantified the resource consumption of the error management by numerical simulation. I found that the scheme, which discards any quantum state in which any error is detected, always achieves an adequate logical error rate regardless of physical error rates in exchange for increased resource consumption.

Additionally, this dissertation gives a new extension of the surface code suitable for quantum memories. This code is shown to require fewer physical qubits to encode a logical qubit than conventional codes. This code achieves the reduction of 50% physical qubits per a logical qubit.

Collectively, the elements to construct distributed quantum computation by connecting quantum computers are brought together to propose a distributed quantum computer architecture.



Keywords: Quantum computer architecture, Distributed quantum computation,
Quantum error correction, Surface code quantum computation, faulty qubit, quantum
error correction code interoperability