Cryogenic CMOS Low-Power and High-Speed Successive Approximation Register ADC for Scalable Quantum Computer

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Abstract

Quantum computers (QCs) possess the potential to solve complex problems that even supercomputers have limited or no ability to solve. Fault-tolerant QCs (FTQCs) are required since a sufficiently low error rate of quantum bits (qubits) is necessary to achieve general-purpose application. More than several thousands of qubits are necessary for a low error rate. The number of cables that interface with a quantum processor operating at cryogenic temperatures (several mK) thus increases and causes many issues, such as reliability and limitation for increasing qubits. To reduce the cables, ultra-low power and high-speed CMOS control & read-out circuits operating at cryogenic temperatures are required. Because of the limited cooling capacity of the dilution refrigerator and the limited coherence time of qubits, the read-out circuits require low-power (several mW) and high-speed (several tens MS/s ~ several GS/s) ADCs. This research designs a CMOS ultra-low power and high-speed ADC that operates at cryogenic temperatures.

Chapter 1 outlines the progress and the control & read-out circuits of quantum computers.

Chapter 2 describes the characteristics of cryogenic CMOS, including the increase in threshold voltage V_{th} and mismatch. Following the device characteristics, the architecture of ADC is reviewed in terms of power consumption and conversion speed. Following that, the performance issues of SAR ADC, such as speed, are discussed. Dynamic comparators, the core block of ADC, are reviewed and discussed, primarily focusing on the performance improvement of power consumption and delay time. The issues of the switching scheme of SAR ADC at cryogenic temperatures are addressed. The performance of SAR ADC is greatly affected by the switching scheme and the comparator.

Chapter 3 describes the proposed high-speed and low-power CMOS two-stage dynamic comparator. The pre-amplifier adopts the dynamic bias technique to save power. In order to increase the output voltage difference of the pre-amplifier, the amplification is enhanced by inserting a StrongARM latch. The proposed latch remains a cross-coupled inverter pair to ensure good positive feedback. An input pair

replaces the tail current source of the proposed latch to suppress the through current. The auxiliary input pair further enhances gain and positive feedback to speed up the latch. Also, the delay analysis of the dynamic bias technique and the proposed comparator is given, providing a deep understanding and good intuition for circuit design.

Chapter 4 describes the proposed gain boosting dynamic capacitive pre-amplifier (DCA) based comparator. The reservoir capacitor powers the DCA and forms an isolated voltage domain during comparison. It achieves the common-mode variation insensitivity and the dynamic bias. The common-mode variation insensitivity alleviates performance degradation due to common-mode variation. The dynamic bias technique reduces power consumption. The DCA utilizes a cross-coupled pair for gain boosting. It increases the output voltage difference of the DCA and, therefore, speeds up the comparison. The larger initial drain-source voltage of the DCA allows the comparator to operate in a wide input range.

Chapter 5 describes the proposed 10-bit 60-MS/s SAR ADC based on an energy-efficient common-mode variation suppression (CMVS) switching scheme. The proposed CMVS switching scheme reduces energy consumption by about 92% compared to the conventional scheme. In addition, the common-mode variation is suppressed to 16.6% full scale. As a result, it improves the accuracy of the SAR ADC and allows the comparator and SAR ADC to operate in the highest-performance region. Also, increasing common-mode voltage alleviates the performance degradation due to the increased V_{th} at cryogenic temperatures.

Chapter 6 summarizes this research and presents future works.

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Chapter 1

Introduction

1.1 Overview of Quantum Computers

1.1.1 Toward Fault-Tolerant Quantum Computers (FTQCs)

Quantum computers (QCs) have attracted much attention in recent years since they have the potential to solve complex problems that even supercomputers have limited or no ability to solve. For example, drug development, materials discovery, and combinatorial optimization [1]. All of them have enormous amounts of data that need to be processed. Classical computers, including supercomputers, need much time, even more than tens or thousands of years, to process these computations. On the other hand, QCs have proved that they can process enormous amounts of data faster than classical computers.

The fundamental computational unit of QCs is a quantum bit (qubit), like the digital bit utilized by classical computers. The qubit behaves following quantum mechanics. The principle of quantum mechanics states that the quantum has two properties: quantum superposition and quantum entanglement [2]. The quantum superposition states that the quantum can possess all possible states simultaneously. It means that QCs can process all possible data in parallel, while classical comput-

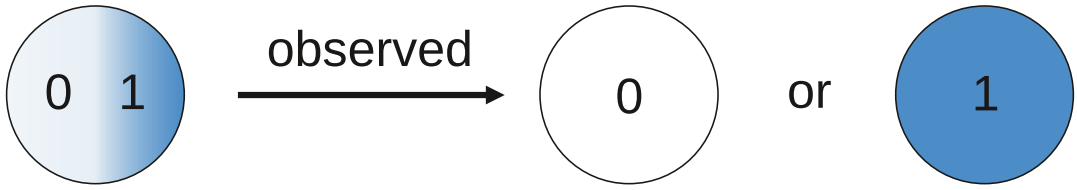


Figure 1.1: Concept of quantum superposition with qubit.

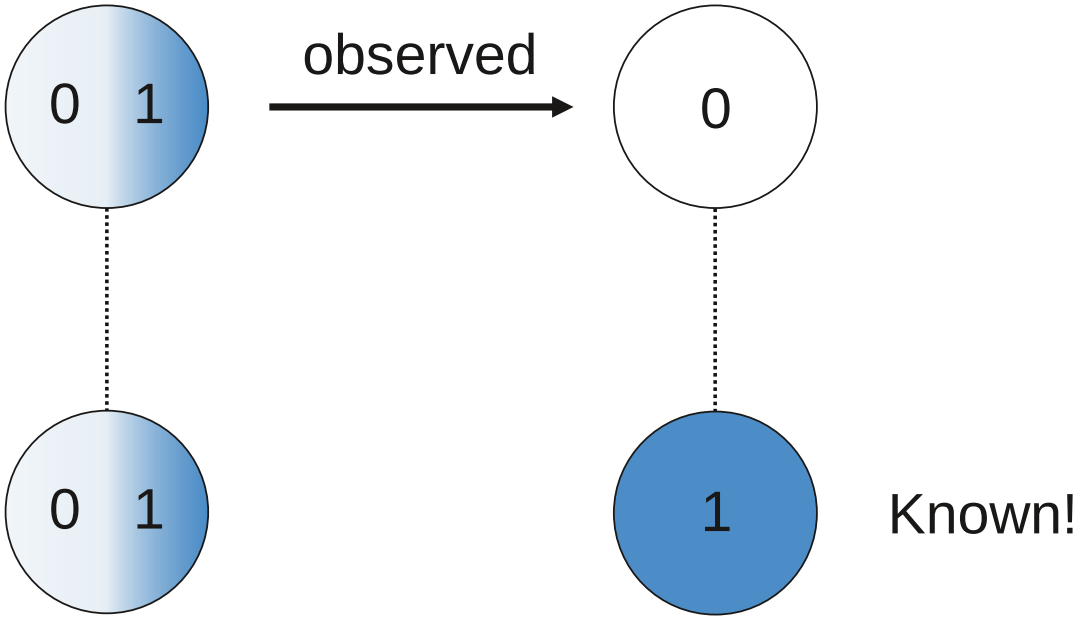


Figure 1.2: Concept of quantum entanglement with qubit.

ers can only process one data at a time. Fig. 1.1 shows the concept of the quantum superposition of a qubit. The state of qubit holds 0 and 1 simultaneously and is determined after being measured. The quantum entanglement states that if the quantum are entangled, there is a strong correlation in quantum. It means that if any entangled quantum is measured, the state of the other entangled quantum can be known. Fig. 1.2 shows the concept.

Similar to classical computers, QCs utilize quantum logic gates to realize the computation. Fig. 1.3 shows the concept of quantum computation utilizing quan-

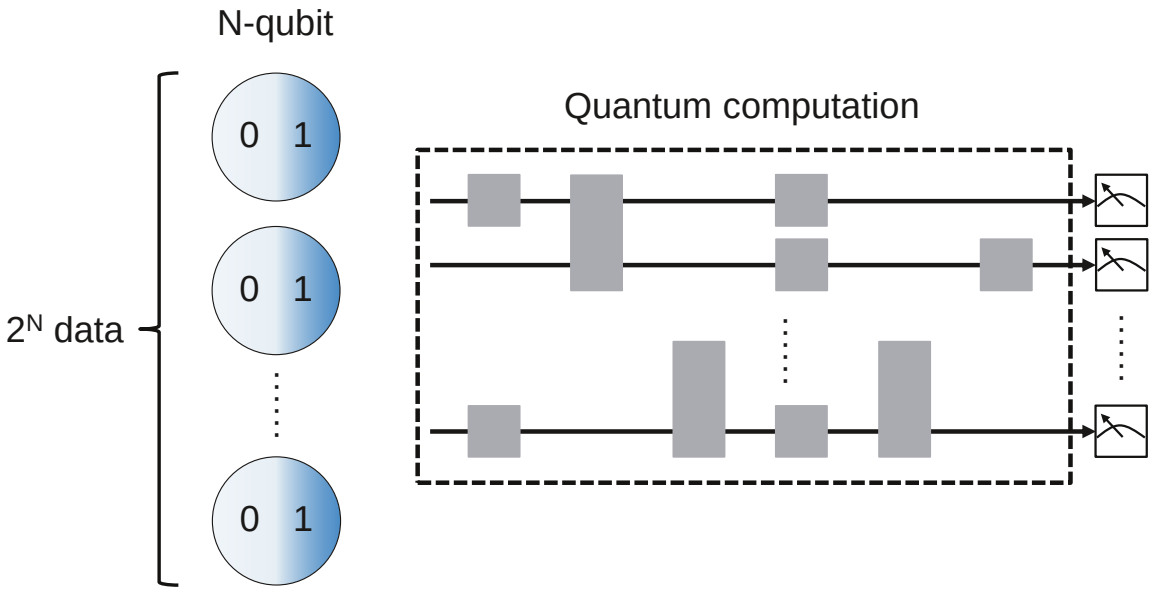


Figure 1.3: Quantum computation utilizing quantum logic gates.

tum logic gates. To illustrate the concept of quantum computation utilizing quantum logic gates, Fig. 1.3 also shows a 2^N qubits data and a set of the quantum logic gates. QCs calculate all of the data simultaneously and determine the answer in the end. Thanks to the quantum superposition, it makes parallel processing for all data is possible. Also, thanks to quantum entanglement, it is possible to determine the solution to the calculation instantly. Therefore, QCs can process data faster, even if the amount of data is huge.

Realizing the QCs still have many challenges, one is the noise. The qubits are extremely sensitive to the noise. This means that it is hard to keep the qubits state stable. As a result, the error rate of QCs is high, and it is hard to make them practical computers. Error detection and correction, therefore, are necessary for QCs. However, to achieve practical and reliable QCs, several thousands of qubits are needed to correct errors and reduce the error rate [1]. Fig. 1.4 shows the relation between the error rate and the number of qubits [3]. The error correction threshold is the error rate below 1%, and it needs at least several hundred qubits to achieve this level. Fault-tolerant QCs (FTQCs) are the true practical QCs that achieve a sufficiently low

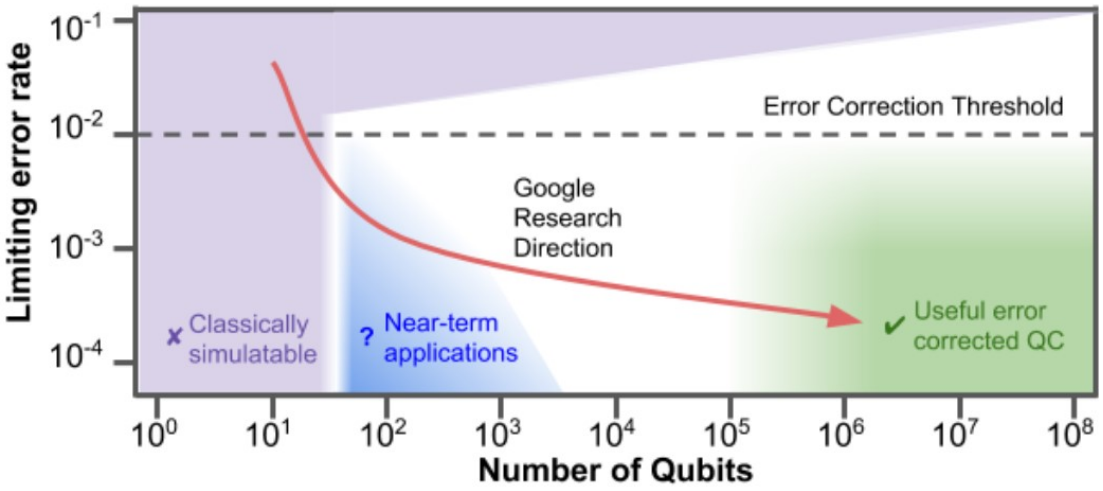


Figure 1.4: Error rate versus number of qubits [3].

error rate and general purpose. It requires at least several hundred thousand qubits.

Fig. 1.5 shows the relation between the number of qubits and the QCs implemented [1]. It is called Rose's law, similar to Moore's law for integrated circuits. It shows that the newest QC has only 433-qubit, just reaching the edge of the noisy intermediate-scale quantum computers (NISQ) while still far from the FTQCs [4–6]. Increasing the number of qubits is still the primary goal of achieving the FTQCs for general-purpose use. Therefore, scalable QCs are desired.

Another challenge is the coherence time of the qubits. The coherence time is how long the qubits can maintain their quantum state. In other words, it is the lifetime of the qubits. The longer coherence time of qubits is preferable to manipulating the qubits to realize quantum computation.

There are several techniques to realize qubits [7]. Besides the coherence time, error rate, and scalability, it is necessary to consider some other properties for achieving FTQCs. Some types of qubits may have to operate at cryogenic temperature to hold the quantum state and reduce the noise. A fast quantum gate operation time is required. Also, it is better to consider the integration with modern semiconductor techniques since this will benefit from matured complex systems.

Table 1.1 summarizes some representative types. Superconducting qubits are the

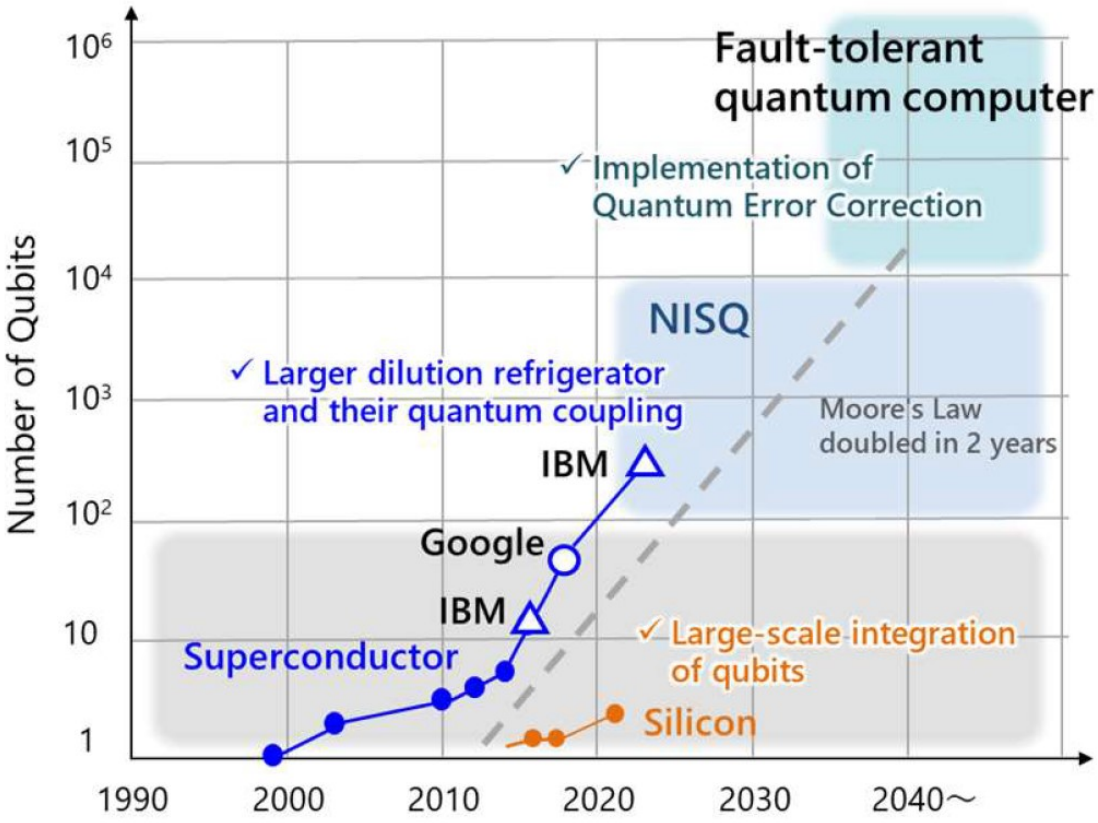


Figure 1.5: Number of qubits versus year [1].

most popular candidates for realizing FTQCs [8, 9]. The advantage of superconducting qubits is the good integration with semiconductor techniques. It helps increase the number of qubits and is easy to combine with mature systems that can realize complex and diverse functions. Also, the error rate of superconducting qubits could be below 1%. The disadvantage is that the coherence time of superconducting qubits is shorter than that of the other techniques. Also, to maintain the superconducting qubits stable, it is necessary to operate at cryogenic temperature, which is at several mK, almost absolute zero. Another popular technique is ion-trapped qubits [10, 11]. The ion-trapped qubits could also maintain a low error rate. Moreover, the coherence time is longer than the superconducting qubits. The disadvantage is that it is difficult to increase the number of qubits. The ion-trapped qubits also need to operate at cryogenic temperatures for stability. The neutral Atom has the potential to increase the number of qubits [12]. This shows good scalability, though

Table 1.1: Types of qubits.

Type of Qubits	Superconducting	Neutral Atom	trapped Ion	Spin in Semiconductor	Photon
Coherence Time	Short	Long	Long	Long	Short
Error Rate	Low	Low	Low	High	High
Scalability	Good	Good	Difficult	Good	Difficult
Integration with Semiconductor Techniques	Good	Difficult	Difficult	Good	Difficult
Cryogenic Operation	Yes	Yes	Yes	Yes	No
Gate Operation	Fast	Slow	Slow	Fast	Fast

more research is still needed to show its scalability. Also, it has a low error rate and long coherence time. Another issue is its slow gate operation time. The spin qubits could be implemented in semiconductors [13]. Therefore, it could take advantage of the mature semiconductor technology. It has the potential to integrate qubits highly. The error rate of the spin qubit is high. It is the bottleneck of the spin qubit as a good candidate for realizing FTQCs. The spin qubits also need to operate at cryogenic temperatures for stability. The photon qubits utilize optical technology to realize the qubit [14]. The advantage of the photon qubit is that it can operate at room temperature and is good with current fibre-optic communication while its error rate is still high. Among these popular types of qubits, superconducting qubits have many advantages and are considered the most promising candidates for realizing FTQCs at the time of writing this paper.

1.1.2 CMOS Control and Read-Out Circuits for Quantum Computers

Fig. 1.6 shows the state-of-art architecture of the quantum processor and control and read-out circuits. The Quantum processor, implemented with superconducting, neutral atom, ion-trapped, or spin qubits, must be placed in the refrigerator to maintain the cryogenic temperature. The qubits behaving as a microwave are controlled and read-outed utilizing a classical radio frequency (RF) transceiver and

receiver. For reading the qubits, analog-to-digital converters (ADCs) and other digital circuits, such as field-programmable gate array (FPGA), are after the RF front-end. The matured CMOS integrated circuits, which achieve various functions with high performance, can implement each block in the control and read-out circuits. Most of today's QCs place the control and read-out circuits at room temperature. Many cables link the quantum processor and the control and read-out circuits. Fig. 1.7 shows a quantum processor of an IBM 27-qubit quantum computer set at Shin-Kawasaki [15]. As shown, many cables are necessary to link the inside and outside of the refrigerator, from the room temperature ($T = 300\,K$) environment to the cryogenic temperature ($T = several\,mK$) environment. As a result, the thermal gradient is very steep. It works well when the number of qubits is small. However, it is a challenge when to increase the number of qubits since the number of cables also has to be increased. Due to the increasing number of cables and extremely steep thermal gradient, more and more heat flows into the refrigerator through the cables. It becomes difficult for the refrigerator to keep the cryogenic temperature. Therefore, the qubits can no longer maintain a stable state, and the number is limited. The increasing cables also cause the system to become complex, difficult to debug, and much more unreliable.

To address these issues, improving the operable temperature of the qubits is a good way. Another way is placing nowadays's control & read-out circuits closer to the quantum processor to avoid long cables and reduce the thermal gradient. Fig. 1.6 shows placing them in the cryogenic environment ($T = 4\,K$). By doing so, in the extreme case, it can utilize only one cable to transform data. The system will become concise and can keep the cryogenic temperature stable. Increasing the number of qubits is easier without considering the instability due to temperature variation. Therefore, increasing the number of qubits and making the scalable QCs realistic is easier.

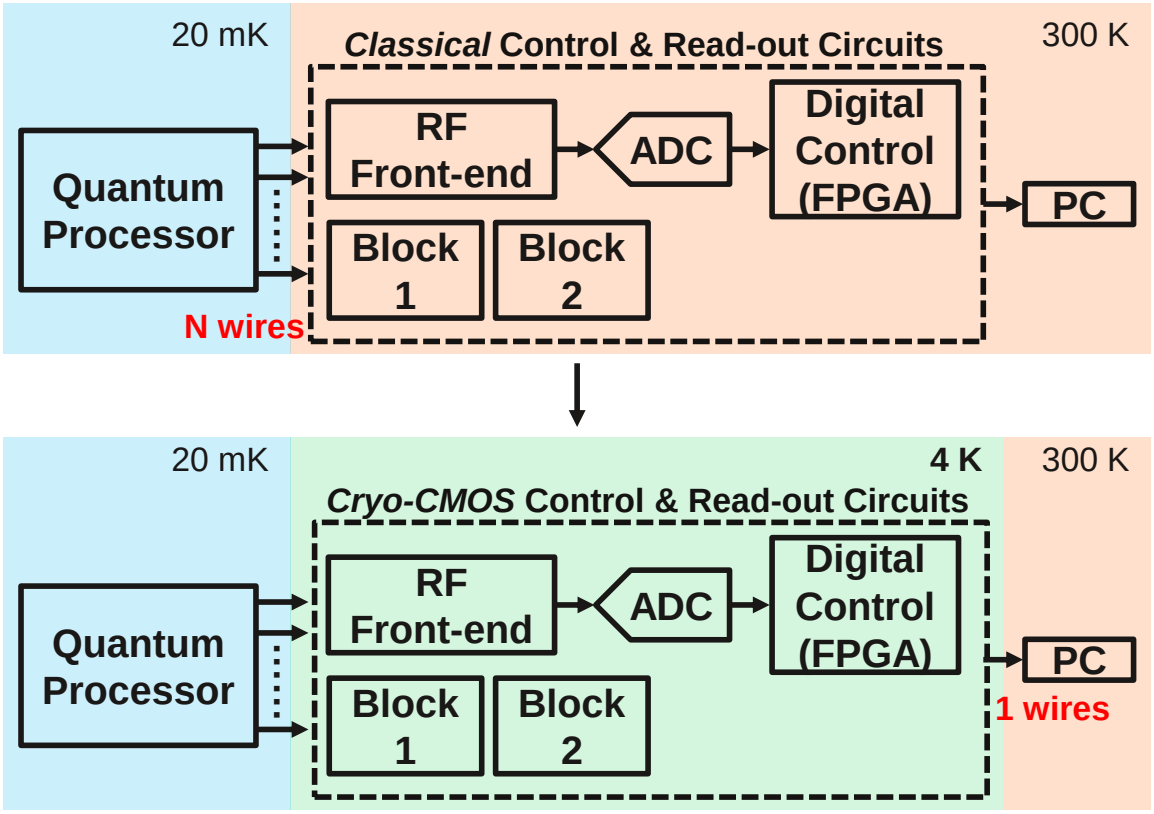


Figure 1.6: Control & read-out circuits for quantum processor.

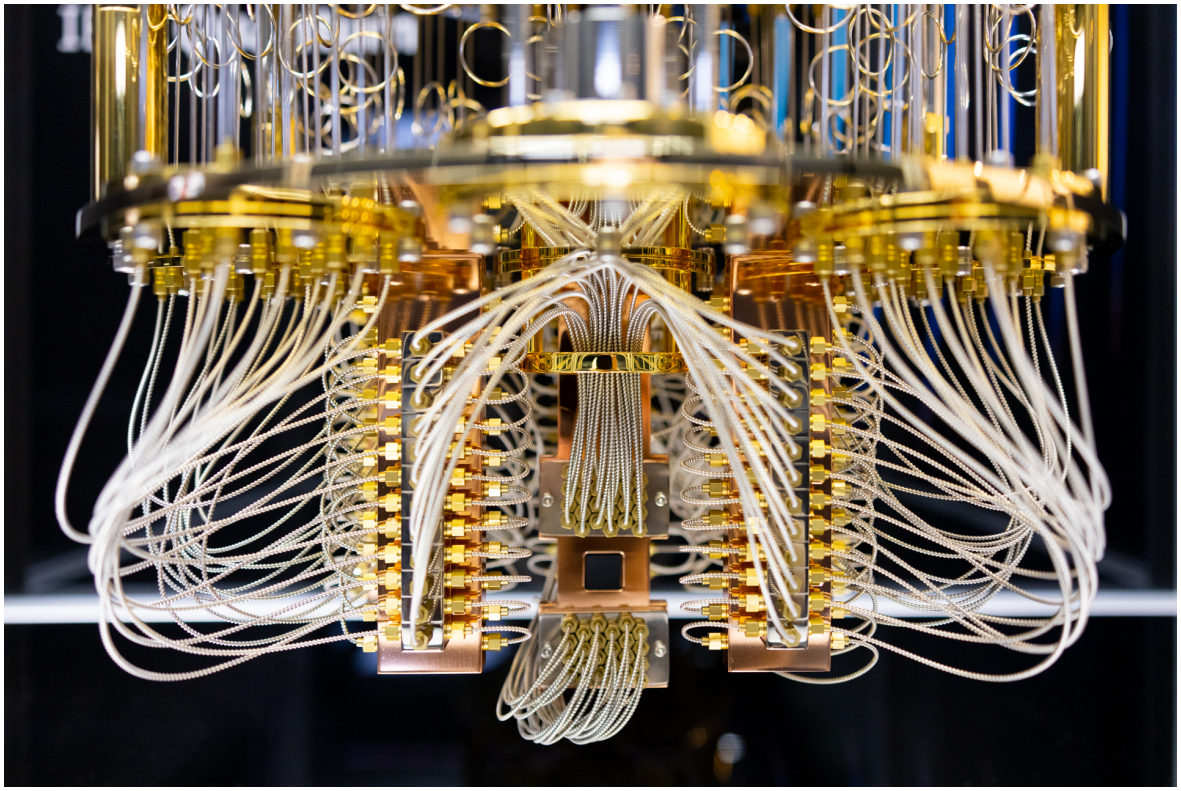


Figure 1.7: Architecture of a quantum processor of an IBM 27-qubit quantum computer [15].

1.2 Research Goal

This research focuses on the ADC for the qubits read-out circuits. As mentioned before, the qubits behave as microwave pulses. The control & read-out circuits adopt the frequency multiplexing technique to manipulate many more qubits to reduce the connecting cables and power. For instance, assuming the bandwidth of a qubit is 10 Mhz, another 10 Mhz is needed for other necessary operations. Therefore, the required sampling frequency of an ADC is about several tens MHz to several GHz, depending on the number of qubits. The cooling power of the refrigerator is limited. At $T = 4\,K$, the cooling power has to be below 1 W [16]. At $T = 4\,K$, the power consumption of the ADC has to be below about 1 mW since Many circuit blocks exist.

To achieve the specifications mentioned above, a cryogenic low-power and high-speed ADC is necessary. This research utilizes CMOS technology to achieve the ADC since it is the most mature technology that can achieve various high-performance complex-function circuits. Another important reason is that CMOS technology has excellent integration ability that can make scalable QCs easier to realize. In other words, it is a good candidate for realizing the FTQCs. From the viewpoint of reliability and scalability, this research aims to design a cryogenic ADC for integrating the control and read-out circuits in a chip. Also, CMOS technology is expected to integrate the quantum processor and the control & read-out circuits in one chip in the future. Therefore, the goal of this research is to design and realize a cryogenic low-power and high-speed ADC for FTQCs..

1.3 Thesis Organization

Fig. 1.8 shows the structure of the thesis. Each chapter is as follows.

Chapter 2 describes the characteristics of cryogenic CMOS devices. It focuses

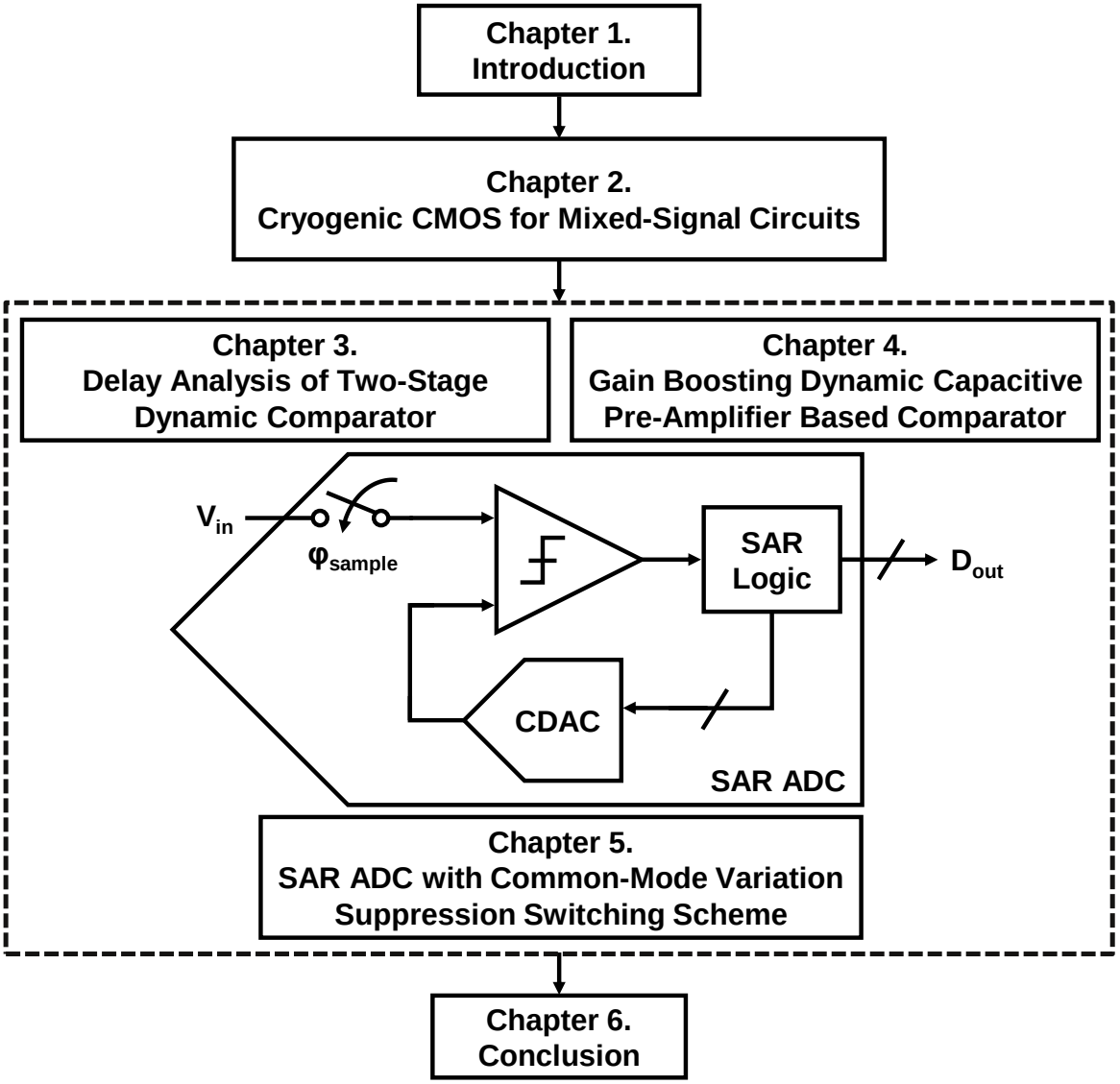


Figure 1.8: Structure of the thesis.

on how the characteristics change at cryogenic temperature and how it affects the circuit's operation from the circuit design perspective, especially the effect on analog and mixed-signal circuit design. The physical images are also given based on semiconductor physics to deepen the insight. This chapter also reviews the basic architecture of ADC and high-speed techniques. The speed issues of SAR ADC are discussed. It implies that the performance of the comparator is directly related to the performance of SAR ADC. Dynamic comparators are reviewed and discussed. Following that, the performance degradation of some previous switching schemes

of SAR ADC at cryogenic temperatures is addressed.

Chapter 3 describes the proposed high-speed and low-power two-stage dynamic comparator. The pre-amplifier adopts the dynamic bias technique to save power. Also, the inserted StrongARM latch increases the output voltage difference. The input pair of the proposed latch replaces the tail current source and suppresses the through current. The cross-coupled inverter pair and the auxiliary input pair enhance positive feedback and speed up the proposed latch. This chapter also describes the proposed delay model with an analysis of the proposed dynamic comparator. The delay analysis provides a deep understanding and a good intuition for circuit design.

Chapter 4 describes the proposed gain boosting dynamic capacitive pre-amplifier (DCA) based comparator. The proposed comparator achieves full-scale input range operation and common-mode variation insensitivity. It further improves the accuracy of the SAR ADC at cryogenic temperature. The DCA achieves low power consumption by utilizing the dynamic bias and current reuse techniques. Also, it adopted a cross-coupled pair to improve the speed by boosting the gain. A similar cross-coupled pair is also adopted for the proposed high-speed and low-power two-stage dynamic comparator described in Chapter 3.

Chapter 5 describes the proposed 10-bit 60-MS/s SAR ADC with a common-mode variation suppression (CMVS) switching scheme. Due to the mismatch of MOSFET increasing at cryogenic temperature, the accuracy of both the comparator and SAR ADC is degraded. To maintain good accuracy and low power consumption, the proposed CMVS switching scheme narrows the common-mode variation to 16.6% V_{DD} and reduces about 92% of energy consumption compared to the conventional scheme. Also, the dynamic common-mode voltage of the proposed CMVS switching scheme increases during conversion. It solves the increased V_{th} issue at cryogenic temperature while making the comparator operate at the best FoM.

Chapter 6 gives the conclusion and presents future work.

Chapter 2

Cryogenic CMOS for Mixed-Signal Circuits

The characteristics of CMOS devices change with temperature. The commercial CMOS devices usually operate in temperatures from $-40°C$ to $120°C$. On the other hand, the CMOS devices operating at the cryogenic temperature are called cryogenic CMOS (cryo-CMOS). In this research, it means the temperature at $T = 4\,K$. This chapter describes the characteristics of cryo-CMOS, including the increase of threshold voltage V_{th}, the increase of mismatch, and the increase of mismatch, and focuses on those effects on circuit design.

After understanding the characteristics of cryo-CMOS, a brief overview of successive approximation register (SAR) analog-to-digital converter (ADC) is described, primarily focusing on increasing the conversion speed. The comparator adopted in SAR ADC greatly affects the performance. The overview of the dynamic comparator follows, including the Strong-ARM latch-type comparator, the double-tail comparator, and the dynamic bias latch-type comparator, etc. This chapter also describes the performance of the prior art from the perspective of power consumption and comparison speed. This implies the design challenges of a high-speed and low-power dynamic comparator.

The capacitive digital-to-analog converter (CDAC) adopted in the SAR ADC is another important block affecting the performance of SAR ADC. The switch schemes of CDAC are discussed from the perspective of power consumption, the effect of mismatch, and the effect on the performance of the comparator.

Through this chapter, the whole picture of this research becomes clear.

2.1 Cryogenic CMOS

Ccryo-CMOS is a CMOS technology that operates at cryogenic temperature. Cryo-CMOS's characteristics are different from those at room temperature, including the increase of threshold voltage V_{th}, the increase of mismatch, the increase of mismatch, and so on.

Fig. 2.1 shows the measured results of the relation between threshold voltage V_{th} and drain current I_D of NMOS at $T = 300\,K$ and $4\,K$. It shows that the threshold voltage V_{th} increases at $T = 4\,K$. Previous researches also show the increased threshold voltage V_{th} at $T = 4\,K$ [17, 18].

To understand the physical phenomenon of increased V_{th}, the energy band of n-type MOSFET (NMOS) are shown in Fig. 2.2. As temperature decreases, the band gap increases. The thermal energy that the carrier needs to excite from the valence band to the conduction band also decreases, which is called the freeze-out effect. The Fermi energy also changes to a lower position. This causes the Fermi potential at cryogenic temperature to become large [19].

The expression of Fermi potential φ_f is [17]

$$\varphi_f = \frac{kT}{q} \ln \frac{N_A}{n_i} - \frac{kT}{q} \ln \frac{1 + \sqrt{1 + 4\alpha N_A / n_i}}{2} \tag{2.1}$$

where k. T, q, N_A, n_i, and α are Boltzmann's constant, temperature, electron charge, acceptors' doped concentration, intrinsic carrier concentration, and incomplete ion-

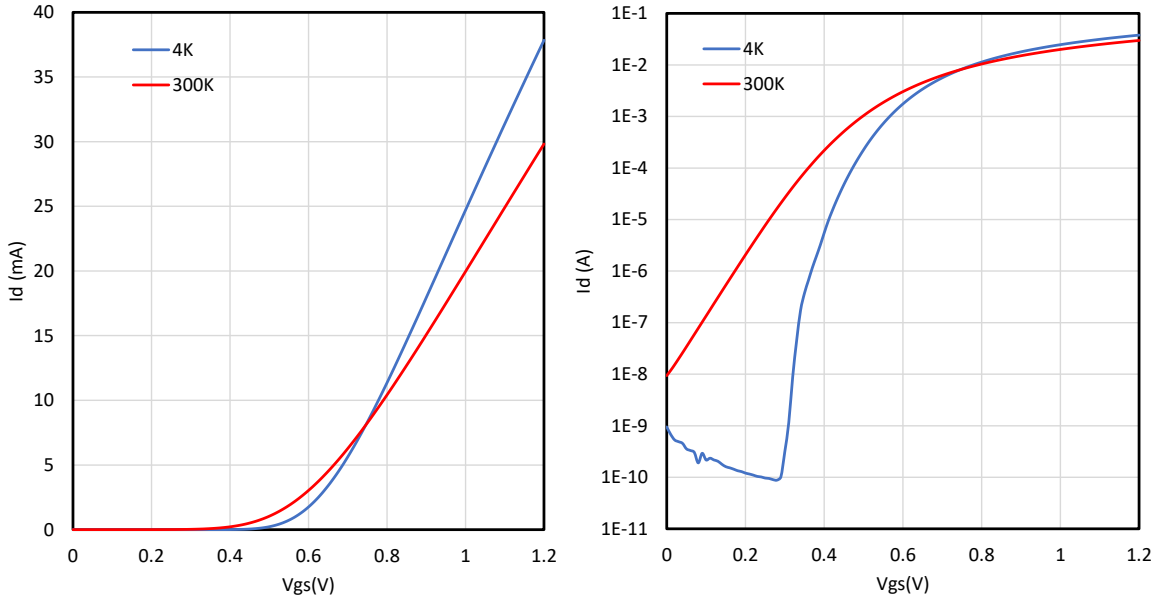


Figure 2.1: I_d-V_{GS} at $T = 300\,K$ and $4\,K$.

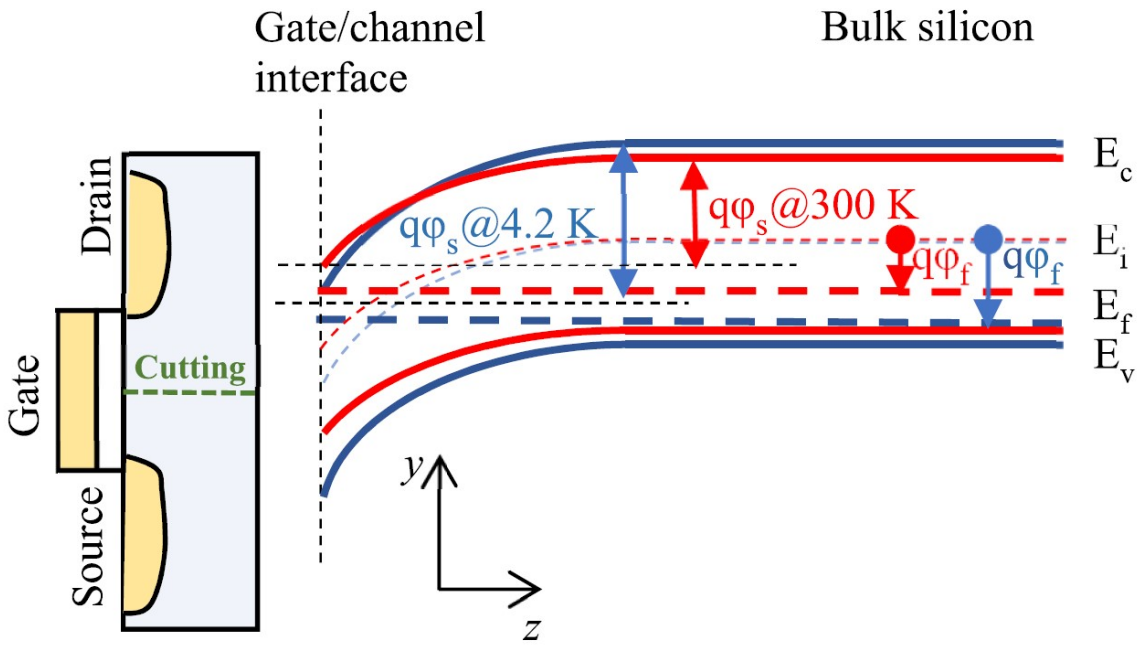


Figure 2.2: Energy band of NMOS at $T = 300\,K$ and $4\,K$ [19].

ization parameter. As 2.1 shown, φ_f increases as T decreases ,which shows the same result.

The energy band shown in Fig. 2.2 is the n-type channel just formed under the gate, which means that the p-type substrate inverses to the n-type. In that case, the surface potential is equal to double the Fermi potential as

$$\varphi_s = 2\varphi_f \tag{2.2}$$

The φ_s also increases due to the φ_f increases at cryogenic temperature. This indicates that the threshold voltage V_{th} increases at cryogenic temperature.

The expression of V_{th} is [20]

$$V_{th} = -\frac{E_g}{2q} + \varphi_f + \frac{\sqrt{2\varepsilon_{Si} q N_A (2\varphi_f)}}{C_{ox}} \tag{2.3}$$

where $E_g (= E_c - E_v)$, ε_{Si} and C_{ox} are energy bandgap, silicon permittivity, and oxide capacitance, respectively. As mentioned before, the band gap E_g and the Fermi voltage φ_f increases at cryogenic temperature. Therefore, the threshold voltage V_{th} increases at cryogenic temperature ($T = 4\,K$).

Fig. 2.3 shows the measured $I_D - V_{DS}$ curve of NMOS at $T = 300\,K$ and $4\,K$. It shows that the drain current I_D increases at $T = 4\,K$. The increased current is related to the mobility of the carrier.

The effective mobility is expressed as

$$\mu_{eff}(T) = \frac{\mu_0(T)}{\sqrt{1 + E^2/[v_{sat}(T)/\mu_0(T)]^2}} \tag{2.4}$$

where E and v_{sat} are the electric field and saturation velocity, respectively. The μ_0 is

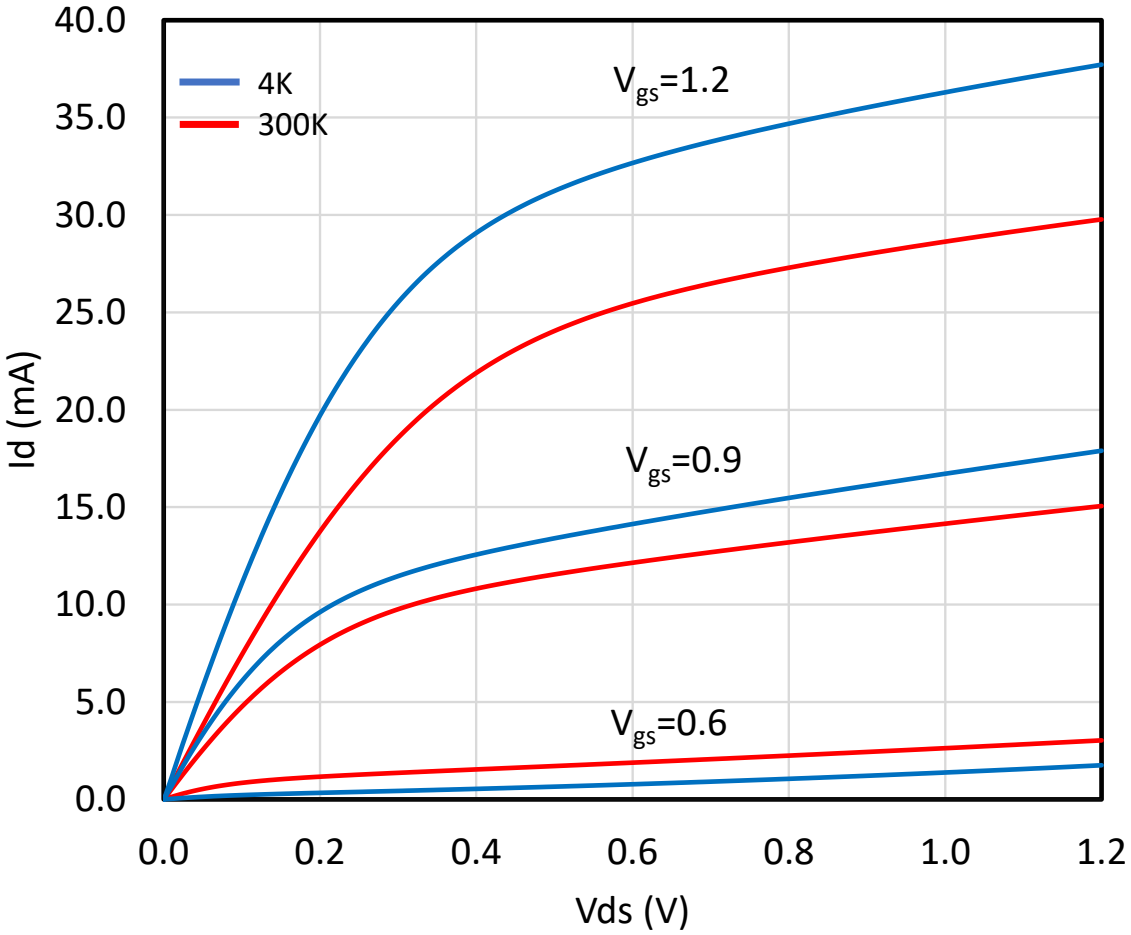


Figure 2.3: I_d-V_{DS} at $T = 300\,K$ and $T = 4\,K$.

extracted from the I_D-V_G curve and is expressed as [21]

$$\mu_0(T) = \frac{Gm(max)L}{C_{ox}V_dW} \tag{2.5}$$

where $G_m = dI_d/dV_g$. [19] shows that the G_m and μ_0 increase with the decrease in temperature. The μ_0 is related to the channel length and width. As the temperature decreases, the phonon scattering decreases for long and wide channels. On the other hand, the Coulomb scattering is unignored for short channel length. The relation of the Coulomb scattering and Substrate impurity concentration inversion layer carrier

concentration shown below:

$$\mu_{Coulomb} \propto {N_{sub}}^{-1} N_{inv} \tag{2.6}$$

A higher impurity will decrease mobility μ_0. From the above discussion, the μ_0 and μ_{eff} have a relatively low increase for short-channel devices at cryogenic temperature.

The results of [19] show that the channel length has a great effect on mobility while the channel width does not. To explain this, the total resistance of NMOS is expressed as [22]

$$R_{total} \equiv \frac{V_d}{I_d} = R_{ch}(L - \Delta L) + R_{ds} \tag{2.7}$$

where R_{ch} and R_{ds} are intrinsic channel resistance per unit channel length and serious resistance. The R_{ch} is inversely proportional to mobility and decreases as the temperature decreases. This shows the R_{total} decreases at cryogenic temperature. At the same V_d, the current increase is shown in (2.7).

Fig. 2.1 also shows the leakage current I_{off} also reduced at cryogenic temperature. [19] shows the decrease on I_{off} is dominated by the subthreshold leakage and Gate-Induced-Drain-Leakage (GIDL) effect. The subthreshold leakage is affected by the amount of carriers and ionized acceptors in the channel. This amount is lower at $T = 4\,K$ compared to that at $T = 300\,K$ due to the freeze-out effect. The GIDL effect occurs when the gate-drain voltage V_{GD} becomes negative and has an inverse bias. It is related to the band-to-band tunnelling (BTBT) process. The probability of the BTBT process is expressed as [23]

$$P_T = \exp(-\pi W_T \sqrt{m^* E_g}/2^{1.5}\hbar) \tag{2.8}$$

where m^* and W_T are the average effective mass of tunneling electrons and tunneling distance, respectively. The W_T becomes large due to the increased E_g as shown

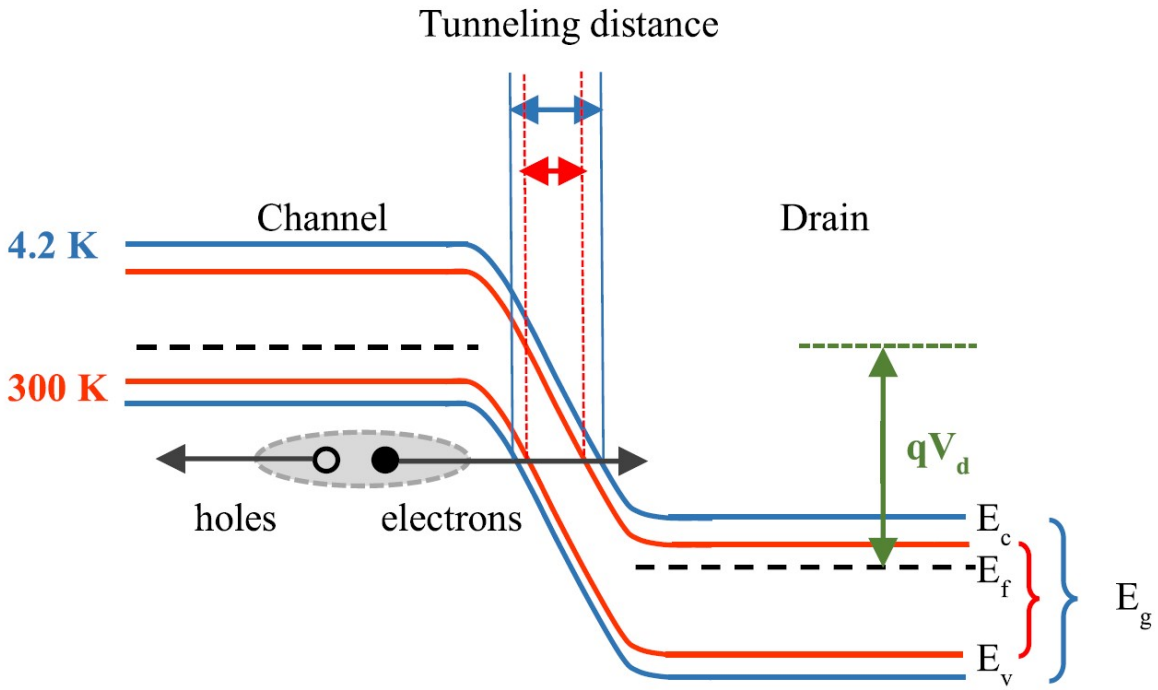


Figure 2.4: The BTBT process of NMOS [19].

in Fig. 2.4. This reduces the BTBT process, and thus, the current due to the GIDL effect also decreases.

An increase in the mismatch of MOSFET has also been reported. The current mismatch is dominant, while the threshold voltage mismatch has less effect and is negligible. As mentioned above, the mobility increase causes the drain current to increase. This also increases the scattering, which means the mobility fluctuations. The measured results show that the mobility fluctuations are more affected by temperature change. The drain current mismatch increases as the gate-source voltage V_{GS} decreases. At $T = 4\,K$, the increased threshold voltage V_{th} make the effective V_{GS} becomes smaller. Therefore, the drain current mismatch increases.

2.2 Cryogenic SAR ADC

Reading qubits demands an ADC with a medium to high conversion speed, medium resolution, and extremely low power consumption. Fig. 2.5 shows the power con-

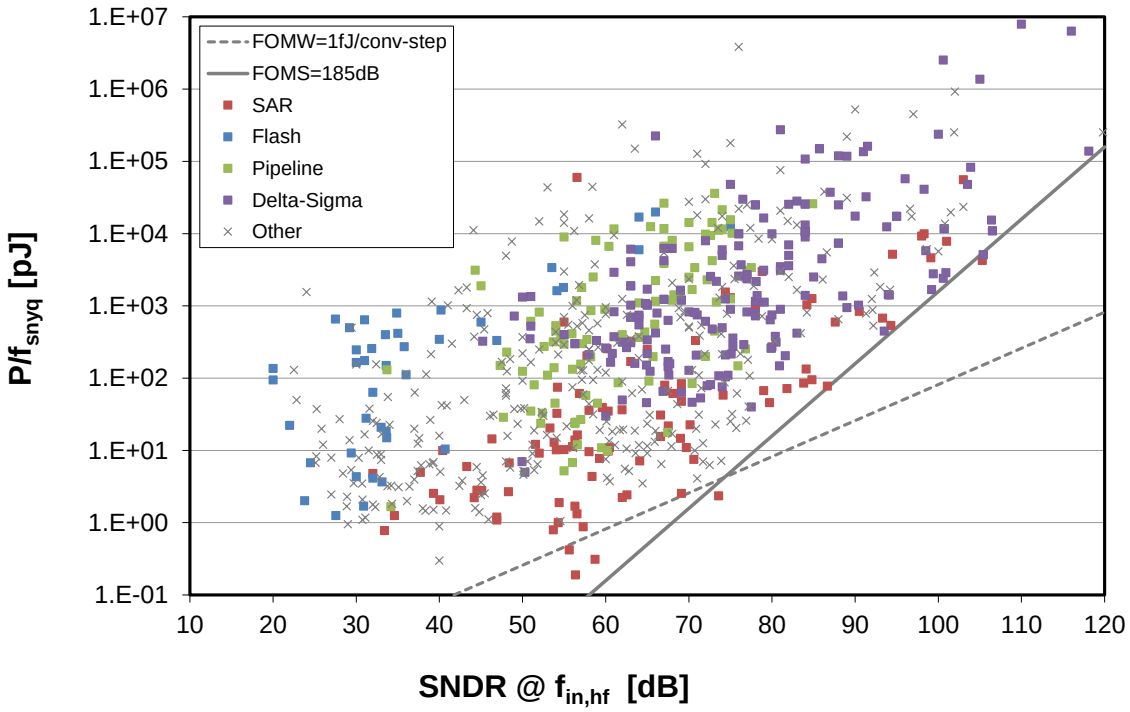


Figure 2.5: Power consumption per conversion versus SNDR [24].

sumption per conversion versus the signal-to-noise-and-distortion ratio (SNDR) using the published data at the ISSCC and VLSI Symposium in 1997-2024 [24]. Four basic architectures: flash, pipeline, SAR, and delta-sigma, are highlighted. Except for delta-sigma, the others are the Nyquist rate ADC. It indicates that the SAR ADC has the best power efficiency while at medium resolution, shown in terms of SNDR. On the other hand, the pipeline ADC, flash ADC, and delta-sigma ADC have worse power efficiency.

The SAR ADC is a good candidate. Its high power efficiency and digital-intensive architecture have made it the most popular ADC in recent times [25–28]. It is widely utilized in many applications, such as wearable sensor systems, wireless communication networks, and more [29, 30]. The cryo-CMOS SAR ADC can be applied to quantum computers, space exploration and particle experiments [31]. The performance of SAR ADC improves with the advancement of CMOS technology thanks to the utilization of digital circuits to implement the successive approximation algo-

rithm.

Fig. 2.6 shows the FoM versus the sampling frequency. The Nyquist rate ADCs are highlighted. It shows that one of the weaknesses of SAR ADC is the conversion speed. Utilizing the pipeline ADC or flash ADC for high-speed applications is more suitable. It also indicates that the SAR ADC is at the lowest FoM region, which again indicates its power efficiency.

Considering the speed of ADC, Fig. 2.7 highlights the high-speed Nyquist rate ADC architectures. Time-interleaved (TI) technique and hybrid ADC architecture are utilized to improve speed and performance [32–35]. Flash ADC and TI flash ADC achieve high sampling rates, while the FoM is the worst. Pipeline ADC is suitable for high-speed applications, and the power efficiency is better than flash ADC and TI flash ADC. To further improve the power efficiency of pipeline ADC, pipelined-SAR hybrid architecture is a practical approach [36–39]. It shows that the FoM of pipelined-SAR ADC is better than that of pipeline ADC and is competitive with SAR ADC. The sampling rate of the pipelined-SAR ADC is still slower than the flash ADC and TI flash ADC. The TI SAR ADC achieves several GHz ~ several tens GHz sampling rates at the lowest FoM. Therefore, as previous research has proved [40–50], the TI SAR ADC is a promising architecture for achieving a low-power and high-speed ADC.

Recently, the cryo-CMOS TI ADC for reading qubits has been developed [51–53]. However, the performance is not as good as those at RT. The TI ADC consist of multiple sub-ADCs (single-channel ADC) forming multichannel parallel architecture [30, 54, 55] as shown in Fig. 2.8 (an example here is a 4-channels 10-bit TI ADC). As the number of channels increases for high-speed operation, the effort made on the mismatch calibration between each single-channel ADC also increase. The overhead of mismatch calibration further degrades the performance. TI ADC usually utilizes SAR ADC as one channel because of its power efficiency. As single-channel SAR ADC significantly determines the performance of the TI ADC, any improve-

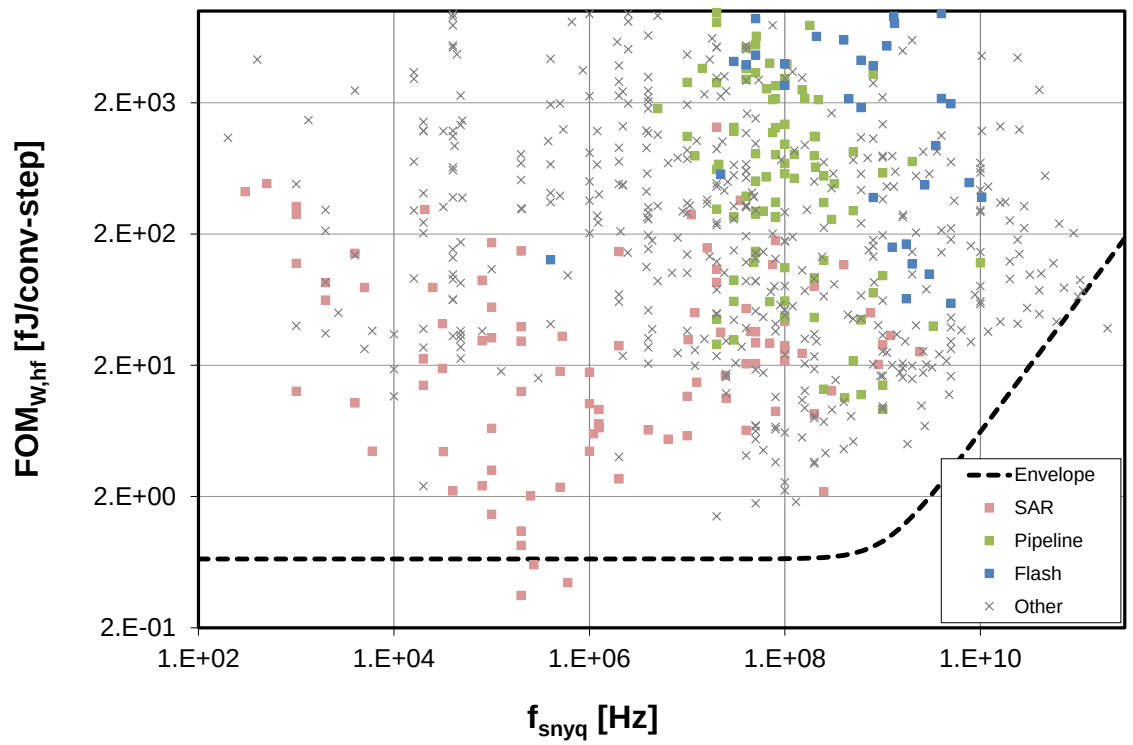


Figure 2.6: FoM versus sampling frequency for Nyquist rate ADC architectures [24].

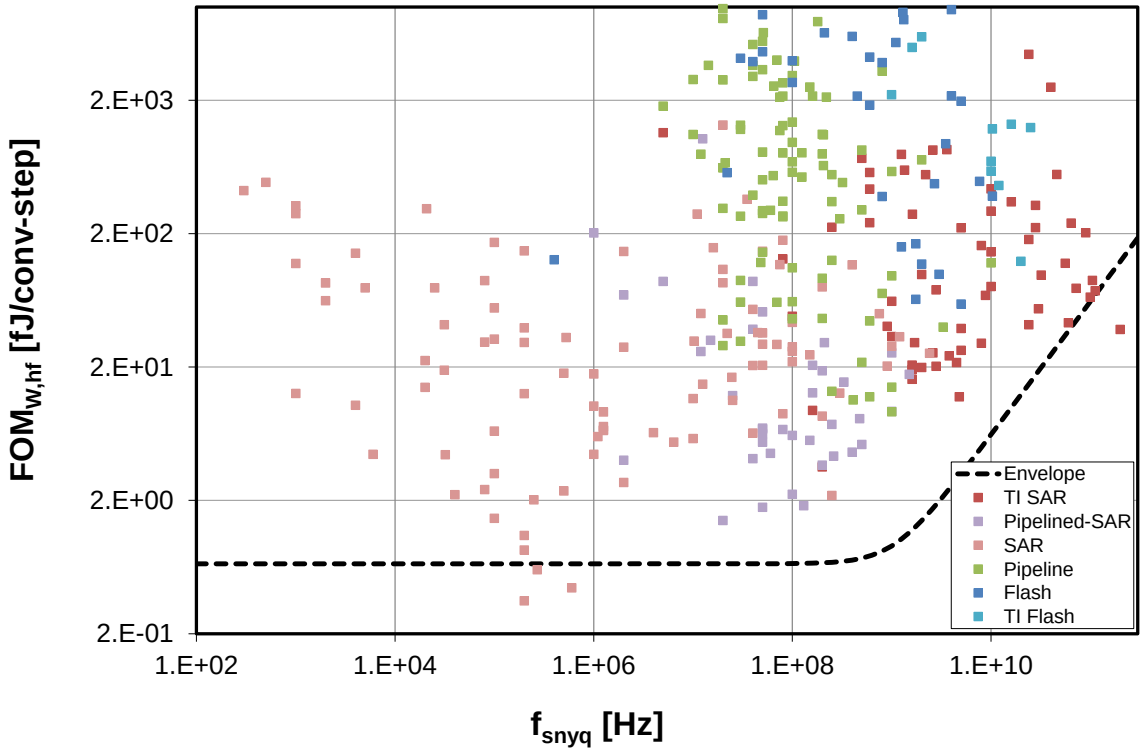


Figure 2.7: FoM versus sampling frequency for high-speed Nyquist rate single-channel ADC architectures [24].

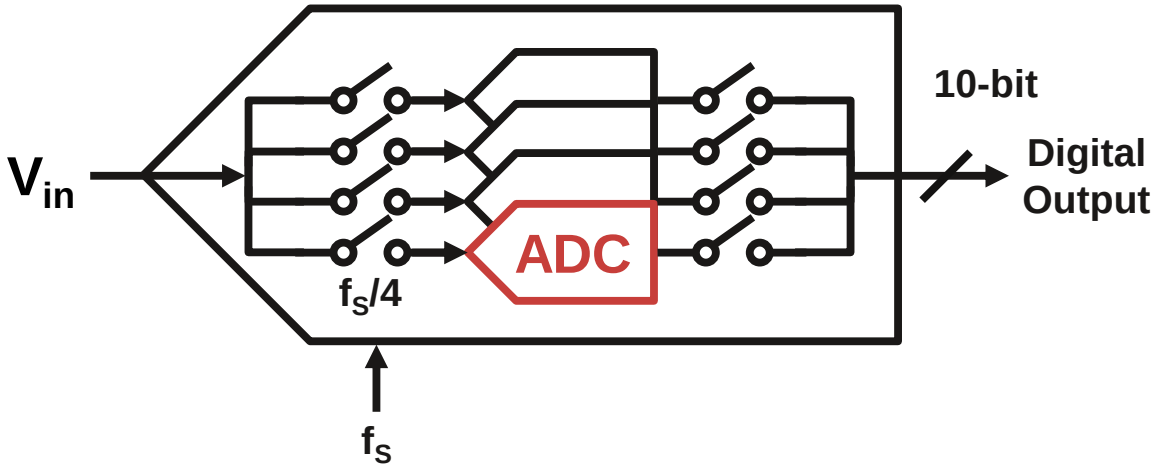


Figure 2.8: Time-interleaved ADC with 4-channels.

ments in its performance, particularly in terms of power consumption and conversion speed, can lead to significant benefits in the overall performance of the TI ADC. This approach can also relieve the requirement for increasing channels or mismatch calibration.

The speed limitation of SAR ADC is because of the nature of the successive approximation. Previous research has made much effort to improve the speed of the SAR ADC, such as multiple bits per conversion [56, 57], loop-unrolled [58–60], and so on [61–64]. Fig. 2.9 shows the architecture of the SAR ADC. It is composed of a sampling switch, a comparator, a CDAC, and a SAR logic. As shown in Fig. 2.9, a SAR ADC needs one cycle to convert 1-bit, and thus, N-bit needs an N-cycle conversion. The critical cycle of a SAR ADC is expressed as [60]

$$t_{cycle} = t_{comparator} + t_{SAR\,logic} + t_{CDAC}. \tag{2.9}$$

The speed of the digital part of the SAR ADC improves with the improved CMOS technology. The settling speed of the CDAC is determined by the resolution, the switching method, and kT/C noise. It can be improved by reducing the capacitance, such as top-plate sampling, while the kT/C noise still restricts the possible improve-

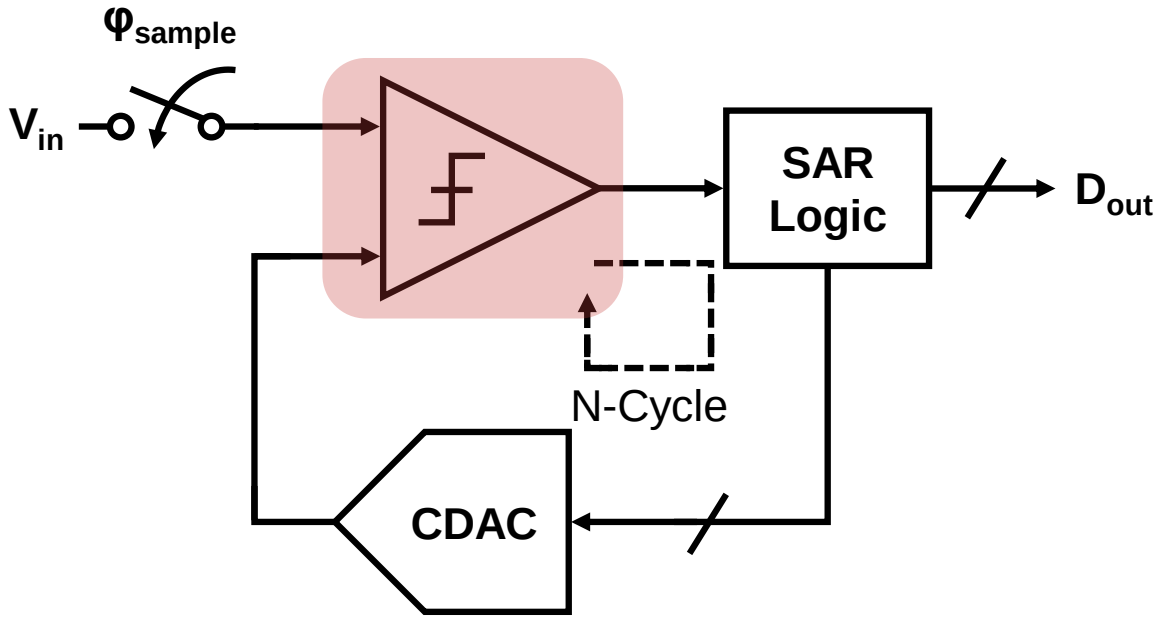


Figure 2.9: SAR ADC Arichitecture.

ment [34]. To inherently realize a low-power and high-speed ADC, a straightforward approach is to reduce the speed and power consumption of the comparator.

2.2.1 Dynamic Comparator

Dynamic comparators, also called regenerative comparators, are the widely utilized core block for ADC and determine the performance of ADC. A high-performance dynamic comparator is desired to improve the performance of SAR ADC.

The StrongARM latch-type comparator [65] is one of the most popular dynamic comparators since it has almost no static power consumption. Its degree of freedom in design is limited due to it being a single-stage architecture. Also, it is not suitable for low supply voltage due to the narrow headroom margin.

Two-stage dynamic comparators consist of the pre-amplifier stage (1^{st} stage) and the latch stage (2^{nd} stage). Separating each stage is more suitable for low supply voltage because of the higher headroom margin. Isolation between the pre-amplifier and the latch provides better amplification and reduces the kickback noise [66].

Also, it allows the input common-mode voltage to be up to near supply voltage V_{DD} since there is no need to consider the gate-source voltage V_{GS} of the latch like the StrongARM latch-type comparator. Therefore, the two-stage dynamic comparator has a greater degree of freedom in design.

The double-tail comparator is a well-known high-speed two-stage comparator. The speed of the latch improves thanks to separating the pre-amplifier and the latch. It suffers from high power consumption due to the leakage current [66–68]. Also, the input pair of the latch starts from the linear region since the initial state is reset to GND. It effectively reduces the gain of the latch, and, thus, the speed degrades. [69] addressed this issue. However, due to the input pair inserted in the middle of the inverter structure in the latch, the gain of the latch is finally degraded, and thus, the speed degrades.

Considering the power consumption, the double-tail comparator or the StrongARm comparator fully discharges the capacitor of the pre-amplifier and consumes energy $2 \cdot C_p \cdot {V_{DD}}^2$. A bi-directional pre-amplifier is proposed to save energy. It only consumes $C_p \cdot {V_{DD}}^2$ by combining the reset and half amplification phases [70]. Due to the complex timing control, the overhead of the digital control circuits is required.

The dynamic bias comparator has attracted much attention recently since it achieves low power consumption [71]. The dynamic bias technique saves power by partial discharging the capacitor of the pre-amplifier. It causes current degradation during the amplification phase, and thus the speed decreases. To alleviate these issues, a high-speed and low-power two-stage regeneration enhancement dynamic comparator was proposed previously [67, 68]. The regeneration enhancement comparator adopts the dynamic bias technique to save power while inserting the StrongArm latch into the pre-amplifier to enhance the amplification [67, 68]. Also, a low-power regenerative latch was proposed to suppress the through current by replacing the tail current source with an input pair. However, the comparators mentioned above

Table 2.1: Comparison of pre-amplifier architecture.

Pre-Amplifier Architecture	Convention	Bi-direction	Dynamic Bias	FIA	CSPC
Speed	Fast	Medium	Slow	Slow	Medium
Area Efficiency	Good	Fair	Fair	Poor	Poor
Insensitivity of Common-Mode Variation	No	No	No	Yes	Yes
Current Reuse	No	No	No	Yes	Yes

suffer from the common-mode variation sensitivity. Also, they could not operate in a wide input range. These further degrade the performance when operating at $T = 4\,K$ [68].

Another comparator architecture that attracted much attention is the comparator with a floating inverter pre-amplifier (FIA) [72]. It not only saves power consumption but also features common-mode variation insensitivity. The common-mode variation insensitivity is achieved thanks to the reservoir capacitor, which serves as the power supply for the pre-amplifier. Utilizing the reservoir capacitor forms an isolated voltage domain and, therefore, forces the output common-mode voltage of the pre-amplifier to be relatively constant. The details of the proposed comparator will be explained in Chapter 4. The comparator with FIA still suffers a speed decrease due to the current degradation, which is similar to the dynamic bias technique. It also could not operate in a wide input range [73]. The dynamic capacitive CMOS split pre-amplifier comparator (CSPC) [73] remains the advantage of the comparator with FIA. Also, it features a wide input range operation thanks to a larger drain-source voltage V_{DS}. However, it still suffers a speed decrease for the same reason. A high-speed and low-power dynamic comparator utilized in SAR ADC is required to implement high-performance cryo-CMOS circuits for reading qubits and achieving the FTQCs.

Table. 2.1 summarized the pre-amplifier mentioned above.

2.2.2 Switching Schemes of the Capacitive Digital-to-Analog Converter

A CDAC serves as the hold capacitor for sampling and the reference voltage generator in the SAR ADC. Many energy-efficient switching schemes have been proposed to reduce the switching energy of CDAC. The monotonic switching scheme [74] is the most famous. The average switching energy was reduced by about 81% compared to the conventional switching scheme [75]. The bidirectional single-side [76], tri-level alternative [77], adaptive-reset [78], and MSB-block switching scheme [79] reduced by about 86%, 86%, 90%, and 94% average switching energy compared to the conventional switching scheme, respectively.

The input common-mode voltage determines the performance of the comparator, including energy, delay, noise, and offset [80], as shown in Fig. 2.10. During successive approximation processes, the CDAC generates a new reference voltage after a comparison is completed, and the input common-mode voltage V_{CM} may change every time [74, 76, 77]. As a result, this may cause the input common-mode voltage variation. This variation can significantly impact the performance of the comparator and SAR ADC. The comparator typically achieves the best performance at the input common-mode voltage, around half V_{DD} [67, 68, 80]. To optimize the performance of SAR ADC, it is better to design the switching scheme operating around half V_{DD}. At $T = 4\,K$, the increased V_{th} further degrades the performance, especially when the input common-mode voltage is around half V_{DD}. Also, the increased mismatch degrades the accuracy. Those switching schemes mentioned before suffer from input common-mode voltage variation except for monotonic and adaptive-reset schemes. However, the last two still consume a lot of energy, especially the monotonic switching scheme. Therefore, a switching scheme and a comparator addressing these cryo-CMOS issues are required to design a low-power SAR ADC that achieves the same or even higher performance at RT.

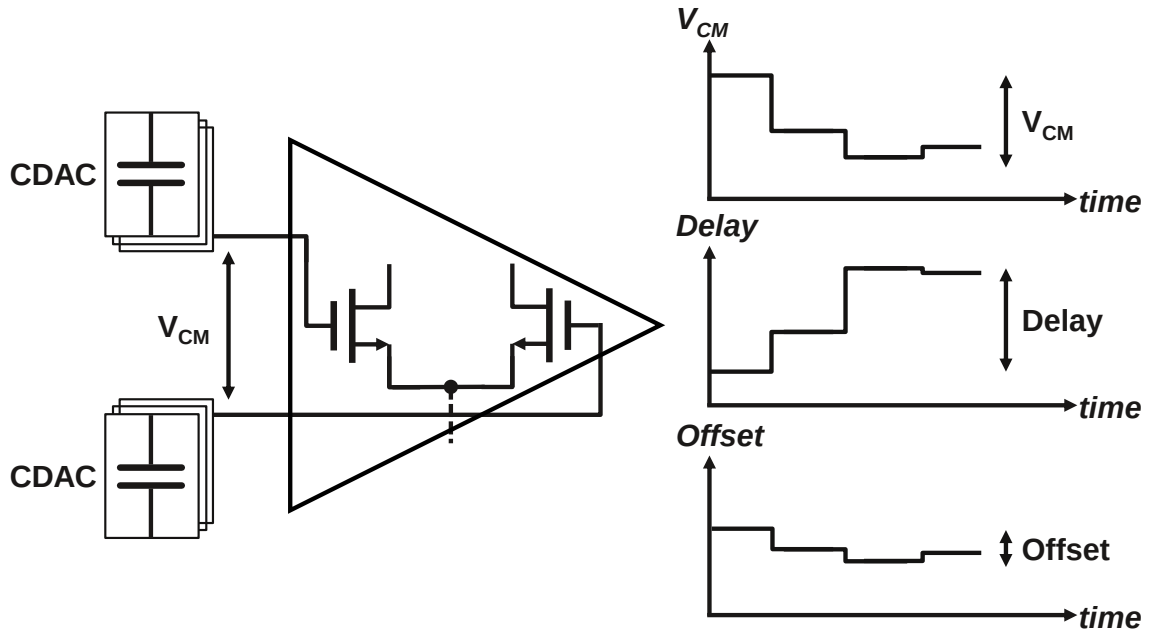


Figure 2.10: Effect of common-mode voltage variation on comparators.

2.3 Conclusion

This chapter briefly summarised the characteristics of Cryogenic CMOS and presented the measurement results at $T = 300\,K$ and $4\,K$, showing the difference. Based on these characteristics, the challenges and issues are addressed from the circuit design perspective. Following that, a brief summary of the speed limitation issue of SAR ADC is discussed. It shows the requirement for a high-speed and low-power dynamic comparator. The performance of the dynamic comparator degrades due to the increased V_{th}. This chapter also briefly summarised the switch schemes of CDAC. It is important to note that the changed characteristics of Cryogenic CMOS affect the circuits' performance, and the designs for cryogenic temperature are required.

Chapter 3

Delay Analysis of Two-Stage Dynamic Comparator

Dynamic comparators are well analyzed including noise, offset, and delay [65, 81–88]. Most analyses focused on the StrongArm latch-type comparator. Only a few are focused on both the StrongArm latch-type comparator and the two-stage dynamic comparator. Dynamic bias, also known as charge steering, is a power-saving and effective technique that is easy to implement. It is analyzed in [71]. However, the delay time of the two-stage dynamic comparator adopting the dynamic bias has not been analyzed.

In this chapter, a high-speed and low-power two-stage dynamic comparator with regeneration enhancement and through current suppression techniques are proposed. The pre-amplifier adopts the dynamic bias technique to save power. To increase the output voltage difference of the pre-amplifier, the StrongARM latch is inserted. The proposed latch keeps a cross-coupled inverter to ensure good positive feedback. The input pair of the proposed latch replaces the tail current source to suppress the through current. The auxiliary input pair enhances the gain and positive feedback to speed up the latch. Following the details of the design of the proposed comparator, the delay analysis of the proposed comparator is described. The delay

analysis also shows the delay time of the pre-amplifier adopting the dynamic bias technique.

3.1 Regeneration Enhancement and Through Current Suppression Comparator

As mentioned above, many two-stage dynamic comparators are proposed to address some issues. Here, the high power consumption issue of the double-tail dynamic comparator and the speed degradation issue of the dynamic bias comparator are addressed.

The double-tail dynamic comparator shown in Fig. 3.1 [66] is a two-stage comparator designed for high-speed operation. Separated tail current sources allow for independent determination of the speed of each stage. As shown in Fig. 3.1, the direct current from the supply voltage V_{DD} to the ground GND causes the through current (Fig. 3.2) and, thus, higher power consumption before the regeneration is completed. This is a severe problem, especially when the input voltage is small. The smaller the input voltage, the more time the through-current flows. Therefore, the power consumption increases.

The dynamic bias comparator shown in Fig. 3.3 [71] has attracted much attention recently because of its low power consumption. By inserting a capacitor under the tail current source of the pre-amplifier stage, the discharging current of the drain node OP and ON of input pair M_1 and M_2 charges the capacitor C_t and reduces the tail current in the amplification phase gradually to almost turn off the tail current source (Fig. 3.4). The drain node OP and ON of input pair M_1 and M_2, therefore, discharge partially and thus save energy. Although the power consumption is low, it suffers a speed decrease due to the small output voltage difference.

The StrongARM latch-type comparator utilizing the dynamic bias technique is

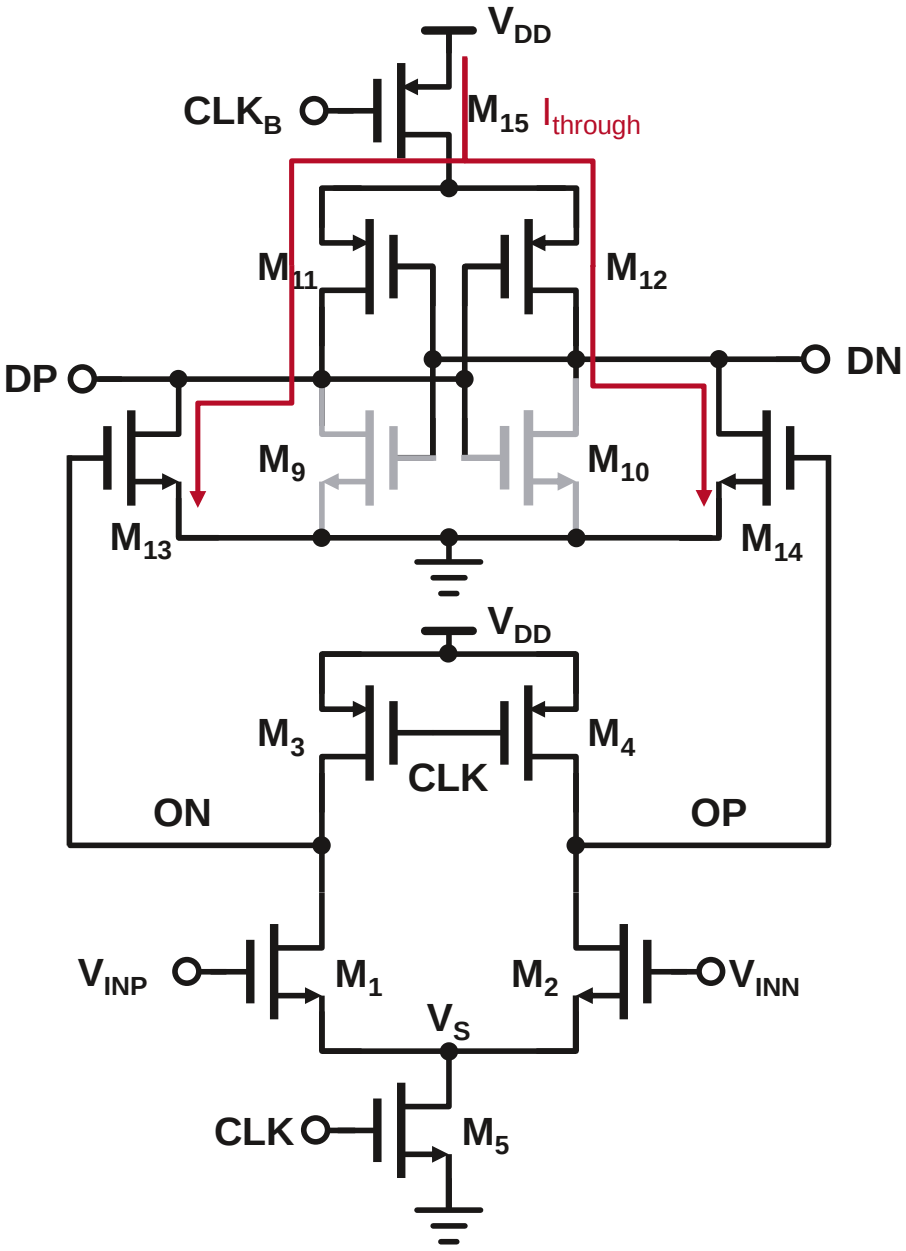


Figure 3.1: Double-tail dynamic comparator [66].

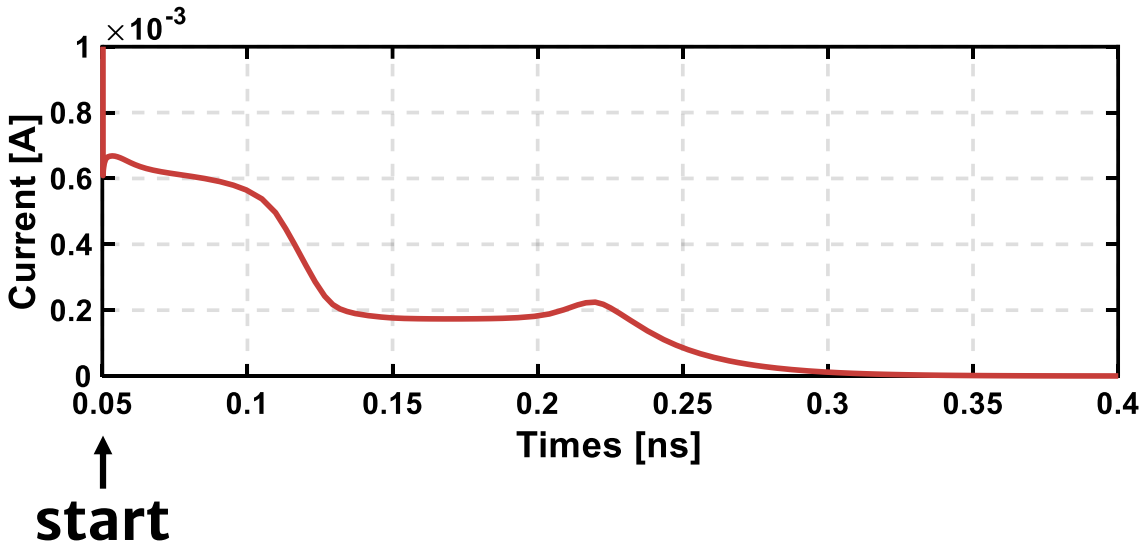


Figure 3.2: Current waveform of the latch of double-tail dynamic comparator.

presented in [89] for low power consumption. The output voltage is not rail-to-rail due to the partial discharging. To guarantee the correct logic level, [89] applies a clock whose duty cycle is more than 50%, which means it needs more time to obtain the correct comparison result. From the perspective of designing the SAR ADC, it takes more time to convert each bit since each conversion of SAR ADC starts when the comparison result is determined. The non-rail-to-rail output voltage also makes the conversion time longer since logic circuits' overdrive voltage is insufficient. Therefore, it is not suitable for high-speed SAR ADC.

Fig. 3.5 presents the proposed high-speed and low-power two-stage dynamic comparator to address the above issues. The speed-enhancement pre-amplifier stage adopted the dynamic bias technique for saving power. The positive feedback of the StrongARM latch speeds up the amplification speed and the regeneration speed of the latch in the 2nd stage. The low-power gain-enhancement latch in the 2nd stage has two input pairs, M_{17}-M_{18} (M_{19}-M_{20}), to sense the output voltage of the pre-amplifier. Instead of the tail current source, the two input pairs enhance input gain and suppress the through current, therefore saving power.

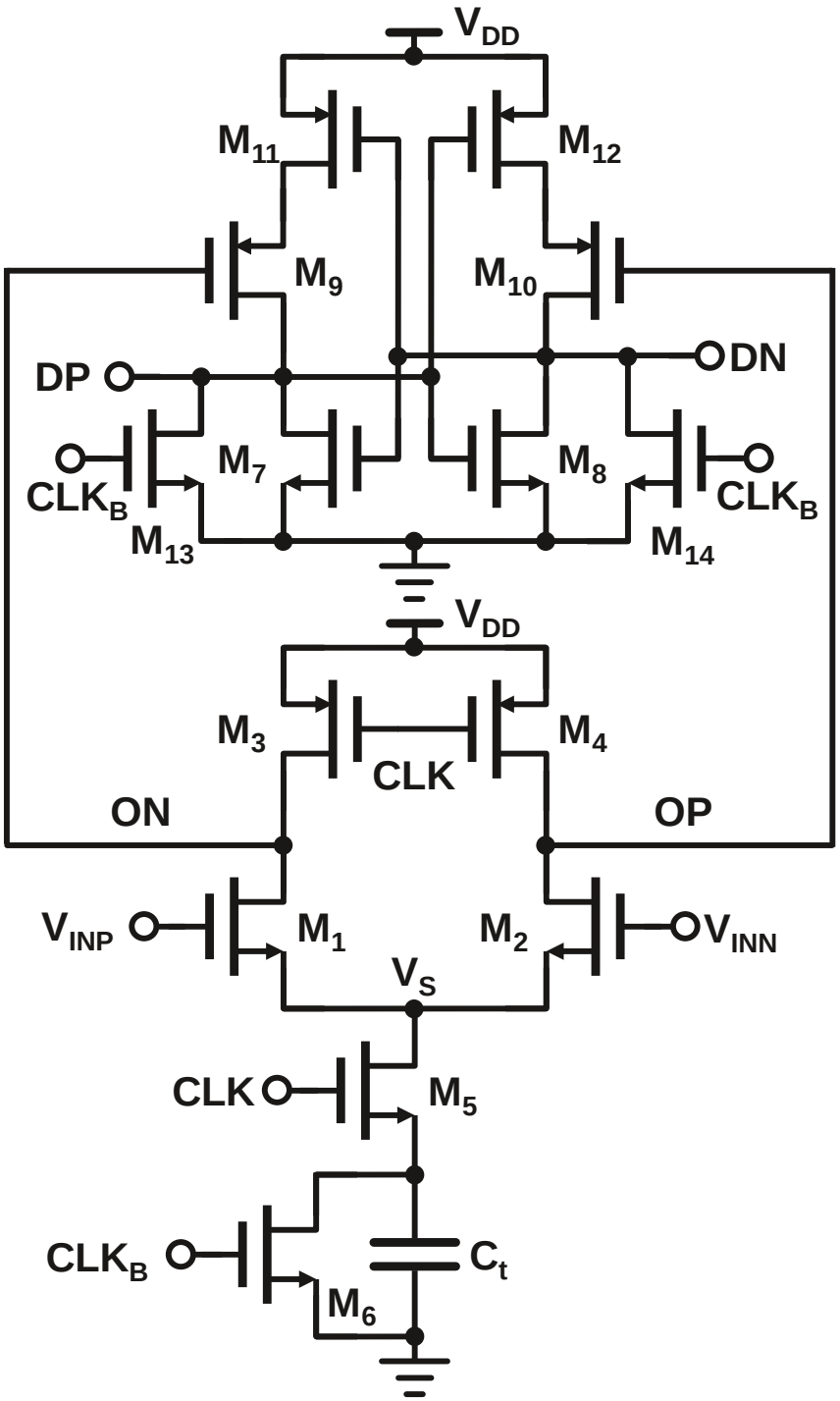


Figure 3.3: Dynamic bias comparator [71].

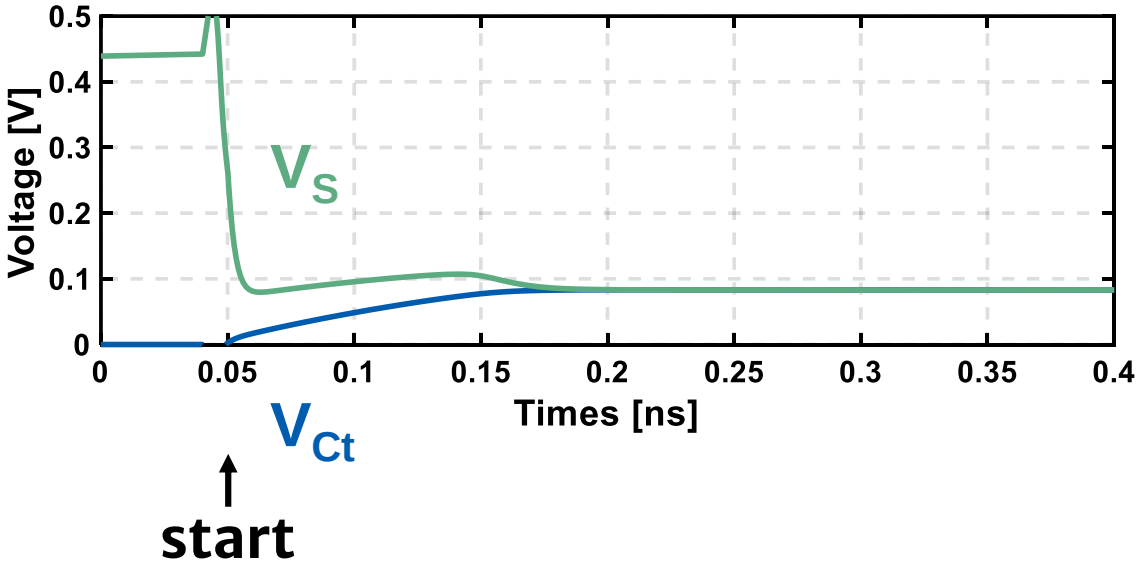


Figure 3.4: Voltage waveform (source voltage of M_5 and top plate voltage of C_t) of the dynamic bias technique.

3.1.1 Operation of the Proposed Comparator

The operation of a dynamic comparator can be divided into two phases: the reset phase and the comparison phase. In the proposed dynamic comparator, during the reset phase ($CLK = GND$, $CLK_B = V_{DD}$), M_8 turns on. The capacitor Ct discharges through M_8. M_9 and M_{10} turns on, and ON and OP is charged to V_{DD}, M_{11} and M_{12} turns on, and the drain node dP and dN of M_1 and M_2 is charged to V_{DD}, ensuring the initial state is determined. M_{21} and M_{22} turn on, and DP and DN discharge to GND. The comparison phase is further divided into two phases: the amplification phase and the regenerative phase. During the amplification phase ($CLK = V_{DD}$, $CLK_B = GND$), M_7 turns on, and M_1 and M_2 start to sense and amplify the input signal. When the voltage of the drain node dP/dN of M_1/M_2 drops greater than a threshold voltage V_{thn} and the voltage of the ON/OP drops a threshold voltage $|V_{thp}|$, the StrongARM latch is active, rapidly amplifying the voltage difference between ON and OP. The input pair M_{17}-M_{18} and M_{19}-M_{20} of the latch in the 2nd stage amplifies the output voltage ON and OP of the pre-amplifier. Then, when DP/DN is greater than V_{thn}, the regeneration starts, and finally, the

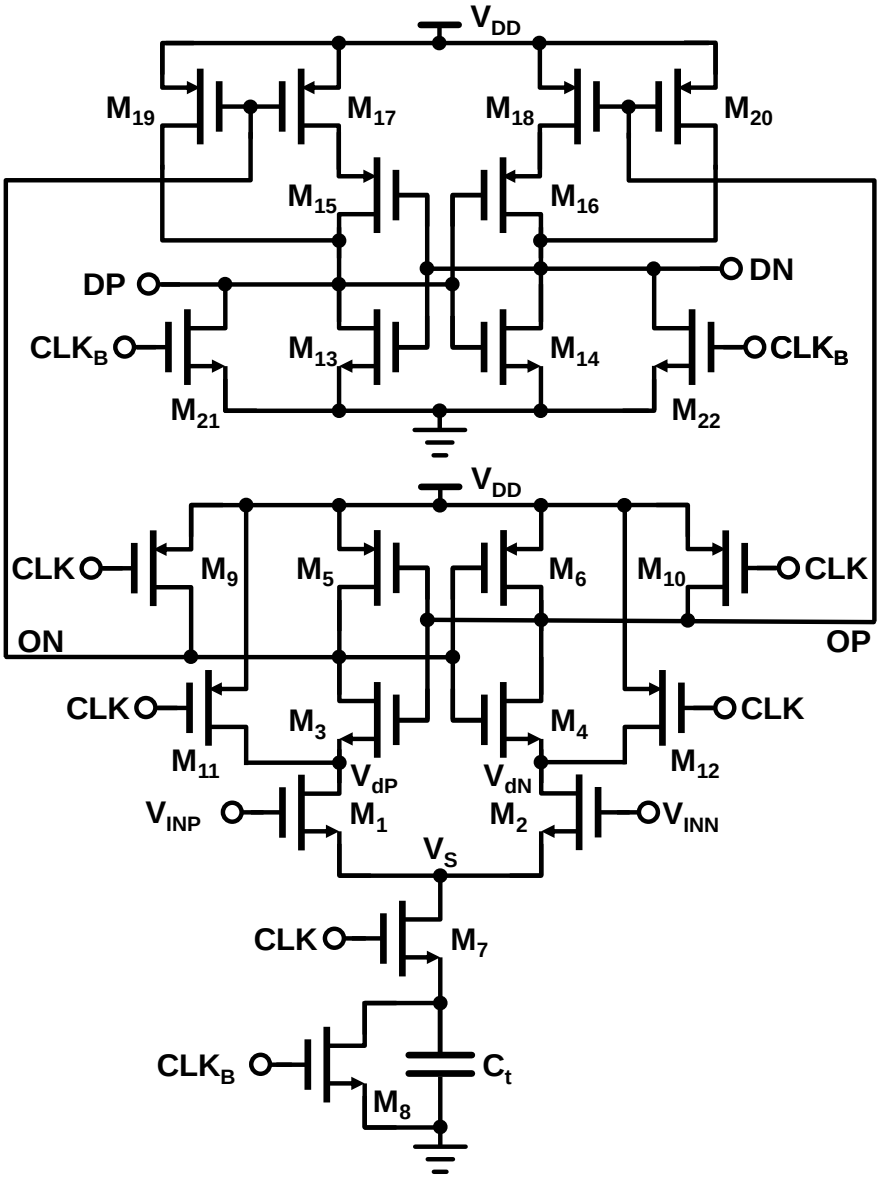


Figure 3.5: Proposed two-stage dynamic comparator.

decision is made on whether V_{INP} is greater than V_{INN}.

3.1.2 Design of the Regeneration Enhancement Pre-Amplifier

The timing waveform of the proposed dynamic comparator is shown in Fig. 3.6. Fig. 3.7 is the timing waveform of the dynamic bias comparator for comparison.

As shown in Fig. 3.7, the voltage difference between ON and OP is very small. The dynamic bias technique saves power consumption by gradually turning off the tail current. Therefore, the ON and OP discharge partially. The gradually decreasing tail current attenuates the voltage difference between ON and OP. In other words, the amplification is also attenuated. This is the reason that the dynamic bias technique slows down the comparison. The regeneration of the latch in the 2nd stage suffers from the small voltage difference between ON and OP.

The proposed pre-amplifier improves the amplification by inserting the StrongARM latch. As shown in Fig. 3.6, This results in a larger voltage difference in the output of the pre-amplifier and the speed enhancement of comparison. The voltage difference becomes larger thanks to the positive feedback of the StrongARM latch. It also accelerates the regeneration of the next stage latch since the more the difference is, the more effective the positive feedback of the latch in the 2^{nd} stage. The detail will be shown in the next section.

3.1.3 Design of the Through Current Suppression Regeneration Latch

As mentioned before, the double-tail comparator (Fig. 3.1) utilizes a high-speed latch, though it has a large through current and thus more power consumption. During the comparison, the through current still flows from V_{DD} to GND until the voltage of ON/OP $V_{ON}/V_{OP} < V_{thn}$. The dynamic bias comparator (Fig. 3.3) utilizes a low-power latch. The through current is suppressed by inserting the PMOS

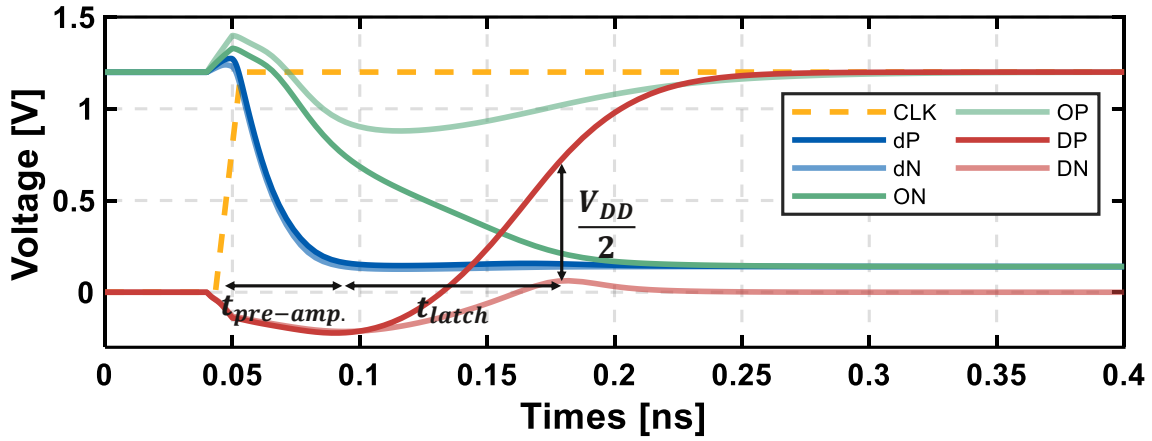


Figure 3.6: Timing waveform of the proposed dynamic comparator ($V_{CM} = 0.8\,V$, $V_{INP} - V_{INN} = 5\,mV$, $f_{CLK} = 1\,GHz$).

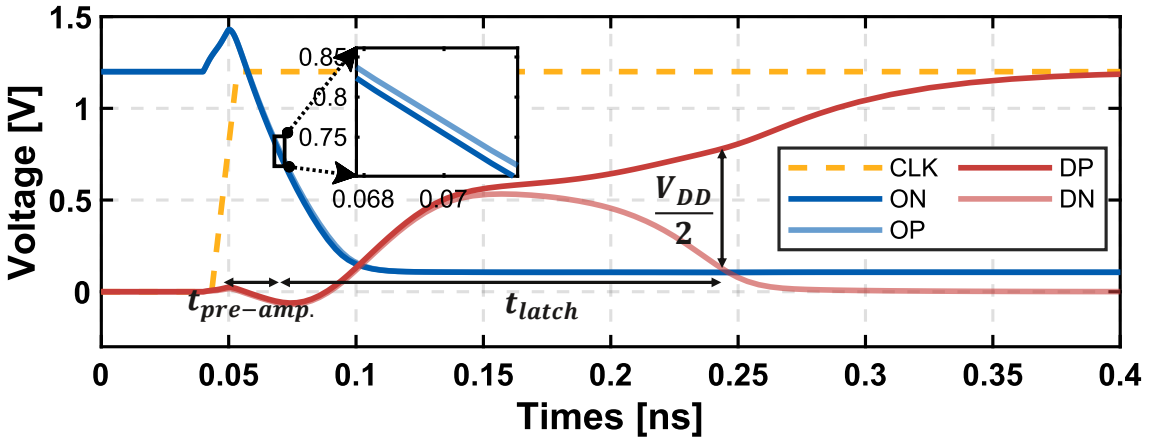


Figure 3.7: Timing waveform of the dynamic bias comparator ($V_{CM} = 0.8\,V$, $V_{INP} - V_{INN} = 5\,mV$, $f_{CLK} = 1\,GHz$).

input pair M_9 and M_{10} into the middle of the path and removing the tail current source. At the beginning of the regeneration phase ($V_{DD} - V_{ON} < |V_{thp}|$ and $V_{DD} - V_{OP} < |V_{thp}|$), the regeneration, which also means the positive feedback, is weakened due to the overdrive voltage V_{ov} of M_9 and M_{10} being very small and the current being very small. The small output voltage difference of the 1st stage further degrades the regeneration. This results in the slow operation of the latch in the 2nd stage. The power consumption is also increased due to the time both NMOS and PMOS turning on becoming longer, and thus, the through current flows more.

The proposed latch remains the cross-coupled inverter. Without any inserting

transistors, this ensures that the positive feedback is not weakened. Therefore, unlike the latch of the dynamic bias comparator (Fig. 3.3) [60], the latch remains in high-speed operation. By replacing the tail current source with an input pair M_{17} and M_{18}, there is no through current path. However, this also damages the speed since, at the beginning, the V_{ov} of the input pair is small, and the current is also small. M_{19} and M_{20} are added as auxiliary input pairs to speed up the regeneration. M_{19} and M_{20} also sense and amplify the voltage of the node ON and OP. Also, connecting the output of M_{19} and M_{20} to DP and DN accelerate the turn-on speed of M_{13}/M_{24}. Although M_{19} and M_{20} make another through current path, the through current flows in a shorter time, and therefore, power consumption does not become a severe problem. Fig. 3.8 shows that the current of the proposed comparator is smaller than the current of the dynamic-bias comparator under a similar bias point (Fig. 3.9). As shown in Fig. 3.6, the difference between ON and OP becomes larger during the regeneration phase. It also speeds up the regeneration. Therefore, the proposed latch achieved high-speed operation and low power consumption.

3.2 Delay Analysis

The analysis of the transconductance and the noise of the dynamic bias pre-amplifier has been analyzed [71]. However, the delay time of the dynamic bias pre-amplifier has not been mentioned. This section discusses the delay of the dynamic bias pre-amplifier and the proposed comparator. It will show the analytical equations that the proposed comparator is faster. Also, the analysis provides the design perspective.

3.2.1 Delay Analysis of the Pre-Amplifier

The clock-to-Q delay (CLK-Q delay) stands for the speed of the comparator and is defined as the time from the rising edge of the clock reaching $V_{DD}/2$ to the output

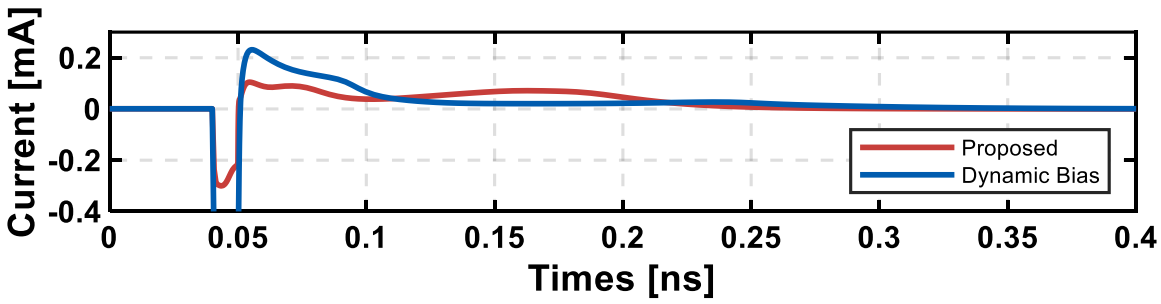


Figure 3.8: Current waveform of the proposed dynamic comparator and the dynamic bias comparator ($V_{CM} = 0.8\,V$, $V_{INP} - V_{INN} = 5\,mV$, $f_{CLK} = 1\,GHz$).

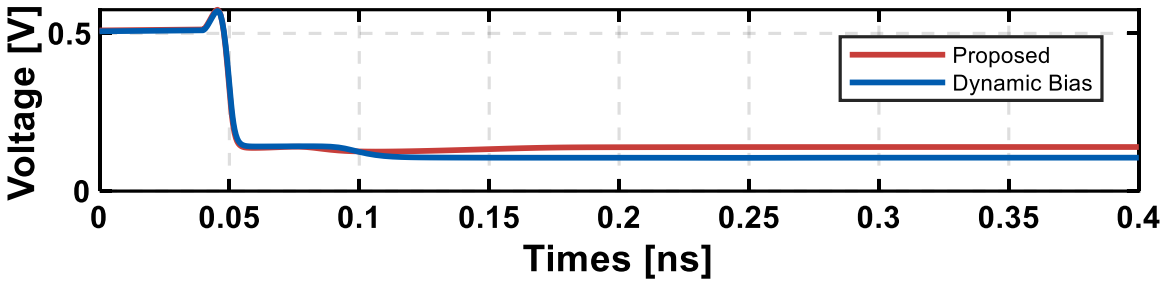


Figure 3.9: Bias voltage waveform of the proposed dynamic comparator and the dynamic bias comparator ($V_{CM} = 0.8\,V$, $V_{INP} - V_{INN} = 5\,mV$, $f_{CLK} = 1\,GHz$).

difference reaching $V_{DD}/2$.

Following the operation of the dynamic comparator, the comparator senses and amplifies the input signal first. The delay of the amplification phase is $t_{pre-amp.}$. The $t_{pre-amp.}$ is defined as the time until the 1st stage latch turns on, which means that at the time the voltage of ON/OP drops to $V_{DD} - |V_{thp}|$, where $|V_{thp}|$ is the threshold voltage of M_5 and M_6. The delay $t_{pre-amp.}$ in the proposed comparator is further divided into two parts: 1) the delay t_1 is defined as the time that M_3/M_4 turns on, and 2) the delay t_2 is defined as the time that the 1st stage latch turns on.

The delay t_1 that M_3/M_4 turns on

The comparison starts at $CLK = V_{DD}$ $(t = 0)$. The charge stored in the parasitic capacitor at the drain nodes dP and dN of the input pair starts to discharge. This results in a current, which is the tail current, also called a common-mode current,

charging the tail capacitor C_t. The charge change of the tail capacitor C_t can be expressed as

$$dq = i_{CM}(t)dt \tag{3.1}$$

Compared to the voltage change of the drain node of the input pair due to the discharging, the voltage change of the source node V_S of the input pair is very small and, therefore, can be seen as a constant voltage. Also, the tail current source M_7 operates at the triode region, and the gate-source voltage V_{GS} change of the M_7 is small. Therefore, it can be modeled as a resistor with constant resistance. Fig. 3.10 shows this first-order approximation RC model.

According to this model, the RC charging equation can be applied to the quantitative analysis of the dynamic bias technique. The charging current $i_{CM}(t)$ can be expressed as

$$i_{CM}(t) = I_{CM}e^{-t/\tau} = i_1 + i_2 \tag{3.2}$$

where I_{CM} is the initial current at $t = 0$, i_1 and i_2 are the current of M_1 and M_2. and the $\tau = r_{ON7}C_t$ is the time constant. The initial current is the sum of the initial current of the input pair expressed as

$$I_{CM} = I_1 + I_2 \tag{3.3}$$

Assuming $V_{INP} > V_{INN}$, the initial current of the input pair can be expressed as

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{CM} + \frac{V_{id}}{2} - V_S - V_{thn})^2 \tag{3.4}$$

$$I_1 = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{CM} - \frac{V_{id}}{2} - V_S - V_{thn})^2 \tag{3.5}$$

where V_{CM} is the bias voltage of the input pair, and V_{id} is the input differential voltage. The current of the input pair flows at a different rate according to the input differential signal, as shown in (3.4) and (3.5). This results in a charge difference

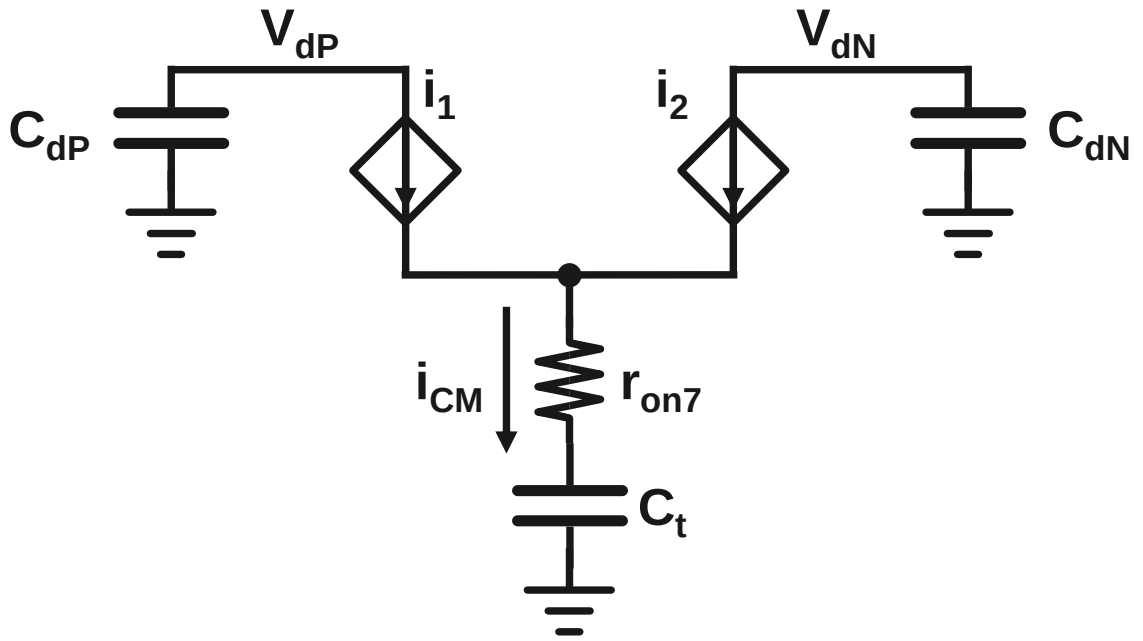


Figure 3.10: The equivalent RC model for the delay t_1.

between the total parasitic capacitor C_d at the drain node of the input pair. The charge difference can be expressed as

$$\Delta Q_1 = C_d \Delta V = C_d(V_{dP} - V_{dN}) = C_d(V_{thn} - \frac{i_2 t_1}{C_d}) \tag{3.6}$$

The delay t_1 can be expressed as

$$t_1 \approx \frac{C_d V_{thn}}{i_i} \tag{3.7}$$

Substituting (3.7) to (3.5), the charge difference can be expressed as

$$\Delta Q_1 = C_d V_{thn}(1 - \frac{i_2}{t_1}) = C_d V_{thn}(1 - \frac{I_2 e^{-t/\tau}}{I_1 e^{-t/\tau}}) = C_d V_{thn}(1 - \frac{I_2}{I_1}) \tag{3.8}$$

At $t = t_1$, according to (1), the total charge of the tail capacitor can be expressed as

$$\int_0^{2C_d V_{thn} - \Delta Q_1} dq = \int_0^{t_1} i_{CM}(t) dt \tag{3.9}$$

Substituting (3.2) and (3.8) to (3.9), the delay t_1 can be calculated and expressed as

$$t_1 = \tau ln[1 - \frac{1}{I_{CM}\tau} C_d V_{thn}(1 + \frac{I_2}{I_1})]^{-1} \tag{3.10}$$

The delay t_2 that the 1st stage latch turns on

After $t = t_1$, the M_3/M_4 turns on, and the model is shown in Fig. 3.11. The charging current of the tail capacitor in this interval can be expressed as

$$i_{CM} = I_{CM,t_1} e^{\frac{-t}{\tau}} \tag{3.11}$$

where $I_{CM,t_1} = i_{CM}(t_1) = i_1(t_1) + i_2(t_1)$ is the initial current that can be seen as the current at $t = t_1$. The initial charge of the tail capacitor in this interval is $2C_d V_{thn} - \Delta Q_1$.

To turn on the 1st stage latch, the total parasitic capacitor of the node ON/OP has to be discharged, and the voltage of the node ON/OP drops a $|V_{thp}|$, the threshold voltage of the PMOS transistor.

Because of the input differential voltage, the charge difference of the node ON and OP can be calculated using the same method as (3.6) to (3.8) and can be expressed as

$$\Delta Q_2 = C_O |V_{thp}|(1 - \frac{I_{2,t_1}}{I_{1,t_1}}) \tag{3.12}$$

where C_O is the total parasitic capacitor of the node ON/OP, $I_{1,t_1} = i_1(t_1)$ is the initial current of the transistor M1 at $t = t_1$, and the same as $I_{2,t1}$.

The total parasitic capacitor C_d at the drain node of the input pair is also continuously discharged. The charge difference of C_d can be expressed as

$$Q_d = C_d \Delta V_d \tag{3.13}$$

where ΔV_d is the voltage difference during this interval.

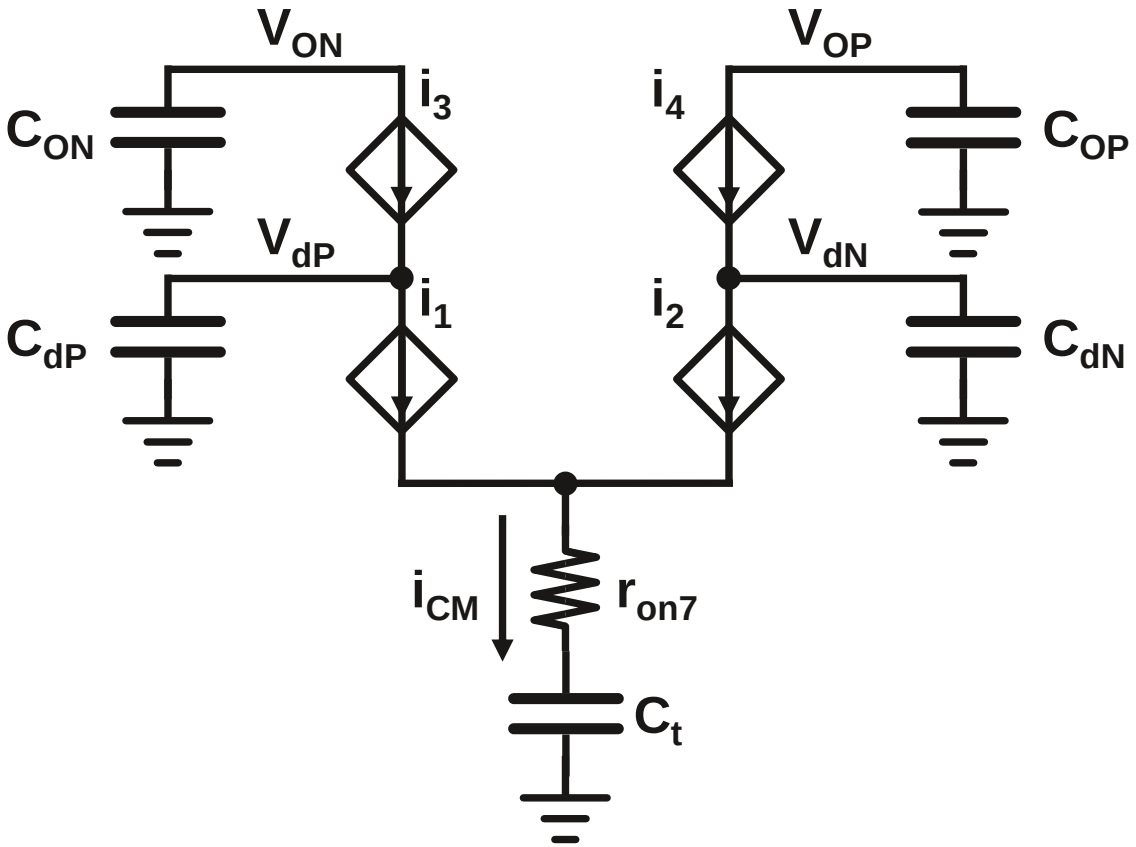


Figure 3.11: The equivalent RC model for the delay t_2.

To obtain the voltage difference ΔV_d, according to the equivalent RC model shown in Fig. 3.11, the current of the parasitic capacitor C_d can be expressed as

$$i_d = i_1 - i_3 \tag{3.14}$$

and can be rewritten as

$$C_{dP} = \int_{V_{DD}-V_{thn}}^{V_{xP}} dV_{ON} = \int_0^{i_2} i_1 dt - C_{ON} \int_0^{|V_{thp}|} dV_{ON} \tag{3.15}$$

where V_{xP} is the final voltage of the node dP at $t = t_2$ and can be calculated as

$$V_{xP} = \frac{-\tau(e^{\frac{-t_2}{\tau}} - 1)}{C_{dP}} - \frac{C_{ON}}{C_{dP}}|V_{thp}| - (V_{DD} - V_{th}) \tag{3.16}$$

The voltage V_{xN} of the node dN can be calculated in the same way as

$$V_{xN} = \frac{-I_{2,t_1}\tau(e^{\frac{-t_2}{\tau}} - 1)}{C_{dN}} - \frac{C_{ON}}{C_{dP}}(|V_{thp}| - \Delta V) - (V_{DD} - V_{th}) \tag{3.17}$$

where ΔV is the small differential voltage between the node ON and OP. From (3.16) and (3.17), the voltage difference delta V_d can be expressed as

$$\Delta V_d = V_{xP} - V_{xN} \approx \frac{(I_{2,t_1} - I_{1,t_1})\tau(e^{\frac{-t_2}{\tau}} - 1)}{C_d} \tag{3.18}$$

Therefore, from (3.13), the charge difference of the capacitor C_d is

$$Q_d = (I_{2,t_1} - I_{1,t_1})\tau(e^{\frac{-t_2}{\tau}} - 1) \tag{3.19}$$

At $t = t_2$, similar to (3.9), the total charge of the tail capacitor can be expressed as

$$\int_0^{2C_O|V_{thp}|-\Delta Q_2+Q_d} dq = \int_0^{t_2} i_{CM}(t)dt \tag{3.20}$$

where $i_{CM}(t) = I_{CM}e^{-(t+t_1)/\tau} = I_{CM,t_1}e^{-t/\tau}$ in this interval. Substituting (3.8), (3.11), (3.12), and (3.19) to (3.20), the delay t_2 can be calculated and expressed as

$$t_2 = \tau ln\{1 - \frac{1}{I_{CM,t_1}\tau}[C_O|V_{thp}|(1 + \frac{I_{2,t_1}}{I_{1,t_2}})]\}^{-1} \tag{3.21}$$

Finally, the delay of the 1st stage pre-amplifier of the proposed comparator is

$$t_{pre-amp.} = t_1 + t_2 \tag{3.22}$$

To reduce the delay of the 1st stage pre-amplifier, (3.22) shows that the straightforward way is increasing the denominator in the natural logarithm function of t_1 and t_2, which are $I_{CM}\tau$ and $I_{CM,t_1}\tau$. The common-mode current (I_{CM} and I_{CM,t_1}) gives an intuition that the larger the current is, the higher the speed becomes. How-

ever, if the common-mode current is too large, as shown later in the delay analysis of the latch, the initial voltage of the latch will be smaller. Thus, the large common-mode current may slow down the latch operation and even the operation of the comparator. The large time constant $\tau = r_{ON7}C_t$ can reduce the delay. The design perspective of the on-resistance r_{ON7} is the same as the common-mode current since the small on-resistance makes the large common-mode current. In the wide temperature range, the on-resistance will vary significantly due to the significant change in the threshold voltage. On the other hand, the capacitance changes slightly in the wide temperature range. Therefore, it is better to design the time constant using the capacitor. There is a trade-off between speed and power consumption. A large tail capacitor C_t can make the delay $t_{pre-amp.}$ become small. However, it means that it will take more time to make the voltage of the tail capacitor reach the drain voltage of tail current M_7, thus weakening the effect of the dynamic bias and consuming more power. The size of the input pair and the latch in the 1st stage are also important for speed. The large size of those transistors makes the parasitic capacitor C_d, and C_O becomes large and thus increases the delay. For the design of capacitor C_d, there is a trade-off between speed and mismatch since the large input pair has good matching; however, this damages the speed.

3.2.2 Delay Analysis of the Regeneration Latch

The delay analysis of the pre-amplifier adopting the dynamic bias technique is mentioned above. [90] gives the delay equation of the cross-coupled inverter. The delay of the 1st stage latch, therefore, can be expressed as

$$t_{1stlatch} = \frac{C_O}{g_{m,inv,1}} ln(\frac{V_{fnl}}{V_{init}}) \tag{3.23}$$

where the $g_{m,inv,1}$ is the transconductance of the inverter in the 1st stage latch.

The V_{fnl} is the final voltage of the latch operation. Here, it is defined as the

voltage that the 2nd stage latch turns on, which is the time t_0 that the node DP/DN is charged to the voltage larger than the threshold voltage

$$V_{fnl} = \frac{t_0 \Delta I}{C_O} = \frac{t_0 g_{m,inv,1} V_{Odiff.}}{C_O} \tag{3.24}$$

where $V_{Odiff.}$ is the differential voltage of the node ON and OP, and the time t_0 can be expressed as

$$t_0 = \frac{V_{thn} C_D}{I_{15/16}} \tag{3.25}$$

The V_{init} is the initial voltage of the latch operation. It is the time that the M_5/M_6 turns on. It can be expressed as

$$\begin{aligned} V_{init} &= |V_{ON} - V_{OP}| = |V_{thP}| - \frac{i_2 t_{pre-amp.}}{C_O} \approx |V_{thP}| - \frac{I_2 |V_{thP}|}{I_1} \\ &= |V_{thP}|(1 - \frac{I_2}{I_1}) = |V_{thP}| \frac{\Delta I_{in}}{I_1} \approx \frac{2|V_{thp}| g_m V_{id}}{I_{CM}} \\ &= 2|V_{thp}| \frac{\sqrt{\mu_n C_{ox} \frac{W}{L} I_{CM}}}{I_{CM}} V_{id} \end{aligned} \tag{3.26}$$

Where $\Delta I_{in} = g_m V_{id} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{CM}} V_{id}$delta Iin=gm Vid=(mu n Cox w/L ICM) Vid. Substituting (3.24) and (3.24) into (3.23), the delay of the 1st stage latch $t_{1^{st}latch}$ can be expressed as

$$t_{1^{st}latch} = \frac{C_O}{g_{m,inv,1}} ln(\frac{V_{thn} C_D g_{m,inv,1} V_{Odiff.} I_{CM}}{2|V_{thp}| \sqrt{\mu_n C_{ox} \frac{W}{L} I_{CM}} V_{id} I_{15/16} C_O}) \tag{3.27}$$

(3.27) shows that to reduce the delay, the aspect ratio of the input pair M_1 and M_2 must be designed large, suppressing the mismatch and thus the input-referred offset voltage. Note that if the aspect ratio is designed too large, as mentioned before, there is a trade-off between the speed and mismatch. The large capacitance C_O also increases the delay $t_{1^{st}latch}$. Also, the common-mode current I_{CM} will increase and turn off the tail current source M_7 quickly. Thus, it takes longer to complete the

operation of the 1st stage latch. The capacitance C_D of the 2nd stage latch should be designed small to reduce the delay. However, as described later, it will slow down the 2nd stage latch.

The delay of the 2nd stage latch is the same as (3.23) and can be rewritten as

$$t_{2\text{nd}_{latch}} = \frac{C_O}{g_{m,inv,2}} ln(\frac{V_{fnl,2}}{V_{init,2}}) \tag{3.28}$$

Where the $g_{m,inv,2}$ is now the transconductance of the inverter in the 2nd stage latch, and the C_D is the total capacitance of the node DP/DN.

The $V_{fnl,2}$ here is the final result of the comparison, which is defined as

$$V_{fnl,2} = \frac{V_{DD}}{2} \tag{3.29}$$

The $V_{fnl,2}$ is the initial voltage of the 2nd stage latch operation. It is the time that the M_{13}/M_{14} turns on. It is similar to (3.26) and can be expressed as

$$\begin{aligned} V_{init,2} &\approx V_{thn}(1 - \frac{I_{14}}{I_{13}}) \\ &= V_{thn}\frac{\Delta I_{2\text{nd}_{latch}}}{I_{13}} \\ &= \frac{V_{thn}(g_{m,17/18} + g_{m,19/20})V_{fnl}}{I_{13}} \\ &= \frac{V_{thn}(g_{m,17/18} + g_{m,19/20})}{I_{13}} \frac{t_0 g_{m,inv,1} V_{Odiff.}}{C_O} \\ &= \frac{V_{thn}(g_{m,17/18} + g_{m,19/20})}{I_{13}} \frac{V_{thn} C_D}{I_{13(15/16)}} \frac{g_{m,inv,1} V_{Odiff.}}{C_O} \\ &= (\frac{V_{thn}}{I_{13}})^2 \frac{(g_{m,17/18} + g_{m,19/20}) C_D g_{m,inv,1} V_{Odiff.}}{C_O} \end{aligned} \tag{3.30}$$

where the V_{thn} here is the threshold voltage of the M_{13} and $_{14}$, and the $\Delta I_{2\text{nd}_{latch}}$ is the differential current of M_{17} and M_{18}. Substituting (3.29) and (3.30) into (3.28), the

delay of the 2nd stage latch $t_{2\text{nd}_{latch}}$t(2nd latch) can be expressed as

$$t_{2\text{nd}_{latch}} = \frac{C_D}{g_{m,inv,2}} ln(\frac{V_{DD}C_O I_{13}^2}{2V_{thn}^2(g_{m,17/18} + g_{m,19/20})C_D g_{m,inv,1} V_{Od}}) \tag{3.31}$$

(3.31) shows that the auxiliary input pair M_{19} and M_{20} reduces the delay with certainty. The previous section described that the 2nd stage latch has two input pairs, the M_{19}-M_{20} and the M_{17}-M_{18}. The M_{17}-M_{18} is not only the input pair but also the current source of the 2nd stage latch. However, due to the partial discharging of the node ON/OP, the sensed voltage difference V_{Od} is small. Thus, the speed of the latch becomes slow, although this saves power consumption. This becomes more severe if the input signal is smaller. To solve this problem, the auxiliary input pairs M_{19}-M_{20} provide another transconductance to further reduce the delay and provide another current path for quickly turning on M_{13}/M_{14}. There is the through current flow from M_{19}/M_{20} to M_{13}/M_{14}. The through current flows very short time thanks to the high-speed operation of the 2nd stage latch. Also, thanks to the partial discharging of the node ON/OP, the M_{19}-M_{20}, like the M_{17}-M_{18}, also operates in the weak or moderate inversion region in which the current is smaller. Therefore, the through current is not a severe problem. As shown in (3.31), the dual latch structure speeds up the regeneration phase. The transconductance of the 1st stage latch times the transconductance of the input pairs of the 2nd stage latch $(g_{m,17/18} + g_{m,19/20})g_{m,inv,1}$ further reduces the delay. The parasitic capacitance C_O/C_D ratio should be designed to be small. However, as mentioned previously, a small C_D reduces the delay of the 1st stage latch while increasing the delay of the 2nd stage latch. It is a trade-off when designing the two latches. For the above reasons, the proposed 2nd stage latch achieved low power and high-speed operation.

Finally, the delay of the proposed comparator is

$$t_{delay} = t_{pre-amp.} + t_{1\text{st}_{latch}} + t_{2\text{nd}_{latch}} = t_{pre-amp.} + t_{latch} \tag{3.32}$$

from (3.27) and (3.31), if the two latches are designed the same, which means that $g_{m,inv,1} = g_{m,inv,2}$, $C_O = C_D$, the delay of two latches can be expressed as

$$\begin{aligned} t_{latch} &= t_{1^{st}latch} + t_{2^{nd}latch} \\ &= \frac{C_O}{g_{m,inv,1}} ln[\frac{V_{DD} I_{CM} I_{13}}{4|V_{thp}|V_{thn} g_m Vid(g_{m,17/18} + g_{m,19/20})}] \end{aligned} \tag{3.33}$$

For comparison, [87] gives the delay of the double-tail dynamic comparator:

$$t_{latch} = 2\frac{V_{thn} C_D}{I_{tail,2}} + \frac{C_D}{g_{m,inv}} ln(\frac{V_{DD} I_{tail,2}^2 C_O}{8V_{thn}^2 C_D g_{m,13/14} g_m V_{id}}) \tag{3.34}$$

(3.33) gives some design intuition. A large common-mode current I_{CM} will slow down the operation speed of the latch. On the other hand, a small current of the 2nd stage latch can reduce the delay. In other words, the delay can be reduced by designing M_{17}-M_{18}, the current source of the 2nd stage latch. Compared to (3.34), it is not easy to adopt the same design strategy since if the tail current of the 2nd stage is reduced, the delay of the amplification phase will increase. Therefore, the proposed comparator has greater design freedom than the double-tail comparator. Again, the auxiliary input pairs M_{19}-M_{20} provide another gain and, therefore, speed up the operation of the latch.

3.3 Results

3.3.1 Measurement Results in 180-nm CMOS Technology

The proposed comparator was taped out in a 180-nm technology. Fig. 3.12 shows the circuits, and the die photo is shown in Fig. 3.13. Note that the M_{17}-M_{18} are not in this version (version 1). Thus, there is a memory effect due to the node dP and dN not being reset.

Fig. 3.14 shows the measurement results of the relation between the probability

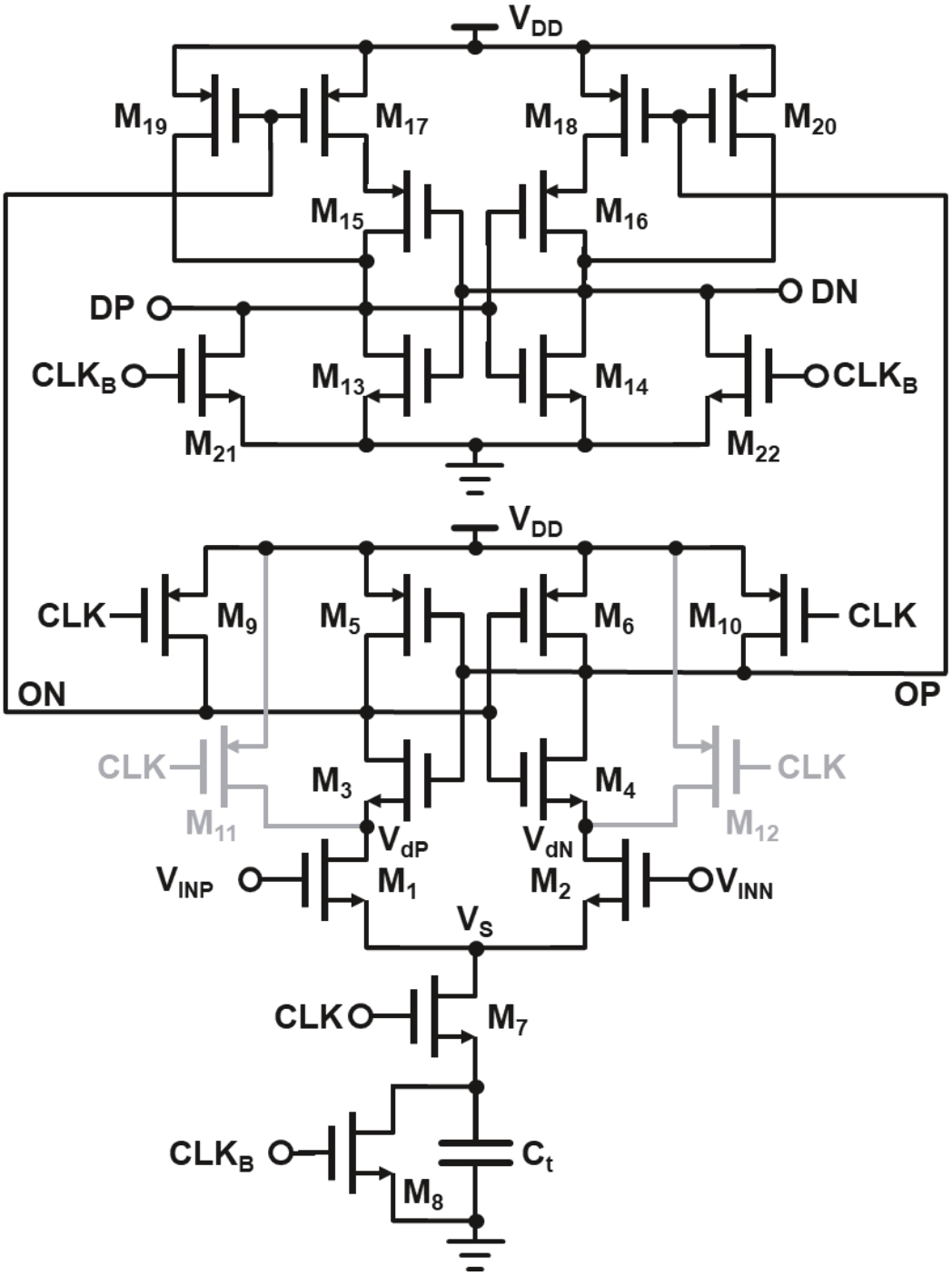


Figure 3.12: Proposed comparator (version 1).

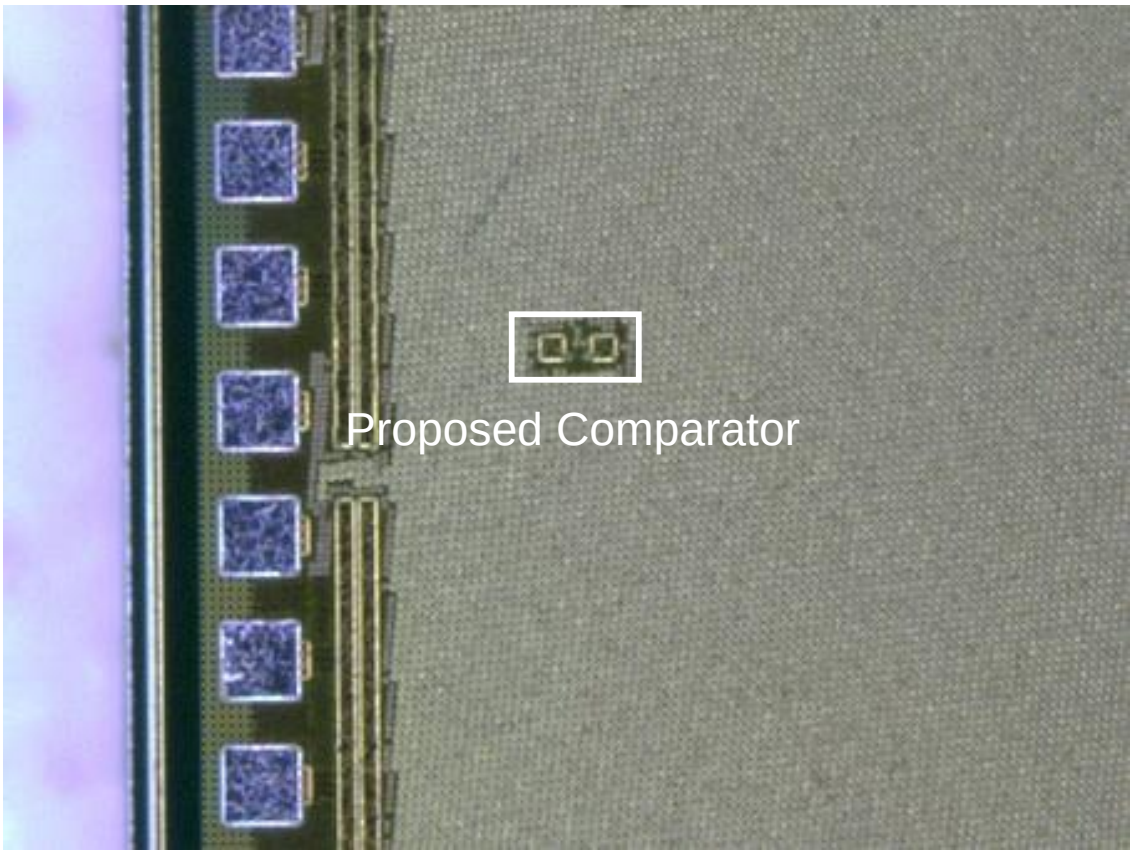


Figure 3.13: Chip photo of the proposed comparator.

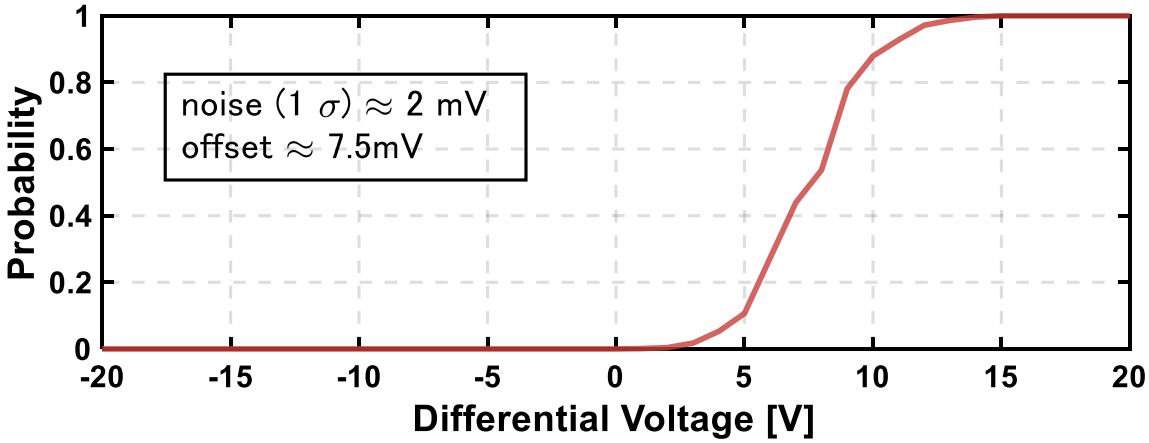


Figure 3.14: Measurement noise and offset of the proposed comparator.

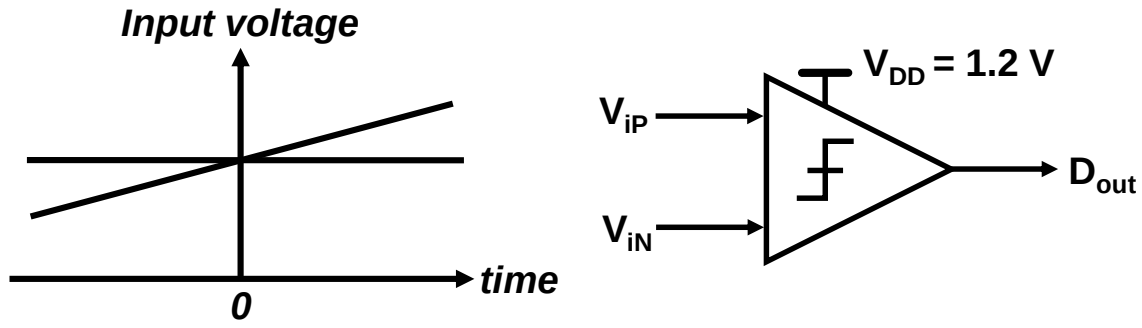


Figure 3.15: Noise simulation method.

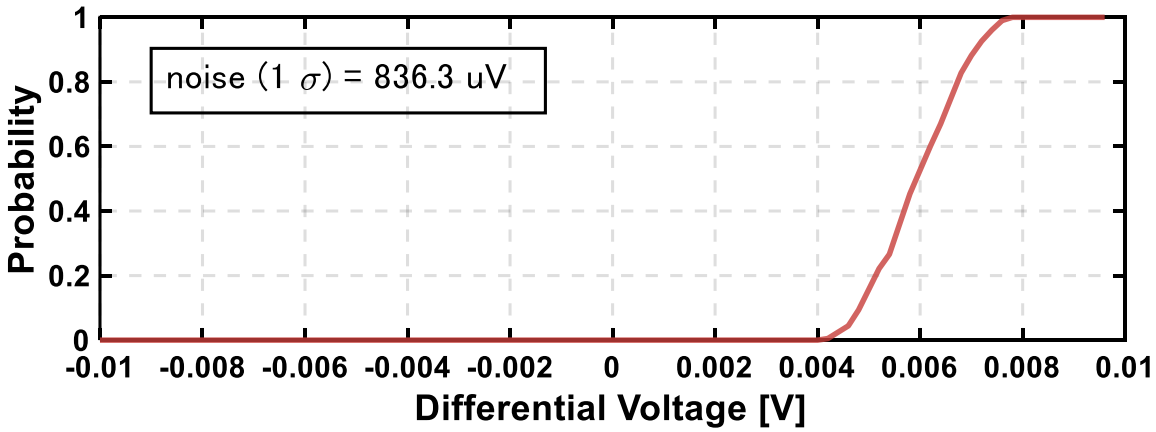


Figure 3.16: Probability of output when $V_{iP} > V_{iN}$.

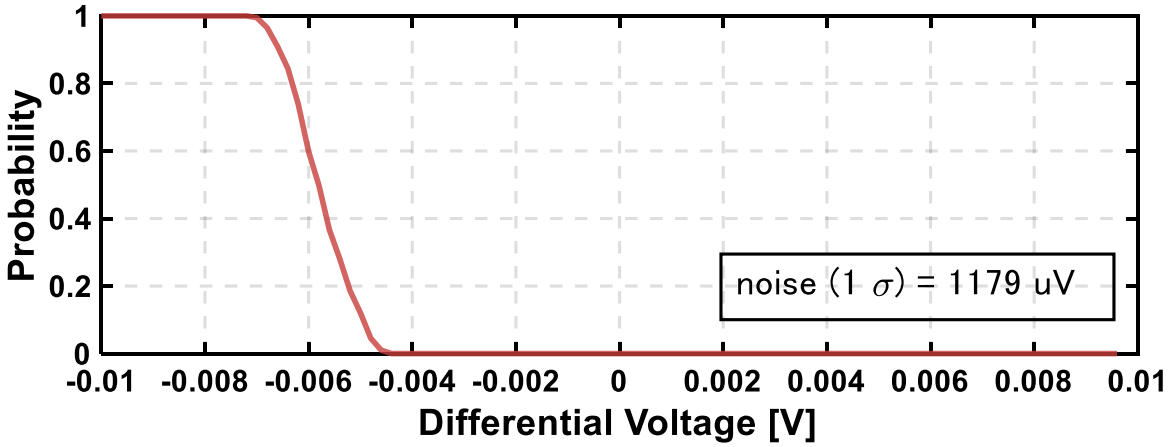


Figure 3.17: Probability of output when $V_{iP} < V_{iN}$.

and the input differential voltage. It shows that the offset is about 7.5 mV, and the noise (1σ) is about 2 mV. Fig. 3.15 shows the method of noise simulation. The simulation results are shown in Fig. 3.16 and 3.17. The offset has a good consistency, while the noise has an unignorable difference. It is considered that the noise from the PCB board causes the difference due to the lack of filters in the design.

3.3.2 Simulation Results in 65-nm Cryo-CMOS Technology

All three comparators have been designed and simulated utilizing 65-nm cryo-CMOS technology with $V_{DD} = 1.2V$ at $T = 300\,K$ and $4\,K$. For a fair comparison, the size of all comparators' input pairs is the same to have similar characteristics. The bias point of the proposed comparator and the dynamic bias comparator are also designed at a similar point. Fig. 3.9 shows the voltage V_S of the proposed comparator and the dynamic bias comparator. They are almost the same value at the amplification phase, so both the transconductance (g_m) of the input pair are almost the same value and thus have similar performances. The 2^{nd} stage latch of all comparators is designed at the same aspect ratio, although the latch architecture is different. The 1st stage latch of the proposed comparator is also designed at the same aspect ratio. Both circuit simulation results and post-layout simulation results are presented. Fig. 3.18, Fig. 3.19, and Fig. 3.20 shows the layout of all comparators. The area of the proposed comparator is 233 μm^2, greater than the double-tail comparator, whose area is 103 μm^2, and smaller than the dynamic bias comparator, whose area is 269 μm^2. The layouts of all comparators are as similar as possible to ensure a fair comparison.

From the perspective of designing SAR ADC, the common-mode voltage variation of comparators affects the performance of SAR ADC, for example, large variation results in large SNDR variation [80]. Another conclusion from [80] is that the best FoM of the comparator is obtained near $V_{DD}/2$ ($= V_{CM}$). Therefore, it is important to design a switching scheme with less V_{CM} variation or no V_{CM} variation

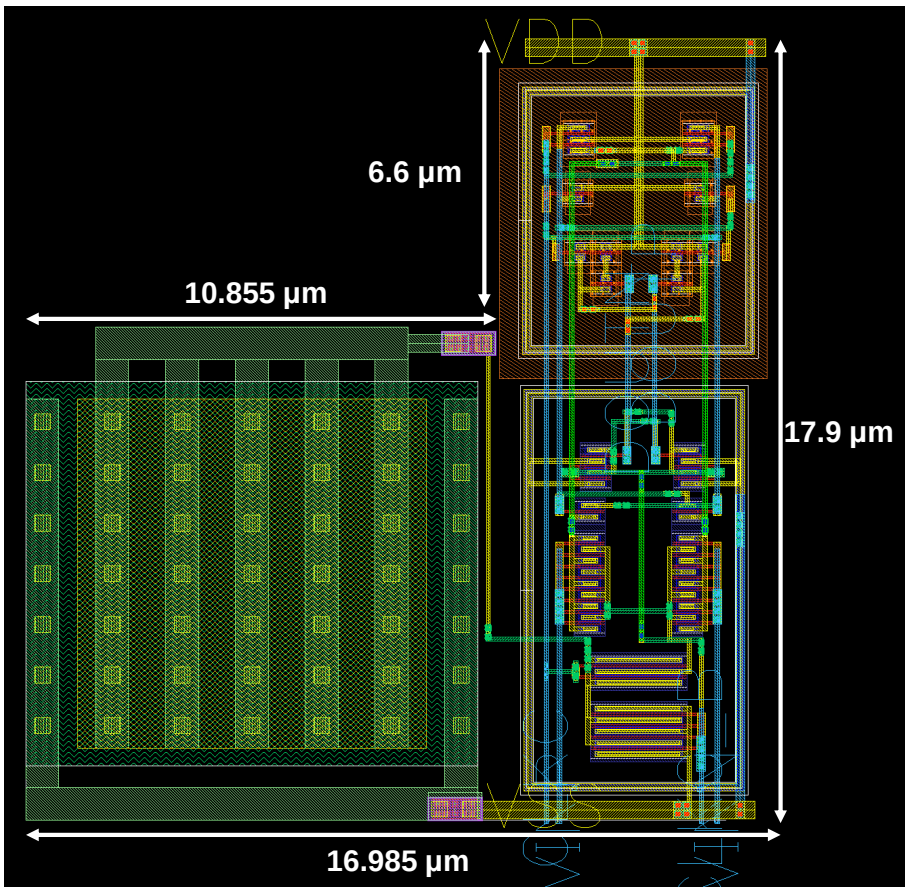


Figure 3.18: The layout of the proposed comparator.

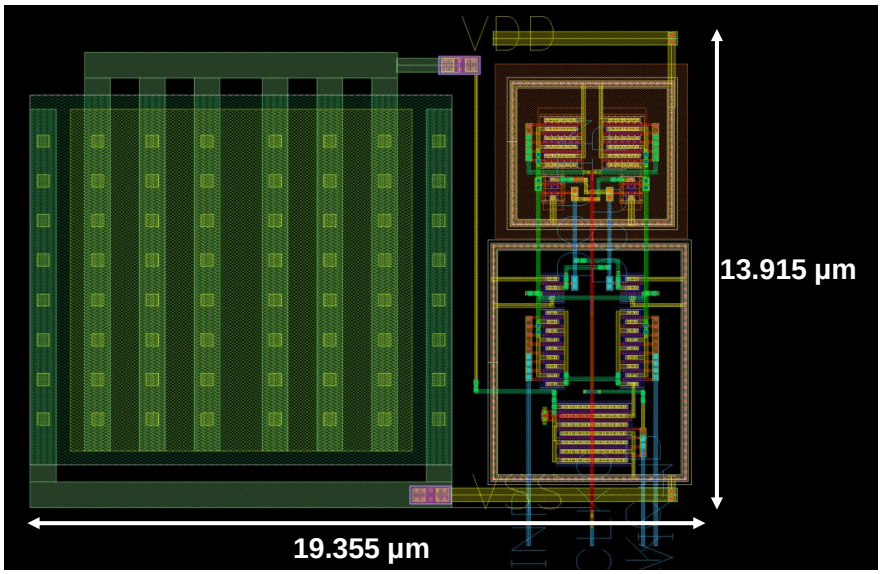


Figure 3.19: The layout of the dynamic bias comparator.

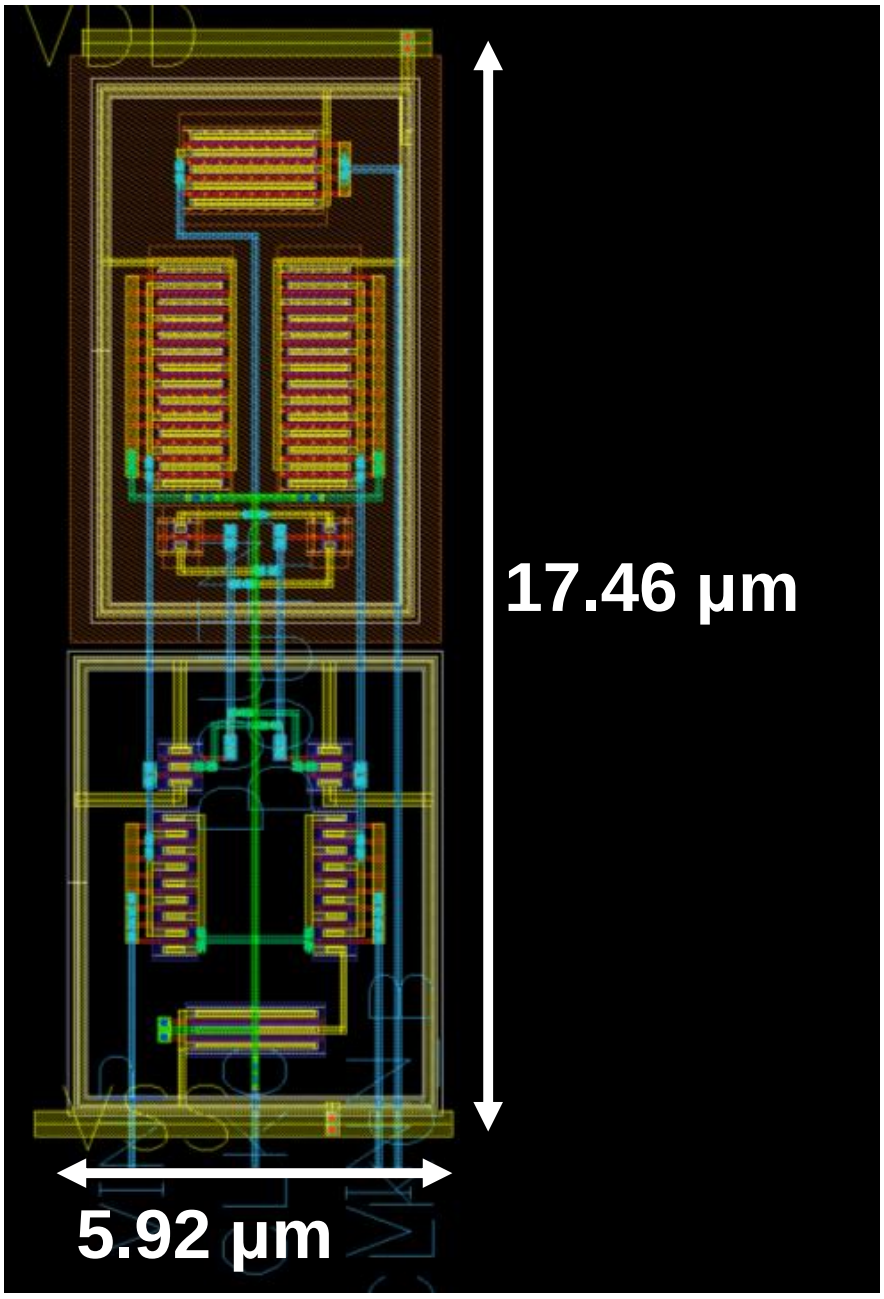


Figure 3.20: The layout of the double-tail comparator.

and operate near V_{CM}. Considering the design of a comparator for a specific SAR ADC, it must match the structure of the SAR ADC in order to achieve the best performance.

Assuming a 10-bit 100 MHz SAR ADC, the LSB is about 1.17 mV with $V_{DD} = 1.2V$. The input differential voltage of the comparator, therefore, is set at 1 mV, which is smaller than 1 LSB. The clock frequency is 1 GHz.

Fig. 3.21 and Fig. 3.22 shows the Energy/comparison as a function of V_{CM}. The proposed comparator has the smallest energy from $V_{CM} = 0.5V$ to V_{DD} at $T = 300\,K$, and from $V_{CM} = 0.6V$ to V_{DD} at $T = 4\,K$. At $T = 4\,K$, due to the increased threshold voltage, all comparators are unable to complete the comparison at $V_{CM} = 0.5V$. Therefore, the figure does not show the data at$V_{CM} = 0.5V$. On the other hand, energy consumption decreases at $T = 4\,K$ because of the improved current performance. The post-layout simulation results show consistency with the circuit simulation results. Note that the double-tail comparator has worsened the most. This is because it charges/discharges fully to V_{DD}/GND and thus consumes more energy when considering the resistance of wires.

Fig.3.23 and Fig.3.24 shows the CLK-Q delay as a function of V_{CM}. At $T = 300\,K$, Although the circuit simulation results show that the proposed comparator is slower than the double tail comparator, it is faster than the dynamic bias comparator except for V_{CM} near V_{DD} and below $V_{DD}/2$ thanks to the proposed technique. At $V_{CM} = 0.5V$, Neither the proposed comparator nor the dynamic comparator can have a rail-to-rail output. Therefore, there is no post-layout simulation data. The circuit simulation results show that the delay becomes slower when the V_{CM} increases for the proposed comparator and the dynamic bias comparator. This is due to the dynamic bias technique of quickly turning off the tail current source, which we call the quick turn-off effect. In more detail, (3.33) shows that increasing I_{CM} reduces the delay of the latch. When the quick turn-off effect governs more than the effect the gain provides, the delay may become slow. Otherwise, the delay may become fast.

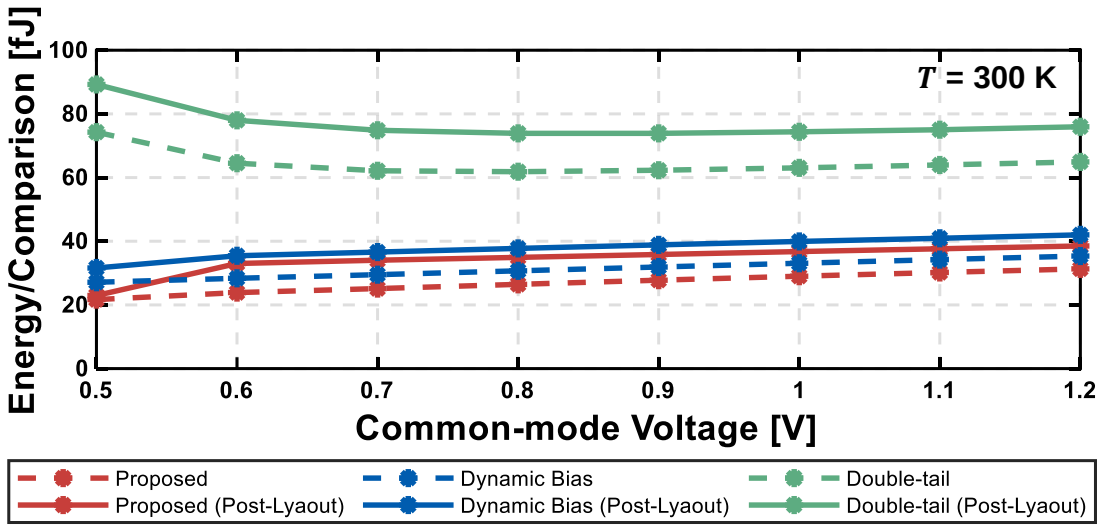


Figure 3.21: Energy per comparison versus common-mode voltage at $T = 300\,K$.

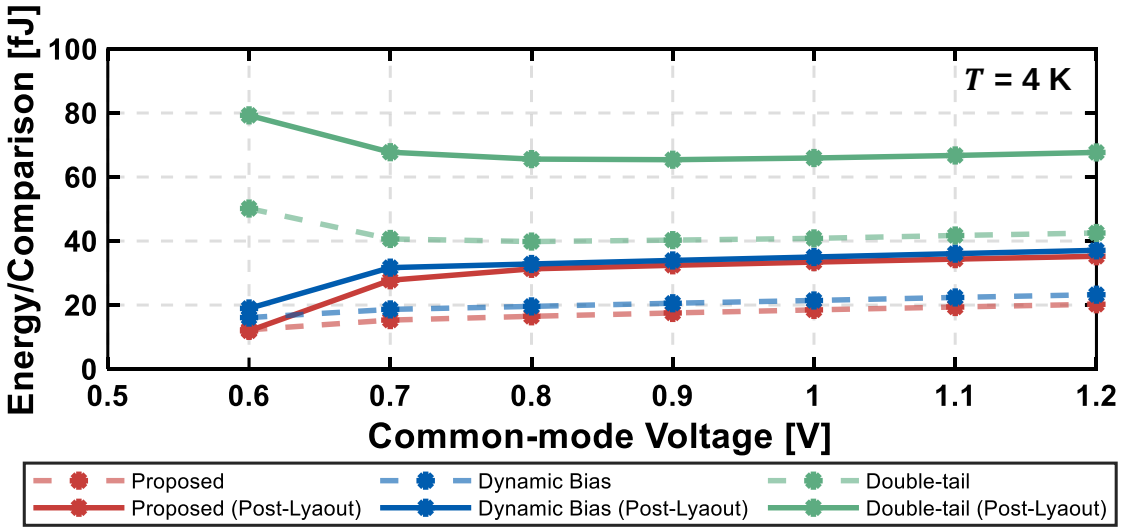


Figure 3.22: Energy per comparison versus common-mode voltage at $T = 4\,K$.

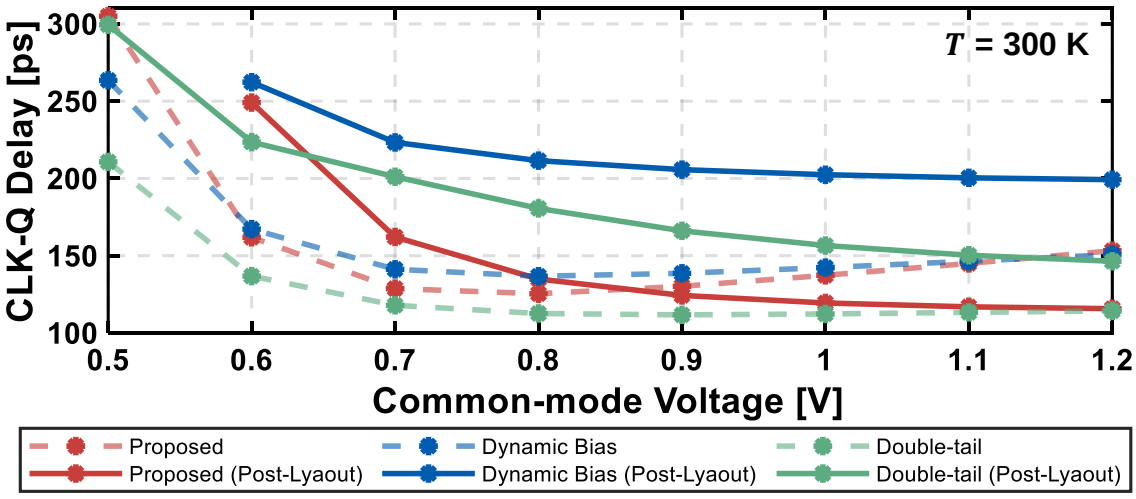


Figure 3.23: Clock-to-Q delay versus common-mode voltage at $T = 300\,K$.

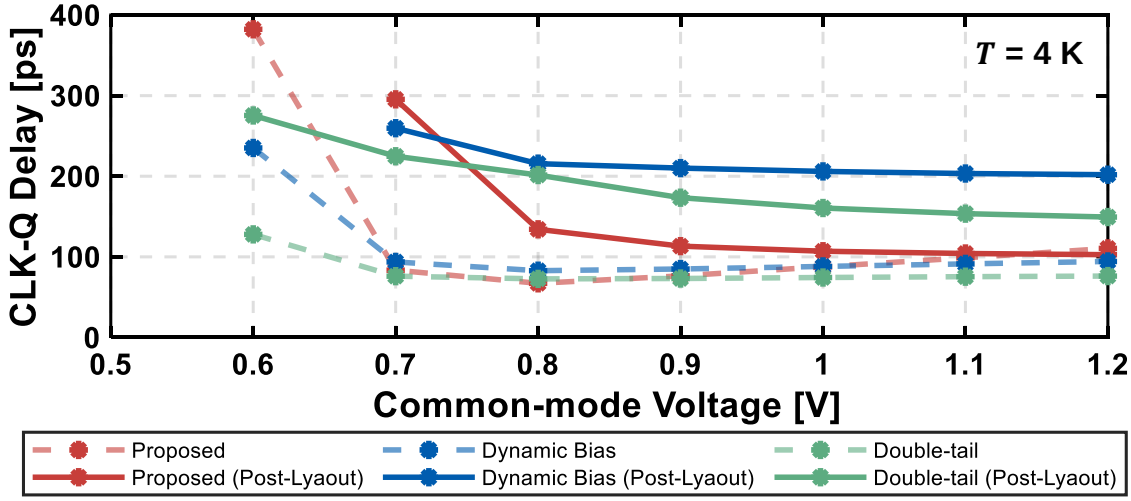


Figure 3.24: Clock-to-Q delay versus common-mode voltage at $T = 4\,K$.

The post-layout simulation results show that the proposed comparator is even faster than the double-tail comparator. Thanks to the greater gain provided by the dual latch structure, this is further enhanced because of the resistance of the wires. This is also the reason that the post-layout simulation shows that all comparators operate faster when V_{CM} increases. As mentioned previously, all the comparators cannot operate correctly at $V_{CM} = 0.5V$ at $T = 4\,K$. Both the proposed comparator and the dynamic comparator cannot have a rail-to-rail output at $0.6V$. Therefore, there is no post-layout simulation data to be shown. At $T = 4\,K$, the overdrive voltage will decrease due to the increased threshold hold voltage and thus degrade the delay of the comparator. The proposed comparator has the least degradation thanks to the stronger positive feedback and gain enhancement. Thanks to the proposed technique, the proposed comparator is the fastest, both at $T = 300\,K$ and $4\,K$.

Fig. 3.25 and Fig. 3.26 shows the post-layout simulation results of the CLK-Q delay as a function of $\log(V_{id})$ at different V_{CM} for all comparators at $T = 300\,K$ and $4\,K$. The proposed comparator shows a higher common-mode voltage sensitivity. The discharging of the input pair M_1 and M_2 is slow at near $V_{CM} = V_{DD}/2$. It causes the transconductance g_m of the 1^{st} stage latch to stay low and thus take a longer time to operate, as (3.33) shows. In other words, low V_{CM} attenuates the positive feedback of the 1^{st} stage latch. For higher V_{CM}, due to the quick turn-off effect, the slope of the proposed comparator is flatter than the other two comparators. Also, (3.21) shows that increasing input difference reduces the delay of the pre-amplifier even though the proposed comparator is the fastest for small V_{id} and is competitive with the double-tail comparator for large V_{id}.

Fig. 3.27 shows the circuit simulation results of input-referred noise as a function of V_{CM}. There is no noise model with good reliability for $T = 4\,K$. Although the thermal noise is easy to model, the shot noise has not been studied well. Therefore, only the results at $T = 300\,K$ are shown. All comparators have been designed to have similar noise at $V_{DD}/2 = V_{CM} = 0.6V$, which satisfies the required SNDR of

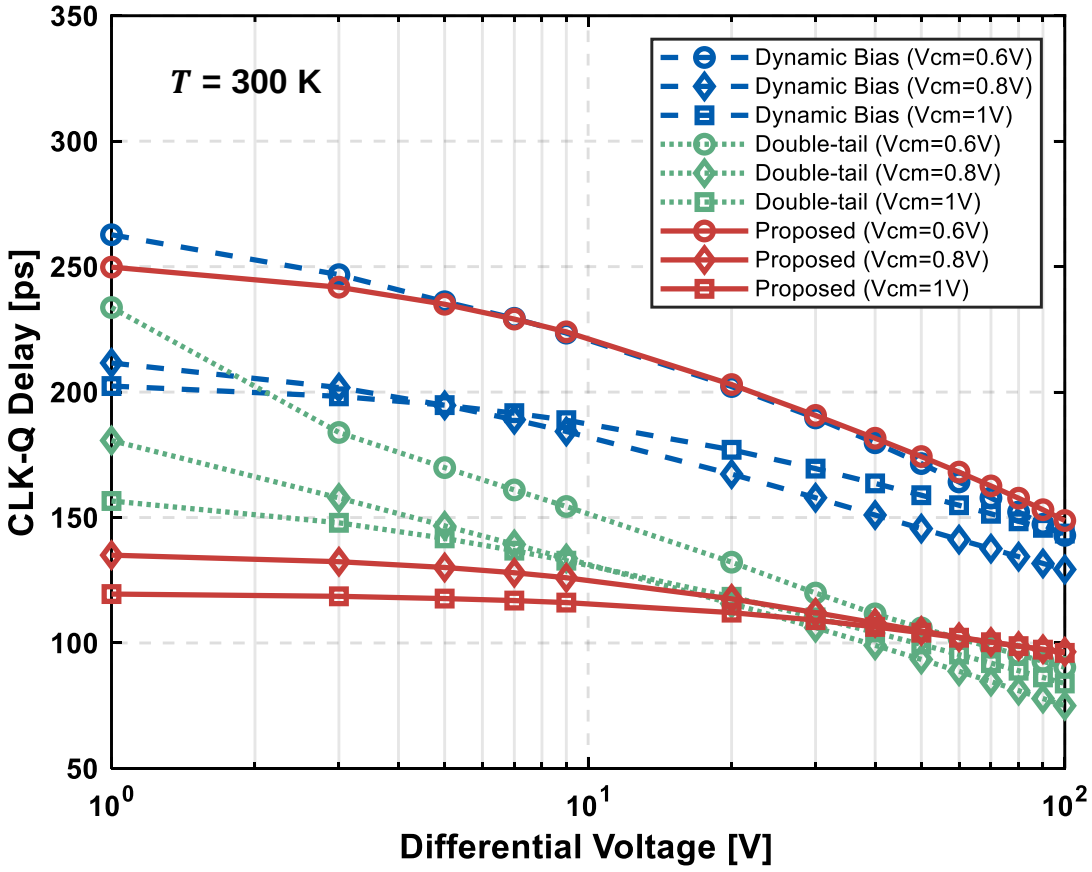


Figure 3.25: The CLK-Q delay as a function of $\log(V_{id})$ at different V_{CM} for all comparators at $T = 300\,K$.

the assuming SAR ADC. The proposed comparator has the lowest input-referred noise except for V_{CM} near V_{DD}.

For comparison, [80] defined an FoM expressed as

$$FoM = \frac{1}{Power \cdot Delay \cdot Noise} \tag{3.35}$$

Fig. 3.28 shows the circuit simulation results of FoM as a function of V_{CM} at $T = 300\,K$. The proposed comparator has the best FoM. From the perspective of designing SAR ADC, for example, a bidirectional switching scheme [76] results in the input common-mode voltage of the comparator going to near $V_{DD}/2$ during the conversion cycle. The voltage difference at the LSB side is smaller than the MSB side,

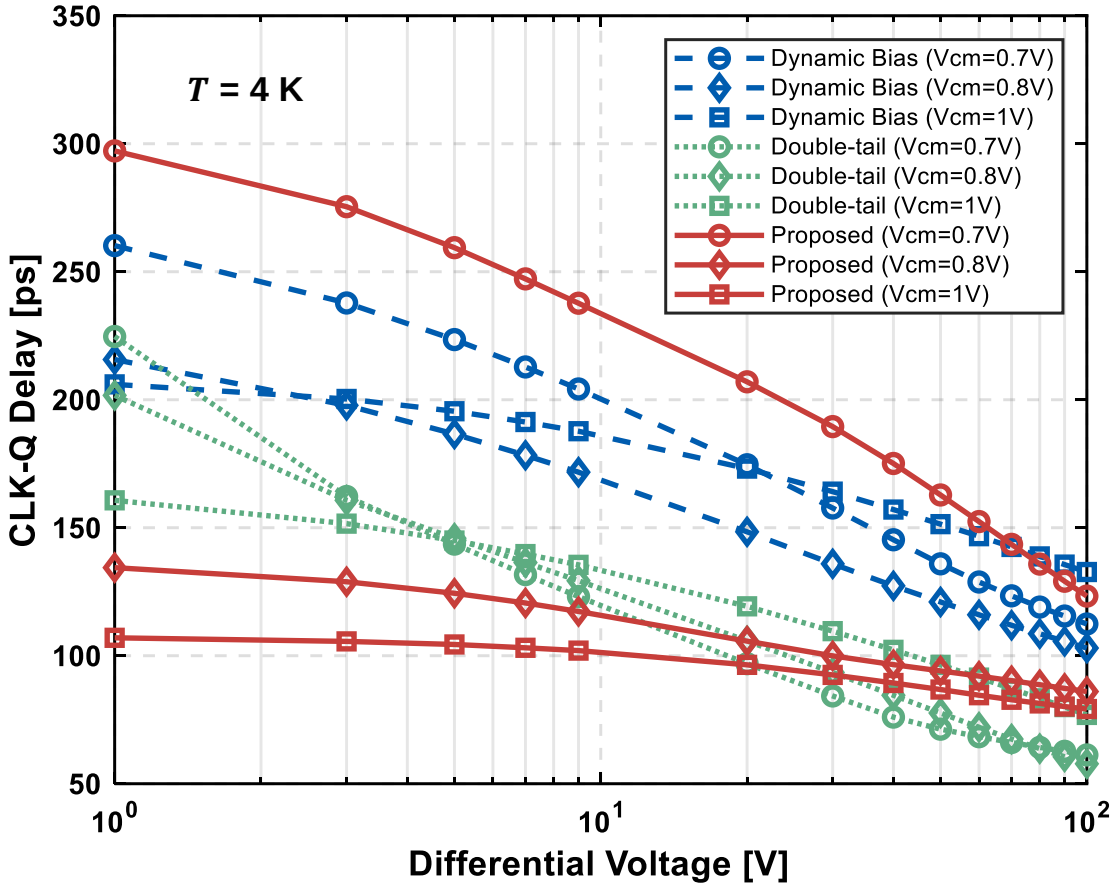


Figure 3.26: The CLK-Q delay as a function of $\log(V_{id})$ at different V_{CM} for all comparators at $T = 4\,K$.

spending more time to complete the conversion. It is more desirable to make the comparator operate at a high FoM region, that is, the input common-mode voltage V_{CM} near $V_{DD}/2$. Therefore, the proposed comparator can improve the performance of the bidirectional switching scheme SAR ADC since, on the LSB side, the proposed comparator can operate at the highest FoM region.

This research defines another FoM for speed orientation. Just remove the input-referred noise from (3.35). Fig. 3.29 shows the speed-orientated FoM at $T = 300\,K$, and the results at $T = 4\,K$ are shown in Fig. 3.30. The proposed comparator achieved the best speed-power performance. It is very suitable for low-power, medium-resolution, high-speed SAR ADC.

Table 3.1 compared the proposed comparator and the other comparator. The

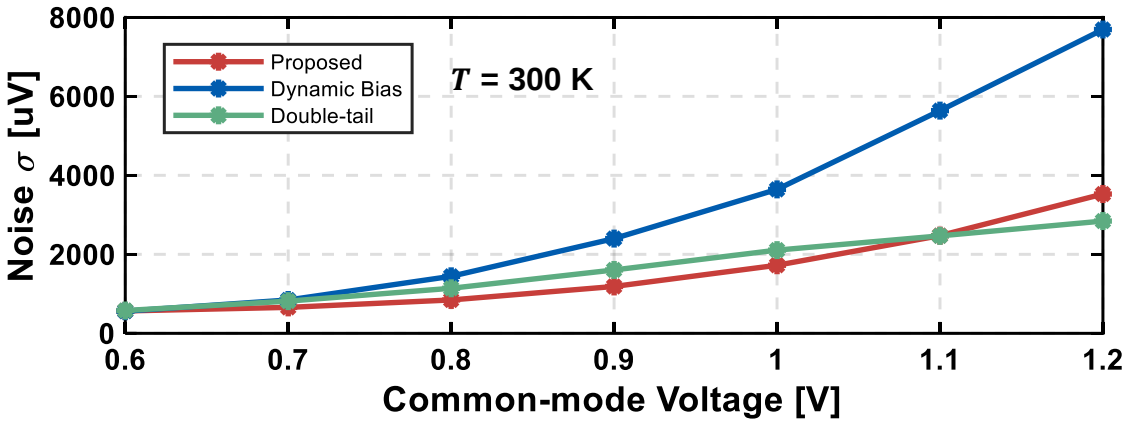


Figure 3.27: Input-referred noise versus common-mode voltage.

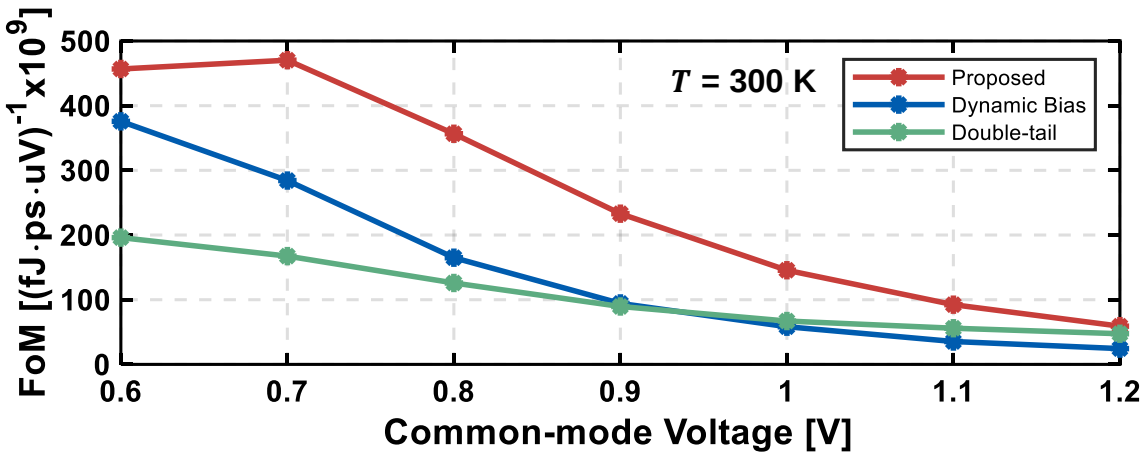


Figure 3.28: FoM versus common-mode voltage.

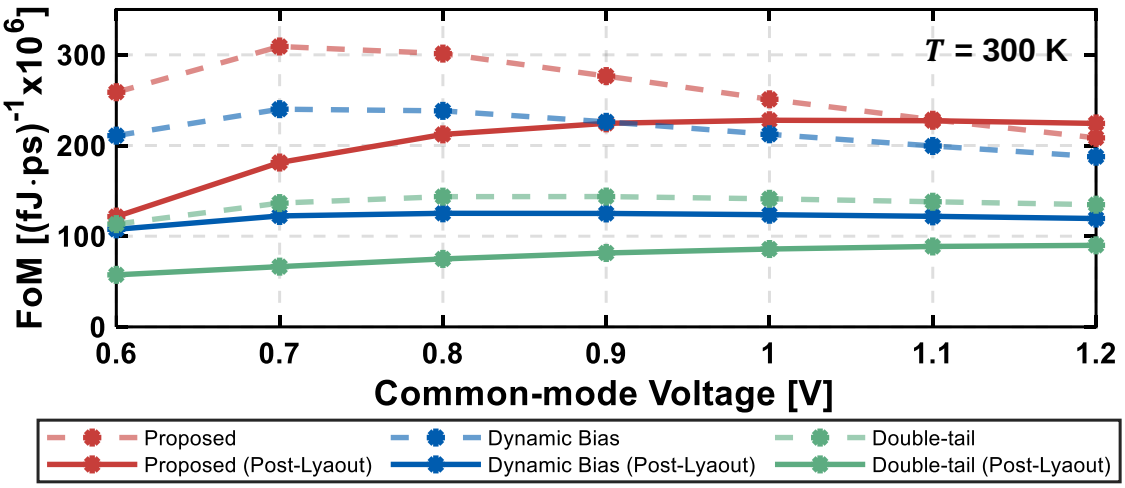


Figure 3.29: Speed-orientated FoM versus common-mode voltage at $T = 300\,K$.

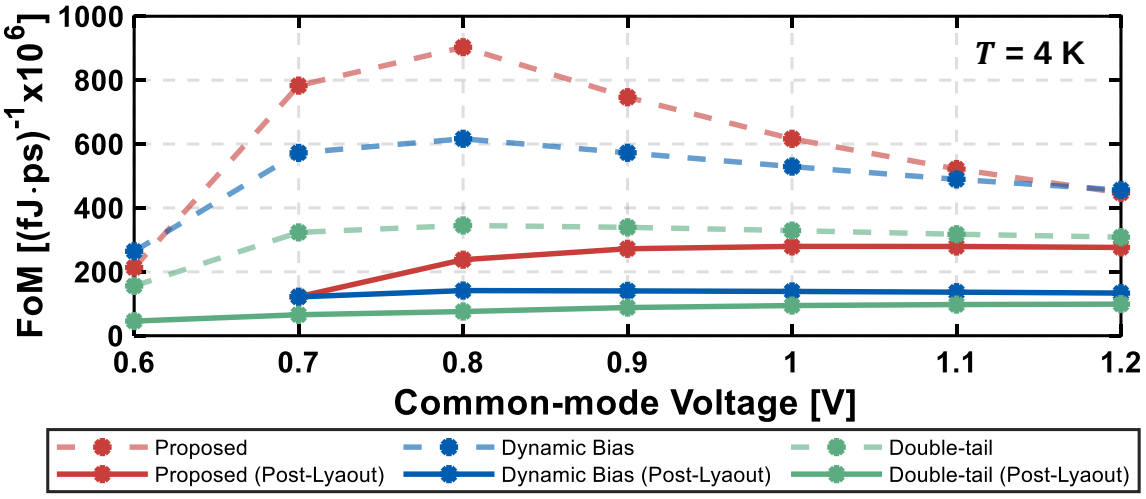


Figure 3.30: Speed-orientated FoM versus common-mode voltage at $T = 4\,K$.

Table 3.1: Performance comparison of dynamic comparator.

	This Work (Circuit & post-layout simulation results @$V_{CM} = 0.7\,V$, 300 K / 4 K)			Simulation results	Measurement results		
	Proposed	Dynamic Bias	Double-tail	TVLSI'23 [93]	JSSC'18 [72]	TVLSI'14 [88]	Access'19 [92]
Technology [nm]	**65**			28	65	180	180
Supply Voltage [V]	**1.2**			1	1.2	1.2	1.2
Frequency [GHz]	**1**			8	0.05	0.5	2
Energy/Comparison [fJ]*	**25.13 / 15.3**	29.5 / 18.64	62.13 / 40.65	1232.5	34	660	112.5
	34.04 / 27.75	36.6 / 31.69	74.85 / 67.75				
Clock-to-Q Delay [ps]*	**128.7 / 83.49**	141.2 / 93.71	117.9 / 76.06	68	1200	550	>800
	162.1 / 295.4	223.3 / 259.6	201.1 / 224.8				
Noise 1σ [uV]*	**657.4** / –	844.6 / –	815.4 / –	45.6	400	7800	–
	– / –	– / –	– / –				
FoM $[(fJ{\cdot}ps{\cdot}uV)^{-1}{\cdot}10^9]$*	**470.33** / –	284.25 / –	167.42 / –	261.66	61	0.35	–
	– / –	– / –	– / –				
FoM w/o Noise $[(fJ{\cdot}ps)^{-1}{\cdot}10^6]$*	**310 / 213**	240 / 264	140 / 156	11.93	24.5	2.8	<11.1
	181.23 / 121.99	122.36 / 121.56	66.43 / 65.66				

*Under this situation: $V_{CM} = V_{DD}/2$, $V_{id} = 1\,mV$. Except for this work and [93]. The V_{id} of [93] is $0.05\,mV$ for delay and the results are at T = 323 K.

proposed comparator has the best FoM and FoM w/o noise at both $T = 300\,K$ and $4\,K$. Therefore, the proposed comparator has the best balance between power consumption and speed. It is more suitable for high-speed, high-performance ADC.

3.4 Conclusion

In this chapter, a high-speed and low-power two-stage dynamic comparator with regeneration enhancement and through current suppression techniques is presented. A delay analysis of the dynamic bias technique is presented. The delay analysis not only gives a deep understanding of the dynamic bias technique but also gives a good intuition for designing the proposed comparator and the dynamic bias comparator. The simulation result shows that the proposed comparator achieved the

best FoM thanks to the proposed positive-feedback-enhancement pre-amplifier and the low-power high regeneration ability latch. The proposed comparator is suitable for realizing low-power and high-speed SAR ADC from $T = 300\,K$ and $4\,K$, making wide temperature operation possible. It will achieve the best performance, especially if the common-mode voltage of the comparator is near $V_{DD}/2$.

Chapter 4

Gain Boosting Dynamic Capacitive Pre-Amplifier Based Comparator

The proposed two-stage dynamic comparator in Chapter 3 has achieved a high-speed and low-power operation. The simulation results show that it is sensitive to the V_{CM} variation due to the NMOS input pair of the pre-amplifier. For instance, the performance changes significantly as the common-mode voltage changes. The increased V_{th} at $4\,K$ causes the NMOS input pair to operate close to the weak inversion region. In other words, the equivalent gate-source voltage shrinks at the same gate voltage V_G. Therefore, it further degrades the performance. Recently, the FIA is another popular pre-amplifier architecture [72]. It has low power consumption and is not so sensitive to the V_{CM} variation, while it is not suitable for high-speed operation due to its initial state being reset to V_{CM}, not V_{DD}/GND. CSPC has addressed the issues [73]. The CSPC has achieved a full-scale input voltage range and is more insensitive to the V_{CM} variation. It also maintains low power consumption. However, the speed of CSPC is still slow, and the speed-power efficiency is low.

In this chapter, the proposed gain boosting dynamic capacitive pre-amplifier (DCA) comparator is present. The proposed gain boosting DCA comparator adopts the cross-coupled pair to enhance the amplification. It increases the output volt-

age difference of the DCA and speeds up the latch operation in the 2nd stage. We call it gain boosting. The proposed gain boosting DCA comparator is insensitive to common-mode variation thanks to the reservoir capacitor. The larger drain-source voltage V_{DS} realizes the wide input range operation. Therefore, the increased threshold voltage V_{th} at $T = 4\,K$ has less effect on the performance of the proposed comparator. The regeneration latch remains the cross-coupled inverter structure to ensure high-speed regeneration. Also, utilizing the input pair as the current source reduces the through current and saves power. With the proposed common-mode variation suppression switching scheme as described in the Chapter 5, the comparator and the SAR ADC can operate at the best performance.

4.1 Operation of Gain Boosting DCA Based Comparator

Fig. 4.1 shows the proposed gain boosting DCA based comparator. Table 4.1 lists the size of the transistors. The 1st stage utilizes the proposed gain boosting DCA as the pre-amplifier, and the 2nd stage is the regeneration latch stage. The pre-amplifier includes a CMOS input pair (M_1, M_2, M_7, M_8), a reservoir capacitor ($C_{res} = 200\,fF$), and a CMOS cross-coupled pair (M_3 M_6) connected by the integration capacitor ($C_{intP} = 12.5\,fF, C_{intN} = 12.5\,fF$). The regeneration latch, a modification from [67, 68], incorporates a CMOS input pair ($M_{13}, M_{14}, M_{22}, M_{23}$) that also serves as the current source and a CMOS auxiliary input pair ($M_{12}, M_{15}, M_{21}, M_{24}$).

During the reset phase ($CLK = 0$), the top plate of the reservoir capacitor, the drain node of the NMOS cross-coupled latch, the drain node of the NMOS input pair, and the digital output (DP and DN) of the regeneration latch are set to V_{DD}. Similarly, the bottom plate of the reservoir capacitor, the drain node of the PMOS cross-coupled latch, and the drain node of the PMOS input pair are set to GND.

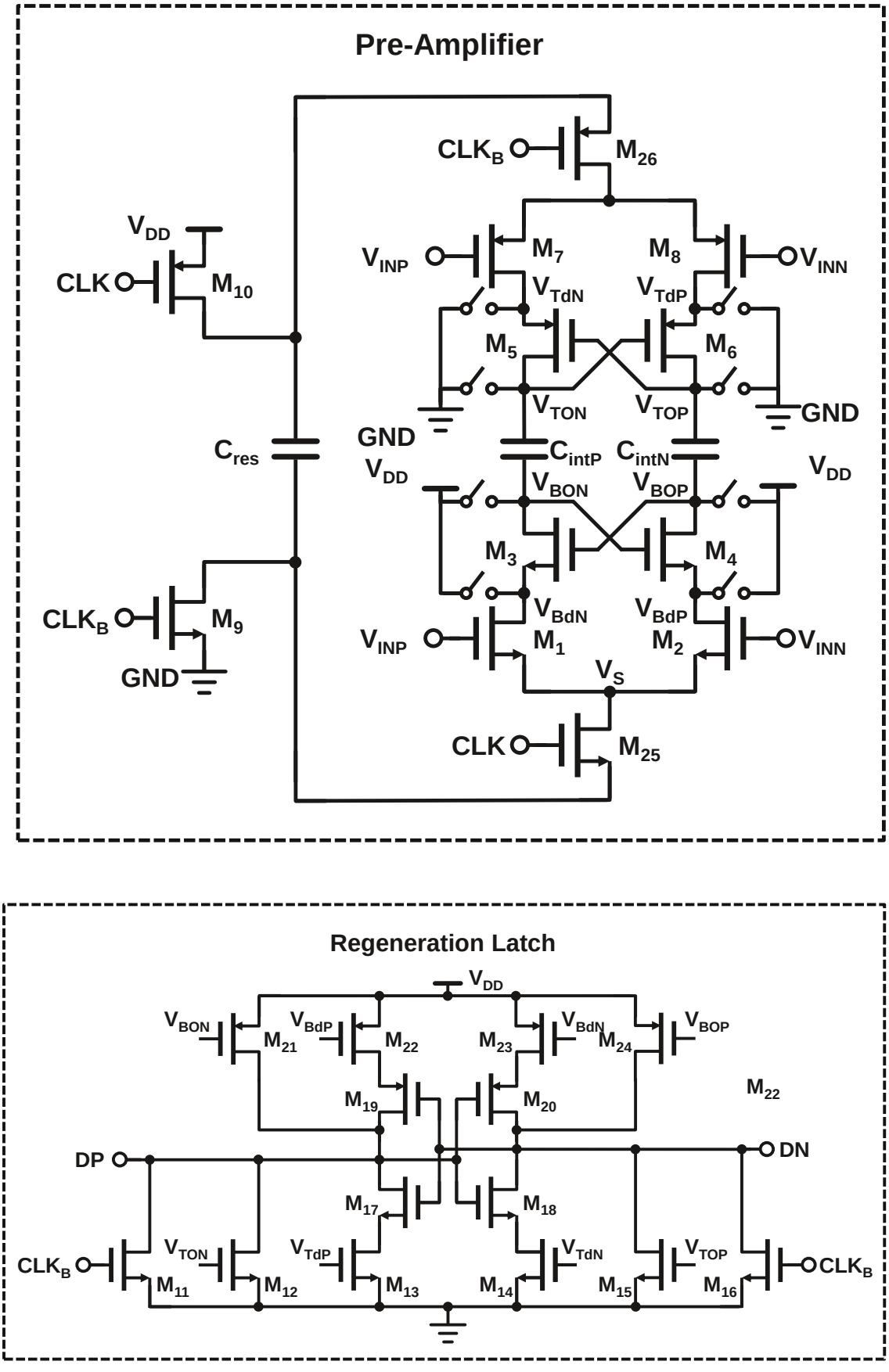


Figure 4.1: Proposed gain boosting DCA based comparator.

Table 4.1: Transistor size of proposed comparator.

Transistor	Size [μm]
$M_{1,2,7,8,25,26}$	$4/0.06$
$M_3 \sim M_6$, $M_{11} \sim M_{24}$	$0.25/0.06$
M_9	$1/0.06$
M_{10}	$2/0.06$

When the comparison starts ($CLK = 1$), the reservoir capacitor powers the gain boosting DCA and forms an isolated voltage domain for the gain boosting DCA. The common-mode current remains constant thanks to the isolated voltage domain, thus achieving the common-mode variation insensitivity [73]. The reservoir capacitor has achieved partial discharging similar to the dynamic bias comparator [72]. Also, it has achieved current reuse during comparison. Therefore, the proposed gain boosting DCA achieves low power consumption.

4.2 Design of Gain Boosting Dynamic Capacitive Pre-Amplifier

The initial states of the proposed gain boosting DCA are set to V_{DD} or GND. Hence, the V_{DS} is larger than that of the FIA, whose initial states are set to V_{CM}. Assume that the input differential voltage is small ($V_{IN,diff} = 1\,mV$) and the input common-mode voltage is high enough to make the PMOS input pair cutoff. In the case of the FIA, if the V_{DS} of the NMOS input pair has only about $V_{DD}/2$, it will operate in

the triode region, resulting in speed degradation. It could not even operate at those input common-mode voltages. These results can be seen in [73]. On the other hand, the larger V_{DS} of the proposed gain boosting DCA ensures that the NMOS input pair could operate at saturation region in full-scale V_{CM}. Therefore, the proposed gain boosting DCA has achieved a full-scale input range and high-speed operation.

During the amplification phase, from the perspective of NMOS operation, the precharged parasitic capacitors of the nodes BdP and BdN start discharge first at a different rate depending on the input voltage difference. The reservoir capacitor C_{res} is charged and gradually turns off the tail current source M_{25}. As a result, the parasitic capacitors of the nodes BdP and BdN discharge partially, thus saving power. However, this decreases the speed of the comparator due to the partial discharge. The partial discharge decreases the speed of the pre-amplifier and the voltage difference $|V_{BdP} - V_{BdN}|$ of the BdP and BdN. However, the speed of the regeneration latch is determined by the voltage difference $|V_{BdP} - V_{BdN}|$. Thus, the speed of the comparator becomes slow due to the dynamic bias. The dynamic bias comparator and CSPC both suffer from low-speed operation.

To increase the output voltage difference of the pre-amplifier, the cross-coupled pair (M_3-M_6) is added to the proposed gain boosting DCA. The positive feedback of the cross-coupled pair enhances the amplification of the proposed gain boosting DCA. As a result, the regenerative latch now exhibits a larger initial input voltage difference. The delay of the latch can be expressed as

$$t_{latch} = \frac{C_O}{g_{m,inv}} ln(\frac{V_{fnl}}{V_{init}}) \tag{4.1}$$

where the $g_{m,inv}$ is the transconductance of the inverter of the latch. As 4.1 indicated, increasing the initial input voltage difference reduces the delay. Therefore, the comparison speed also increases.

4.3 Design of Modified Regeneration Latch

For high-speed operation, the regeneration latch remains the cross-coupled inverter structure without any inserting transistor like the 2nd stage of the dynamic bias comparator [71]. On the other hand, the high-speed regeneration latch utilized in double-tail comparator [66] has a large through current and consumes much power due to the high through current [67, 68]. The proposed regeneration latch utilizes M_{13}-M_{14} and M_{22}-M_{23} as input pairs and current sources to reduce the through current. However, this decreases the speed of the regeneration latch operation. The amplification is small initially as the overdrive voltage of the M_{13}-M_{14} and M_{22}-M_{23} is small. To enhance the amplification, auxiliary input pairs M_{12}-M_{15} and M_{21}-M_{24} are added, and the output is directly connected to the DP and DN, not to the drain of M_{13}-M_{14} and M_{22}-M_{23}. It accelerates the turn-on speed of the M_{17}/M_{18}. Although the auxiliary input pairs cause another through current path, this through current flows for a very short time and, therefore, consumes almost no power.

Thanks to all the techniques mentioned above, the proposed gain boosting DCA based comparator achieves high-speed, low-power, and full-scale input range operation.

4.4 Simulation Results

For comparison, the double-tail comparator [66] and previously proposed regeneration enhancement comparator [67, 68] have been designed and simulated. As mentioned before, the CSPC is slow, and its delay is longer than the dynamic bias comparator with the charge pump [93]. Thus, it is not suitable for high-speed operation. All three comparators have similar noise around 470 mV at $V_{CM} = V_{DD}/2 = 0.6V$. The 1 LSB of the proposed SAR ADC is about 1.17 mV. The designed input referred noise is low enough to satisfy the required SNDR of the proposed SAR ADC. All

comparators have the same size of input pairs to have similar characteristics. To suppress the mismatch, the input pair is designed with a large size. The common-mode voltage of the proposed switching scheme of CDAC decribed in Chapter 5 is greater than the $V_{DD}/2$. As a result, the NMOS input pair serves as the primary input pair and the PMOS input pair of the proposed gain boosting DCA based comparator is designed with the same size. The regeneration latch of all comparators is designed to be the same size, although the latch architecture is different. The input differential voltage $V_{IN,diff} = 1mV$ with $V_{DD} = 1.2$ V and $f_S = 1GHz$ at $T = 300K$.

Fig. 4.2 shows the Energy/comparison as a function of V_{CM}. The double-tail comparator could not operate as V_{CM} smaller than 0.5 V. In the case of the regeneration enhancement comparator, it could not operate as V_{CM} smaller than 0.6 V. The proposed gain boosting DCA based comparator has the advantage of being able to operate across all V_{CM} regions ($0 \sim V_{DD}$).

Fig. 4.3 shows the CLK-Q delay as a function of V_{CM}. Only the proposed gain boosting DCA based comparator could compare at all V_{CM} regions ($0 \sim V_{DD}$). Also, it achieves a relatively stable delay. The delay of the other two comparators changes gradually depending on the V_{CM}. The results show the proposed gain boosting DCA is based comparator is common-mode variation insensitivity.

At $T = 300K$, both the double-tail comparator and the gain boosting DCA based comparator can operate at high speed at the beginning. However, those comparators, which are common-mode sensitive, will suffer from speed degradation due to the increased V_{th} at $T = 4\,K$. The increased V_{th} results in the V_{GS} becoming small. It is equivalent to the V_{CM} decreasing at RT. The CLK-Q delay of the proposed gain boosting DCA based comparator is stable and, therefore, is suitable for both RT and $T = 4\,K$ thanks to the common-mode insensitivity.

Fig. 4.4 shows the offset as a function of V_{CM}. The proposed gain boosting DCA based comparator is competitive with the previously proposed comparator and has a lower offset than the double-tail comparator. At $T = 4\,K$, the offset is expected to

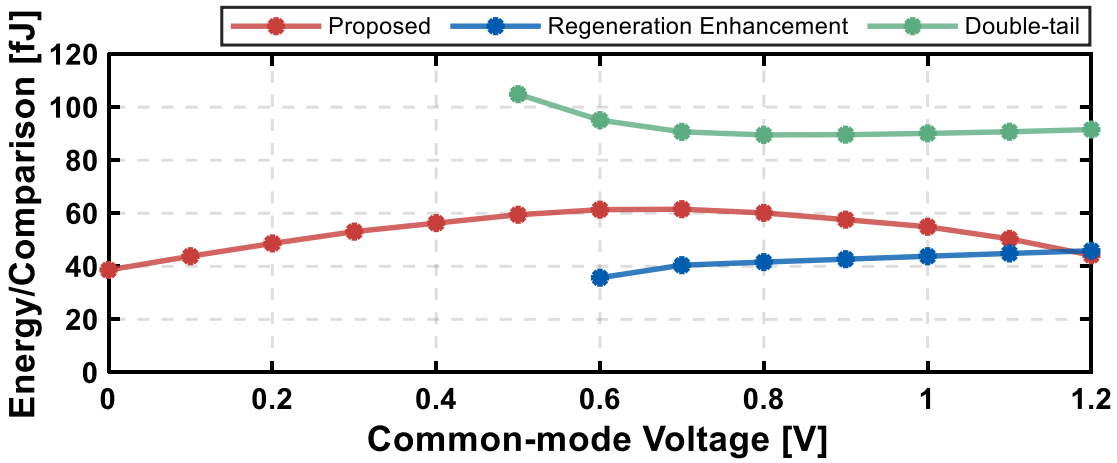


Figure 4.2: Energy per comparison versus common-mode voltage.

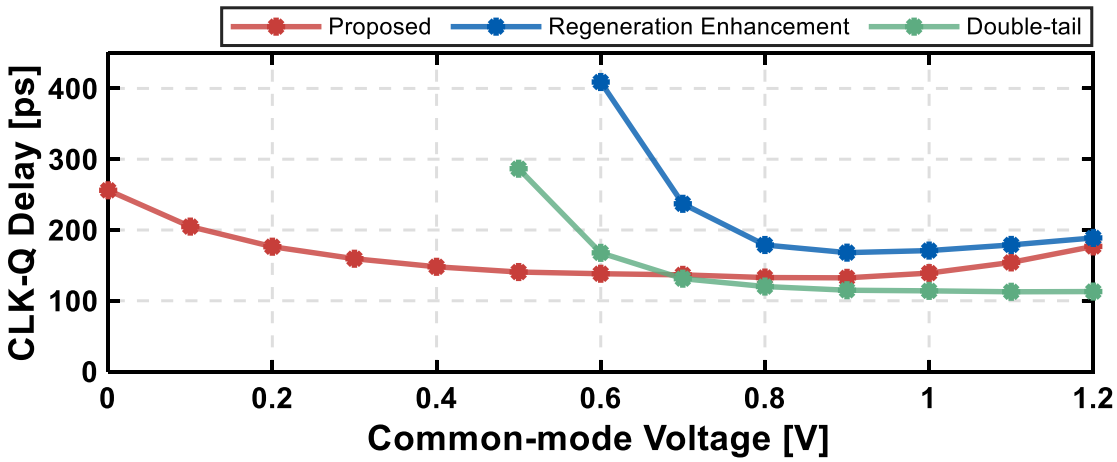


Figure 4.3: Clock-to-Q delay versus common-mode voltage.

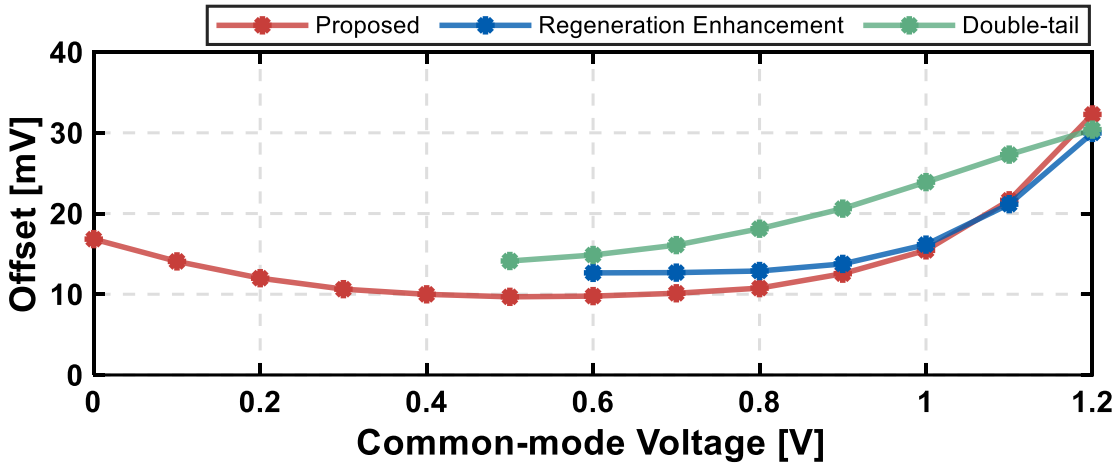


Figure 4.4: Offset versus common-mode voltage.

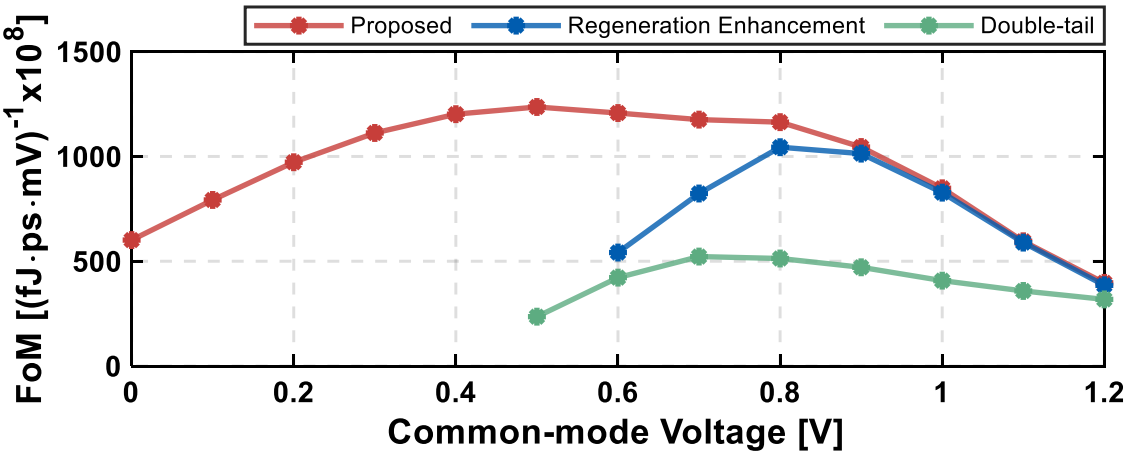


Figure 4.5: FoM versus common-mode voltage.

become more severe due to the increased mismatch. Therefore, the proposed gain boosting DCA based comparator is expected to perform well even at $T = 4\,K$.

The FoM, including power, delay, and offset, is defined in [30, 52], and it can be expressed as

$$FoM = \frac{1}{Power \cdot Delay \cdot Offset} \tag{4.2}$$

Fig. 4.5 shows the FoM versus the common-mode voltage V_{CM}. The proposed gain boosting DCA based comparator has achieved the best FoM around $V_{DD}/2$ ($V_{CM} = 0.4 \sim 0.8V$).

The FoM indicates that to ensure the comparator operates at the best performance, it is necessary to set the common-mode input voltage V_{CM} near $V_{DD}/2$. The relationship between the comparator's performance and SAR ADC's performance will be discussed in Chapter 5.

4.5 Conclusion

In this chapter, a gain boosting DCA based comparator is present. The proposed gain boosting DCA based comparator achieves input common-mode voltage insensitivity thanks to the isolated voltage domain by utilizing the reservoir capacitor. The reservoir capacitor also achieves the dynamic bias, enhancing energy efficiency. The comparison speed increases thanks to the large output voltage difference of the proposed gain boosting DCA. Full-scale resetting (to V_{DD} or GND) enlarges the V_{DS} and, therefore, achieves wide input range operation. The proposed regeneration latch suppresses through current and increases speed utilizing the auxiliary input pair.

Chapter 5

SAR ADC with Common-Mode Variation Suppression Switching Scheme

A 10-bit 60-MS/s SAR ADC adopting an energy-efficient common-mode variation suppression (CMVS) switching scheme is present in this chapter.

Fig. 5.1 shows the architecture of the proposed 10-bit SAR ADC. It is a differential architecture combined with the proposed gain boosting DCA based comparator, a set of differential CDAC arrays with switches, a set of differential bootstrapped switches for sampling, and SAR logic for control. For high-speed and high-accuracy sampling, the bootstrapped switch is designed with a quick turn-off technique and revised to improve the accuracy. The SAR logic implements the asynchronous control clock. The asynchronous control clock does not need a high-speed internal clock. It releases the internal clock from the worst case of the comparison period, which is the longest period, and therefore speeds up the conversion speed of SAR ADC. Utilizing the top plat sampling, the CDAC can reduce 1-bit since the MSB is directly conversion after sampling. It also saves the power consumption of the CDAC and improves the speed because of the reduction in capacitance. The pro-

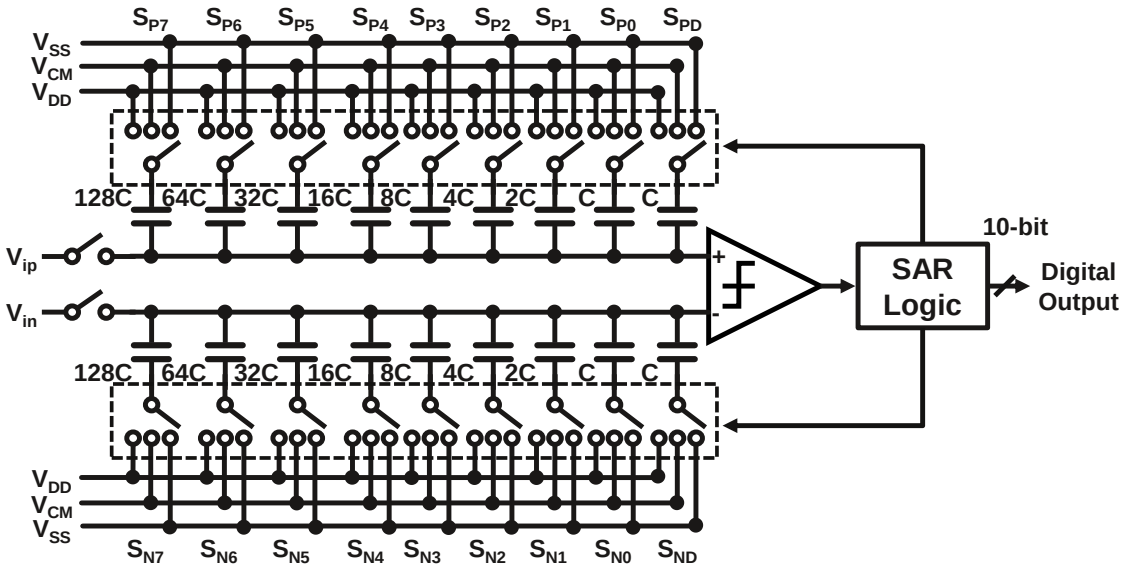


Figure 5.1: Architecture of the proposed 10-bit SAR ADC.

posed CMVS switching scheme adopts three reference voltages: supply voltage V_{DD}, half supply voltage V_{CM}, and ground V_{SS}. Thanks to the additional reference voltage V_{CM}, the proposed CMVS switching scheme can reduce 1-bit, exploiting the dummy capacitor of the CDAC. Therefore, the proposed SAR ADC only needs 8-bit CDAC to convert 10-bit data.

Following the details of the proposed CMVS switching scheme, the circuit implementation and the relationship between the comparator's performance and the SAR ADC's performance will be discussed.

5.1 Common-Mode Variation Suppression Switching Scheme

The 4-bit example of the proposed CDAC switching scheme is shown in Fig. 5.2 5.3, with the energy consumption of each conversion. Fig. 5.2 presents the sampling phase and the first 3-bit, while the switching process of the dummy capacitor is shown in Fig. 5.3. At the sampling phase, the initial state of the switches is precharged as a V_{CM} and V_{SS} crossing form, and the input signal is sampled and

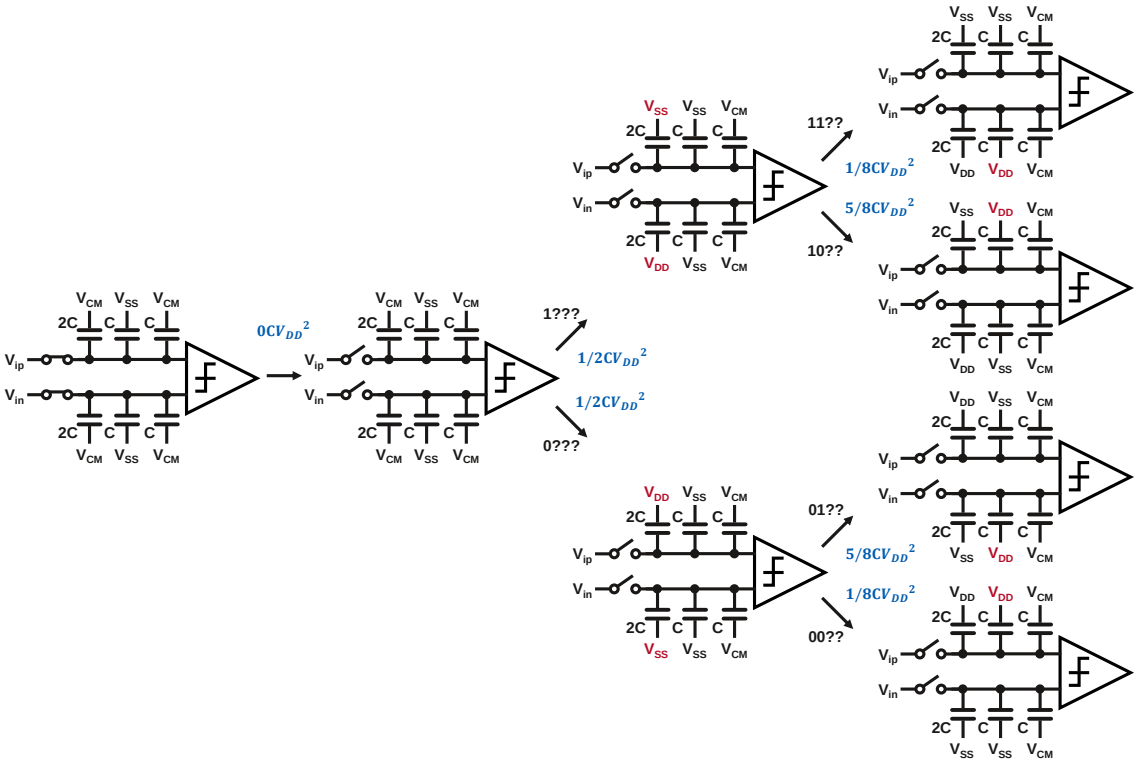


Figure 5.2: 4-bit example of the proposed common-mode variation suppression (CMVS) switching scheme: sampling and first 3-bit.

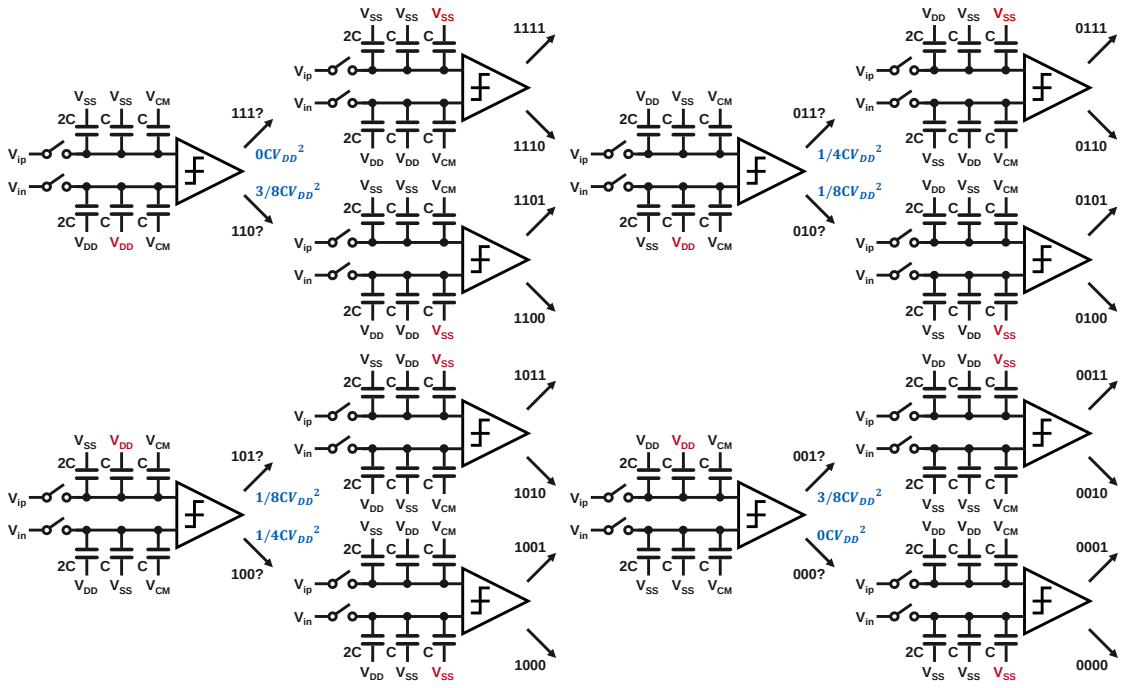


Figure 5.3: 4-bit example of the proposed common-mode variation suppression (CMVS) switching scheme: the last bit utilizing dummy capacitor.

held at the top plate of the CDAC. As mentioned before, the comparison of MSB needs no switching and, therefore, consumes no energy.

The switching behavior can be divided into three types: double-side switching, one-side-up switching, and one-side-down switching. The double-side switching is for the capacitor, which is precharged to V_{CM}. In this case, it is all the odd capacitors except for the dummy capacitor. The one-side-up switching is for the capacitor, which is precharged to V_{SS}. In this case, it is all the even capacitors. The one-side-down switching is for the dummy capacitor to convert one more bit. After the MSB comparison, according to the result, the double-side switching of the first odd capacitor (MSB) starts and generates the new reference voltage. If the MSB = 1, the P-side switches from V_{CM} to V_{SS}, and the N-side switches from V_{CM} to V_{DD}. Each side changes $1/4V_{DD}$, and the total is $1/2V_{DD}$, which means the input difference $V_{ip} - V_{in}$ is greater than $1/2V_{DD}$ or not. If the MSB = 0, the switching is vice versa. Next, the one-side-up switching of the following even capacitors (MSB-1) stars generates the new reference voltage. If the output of the comparator is 1, the N-side CDAC is charged from V_{SS} to V_{DD}. The P-side keeps the previous switching setting, and the top plate voltage of the P-side CDAC remains unchanged. If the output of the comparator is 0, the P-side CDAC is charged from V_{SS} to V_{DD}. The N-side CDAC remains unchanged. The one-side-down switching for the dummy capacitor is shown in Fig. 5.3. As mentioned before, this can convert one more bit without increasing the resolution of CDAC. If the output of the comparator is 1, the dummy capacitor of P-side CDAC discharges from V_{CM} to V_{SS}. Similar to the one-side-up switching, the N-side CDAC remains unchanged. If the output of the comparator is 0, the dummy capacitor of the N-side CDAC discharges from V_{CM} to V_{SS}, and the P-side CDAC remains unchanged.

The double-side switching operating before the one-side-up switching can suppress the common-mode voltage. The common-mode variation remains constant by setting a new reference voltage from the opposite direction, as in the previous

state. In contrast, the one-side switching, whether it is up or down switching, will cause the common-mode voltage variation. The voltage change is bigger than the following conversion. For instance, the voltage change is $1/2V_{DD}$ for MSB and is $1/4V_{DD}$ for MSB-1. Therefore, applying the double-side switching to the bigger voltage change results in a smaller common-mode variation throughout the entire conversion process. It will effectively suppress the common-mode variation and improve and stabilize the performance of the SAR ADC.

Fig. 5.4 shows the common-mode voltage variation of the proposed and the tri-level alternative [77] switching scheme. Both are normalized to the supply voltage V_{DD}. The common-mode voltage variation of the proposed CMVS switching scheme is $0.166V_{DD}$, which is lower than the $0.25V_{DD}$ of the tri-level alternative switching scheme. The lower the common-mode voltage variation, the better the performance of the comparator and, therefore, SAR ADC [80]. Note that the common-mode voltage variation of the proposed CMVS switching scheme goes to higher than $V_{CM} = 1/2V_{DD} (> 0.5)$ during conversion. On the other side, those of the tri-level alternative switching scheme become lower than V_CM. This different behaviour affects the performance of the comparator. The comparator has the best FoM near V_{CM} [67, 68, 80]. Therefore, to achieve the best performance of SAR ADC, it is better to design a switching scheme whose common-mode voltage variation is near V_{CM}. At $T = 4\,K$, the performance of the comparator worsens dramatically due to the increased V_{th} in the result. The comparison time will become several times longer than that at RT, as the pre-amplifier may operate in a subthreshold region. The higher $V_{CM} (> 0.5)$ of the proposed CMVS switching scheme helps to overcome this issue. The relation between the comparator's performance and V_{CM} will be discussed in more detail in next section.

The switching energy for each comparison is also shown in Fig. 5.2 and Fig. 5.3. For 10-bit SAR ADC, the switching energy versus digital code is calculated utilizing MATLAB, shown in Fig. 5.5. The average switching energy of the monotonic

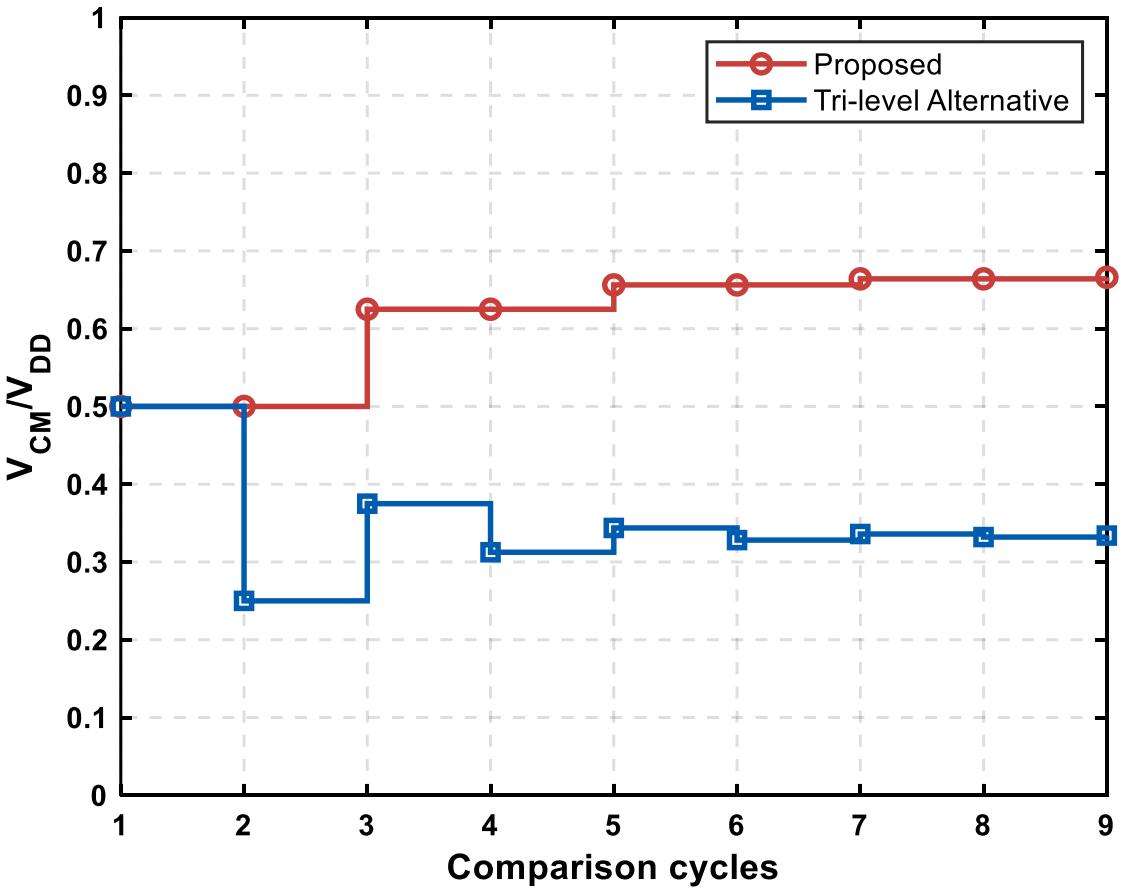


Figure 5.4: Normalized common-mode voltage variation.

and tri-level alternative switching scheme is $255CV_{ref}{}^2$ and $184.1CV_{ref}{}^2$, respectively [74, 77]. The tri-level alternative switching scheme reduces about 28% and 86% compared to the monotonic and conventional switching schemes. The average switching energy of the proposed CMVS switching scheme is $113.6CV_{ref}{}^2$. It reduces by about 56% and 92% compared to the monotonic and the conventional switching schemes, respectively.

Two types of CDAC switching schemes exist: those with reset energy and those without. The reset energy is the energy that the reference voltage sources consume to switch back from the final state to the initial state. In other words, from the LSB state to the sampling state for the subsequent conversion. The monotonic switching scheme has no reset energy since all the bottom plates of the CDAC are switched back to the same voltage V_{DD} [94], although it still consumes much energy and has

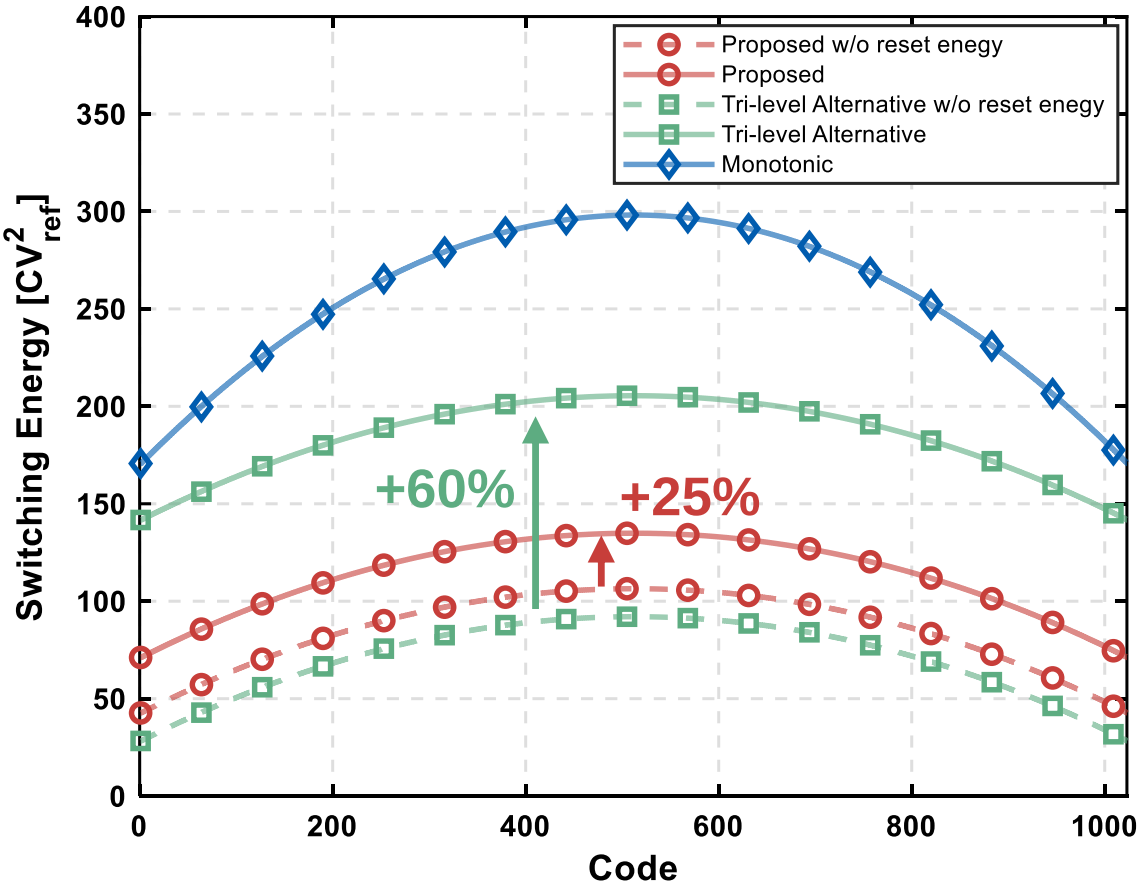


Figure 5.5: Switching energy versus output code.

a large common-mode variation. The tri-level alternative switching scheme, on the other hand, consumes less energy and has less common-mode variation. However, the bottom plates of the CDAC at the initial state of the tri-level alternative switching scheme are not connected to the same voltage, and thus, they consume reset energy. The reset energy accounts for about 60% of the average energy. It means that the tri-level alternative switching scheme has much worse energy efficiency. The proposed CMVS switching scheme consumes much less energy and has much less common-mode variation, with the reset energy accounting for about 25% of the average energy ($28.5CV_{ref}{}^2$). The change value of the charge determines the reset energy. An intuitive way is to see the difference in the common-mode voltage variation. As shown in Fig. 5.4, the common-mode voltage variation of the proposed

Table 5.1: Average switching energy of 10-bit SAR ADC.

Switching scheme	Average Energy* $[CV_{ref}^2]$	Reset Energy $[CV_{ref}^2]$	Common-Mode Variation	# of ref.
Conventional [76]	1365.3	0	0	2
Monotonic [75]	255.5	0	$0.5V_{DD}$	2
Bidirectional Single-side [77]	192	0	$0.25V_{DD}$	2
Tri-Level Alternative [78]	184.1	113.4	$0.25V_{DD}$	3
Adaptive-Reset [79]	138.2	0	0	3
MSB-block [80]	85.2	0	0	5
Proposed	**113.6**	**28.5**	$\mathbf{0.166V_{DD}}$	**3**

*The average energy is the total energy, including the reset energy.

CMVS switching scheme is small. It means that the change value of the charge when resetting to the initial state is also small and, therefore, consumes less energy to reset. Therefore, the proposed CMVS switching scheme has achieved high energy efficiency and a small common-mode variation switching scheme.

For comparison, Table 5.1 summarizes the average switching energy, reset energy, common-mode voltage variation, and the number of reference voltages (# of ref.) needed for the proposed switching scheme and others previously reported. Note that using too many reference voltages can burden the reference voltage buffer

with high accuracy requirements. From a system design perspective, the proposed CMVS switching scheme achieves a good balance by avoiding using too many reference voltage buffers.

5.2 Circuits Implementation

This section discusses the circuits implementing the proposed SAR ADC. First, the design of the high-speed and high-accuracy bootstrapped switch for sampling is discussed. Following that is the proposed gain boosting DCA based comparator. The relation between the CDAC switching schemes and the comparator's performance is also discussed in more detail. The SAR logic for implementing the proposed CDAC switching scheme concludes this section.

5.2.1 High-Speed and High-Accuracy Bootstrapped Switch

The bootstrapped technique is commonly applied to sampling switches for high linearity. A MOSFET switch or a transmission gate is also a commonly utilized switch. However, they suffer a large on-resistance variation due to the input voltage change. The on-resistance variation even becomes larger due to the increased V_{th} at $T = 4\,K$ [51, 53]. It decreases the linearity of the sampled signal [95]. Assuming an NMOS as a switch, the on-resistance of the NMOS becomes large when the input voltage is large due to the overdrive voltage becoming small. It makes the linearity of the sampled signal decrease further. To solve this problem, it is necessary to keep the on-resistance of the sampling switch at a stable and small value. This can be achieved utilizing the bootstrapped technique.

Fig. 5.6 shows the modified bootstrapped switch as a sampling switch utilized in the proposed SAR ADC [96]. Table 5.2 lists the size of the transistors. The bootstrapped switch utilized in the monotonic SAR ADC shares a similar structure without the M_7, M_9, and M_{13} [74]. The role of them will be discussed below.

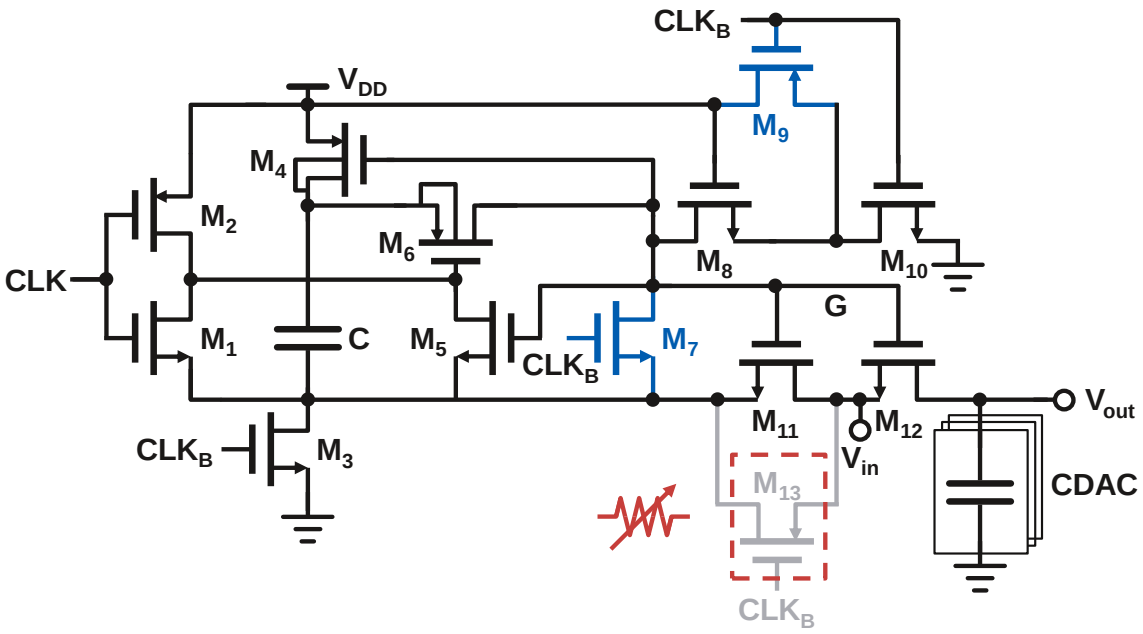


Figure 5.6: Modified bootstrapped switch.

During the hold phase ($CLK = 0$), the M_3 and M_4 turn on and charge the capacitor $C = 450\,fF$ to V_{DD}, which is utilized to bootstrap the input voltage. To reduce the distortion of the sampled signal, the sampling switch M_{12} is designed to be large to suppress the on-resistance variation. Also, it is necessary to turn off quickly. It is more critical at high-speed operation and can be achieved by discharging the parasitic capacitor at node G as quickly as possible. However, the sampling clock does not drive directly sampling switch M_{12}. The discharging of the parasitic capacitor at node G has to wait for the M_5 and M_6 to turn off and then discharge through M_8 and M_{10}. To avoid this waiting time, the M_7, directly driven by the sampling clock, shorts the gate (node G) and the source of the M_{11} and M_{12} when $CLK = 0$. This achieves a quick turn-off and improves the distortion of the sampled signal.

During the tracking phase ($CLK = 1$), the M_3, M_4, and M_7 turn off, and the M_{11} and M_{13} turn on. The sapling switch M_{12} turns on and tracks the input voltage. The M_5 pulls down the gate voltage of the M_6 to ensure the M_6 is on even if the input voltage equals V_{DD}. The bodies of the M_4 and M_6 are connected to the top plate of capacitor C since the voltage of the top plate may be greater than V_{DD}, and the

Table 5.2: Transistor size of bootstrapped switch.

Transistor	Size [μm]
$M_{1,5}$	1/0.06
$M_{2,3,4,7,8,10}$	2/0.06
M_6	4/0.06
$M_{9,11}$	0.5/0.06
M_{12}	10/0.06

body of PMOS has to connect to the highest voltage level. The M_9 is added to turn off the M_8 during the tracking phase to reduce the distortion. It decreases the total parasitic capacitance and prevents the leakage voltage of node G. The M_{13} and M_{11} form a transmission gate to accelerate turn-on speed by reducing the on-resistance [96]. However, this causes distortion and damages the accuracy of the sampled signal. The gate-source voltage of M_{11} is always V_{DD}, while the gate-source voltage of M_{13} is variable depending on the input voltage, resulting in the undesired on-resistance variation. Therefore, in our design, the bootstrapped switch removed the M_{13}, significantly improving the linearity without affecting the operation speed.

Table 5.3 summarizes the simulation results of the three bootstrapped switches utilized as a sampling switch and the CDAC as a hold capacitor. These are designed and simulated at $CLK = 200\,MHz$. The input signal is at Nyquist frequency. The signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) at node G and the SNDR of the sampled signal are shown. The modified

Table 5.3: Accuracy of bootstrapped switch.

	Node G		V_{out}
	SNDR [dB]	SFDR [dB]	SNDR [dB]
[75]	61.24	63.73	62.84
[97]	46.6	46.26	77.55
Modified	**61.80**	**64.61**	**80.14**

bootstrapped switch has a similar SNDR and SFDR at node G to the one utilized in monotonic SAR ADC. As mentioned before, the lowest SNDR and SFDR at node G of [30] is due to the undesired on-resistance variation. The SNDR of the sampled signal of the one utilized in monotonic SAR ADC is only 62.84 dB due to the speed limitation. It cannot turn off quickly, thus resulting in large distortion. The SNDR of the sampled signal of the one in [96] is 77.55 dB thanks to the quick turn-on/turn-off feature, even though the accuracy of the sampled signal is decreased due to the extreme distortion of node G. The modified bootstrapped switch has achieved better accuracy. The SNDR of the sampled signal is 80.14 dB. These results suggest that the modified bootstrapped switch could offer improved performance in ADC design.

5.2.2 Gain Boosting DCA Based Comparator

The CLK-Q delay changes with the V_{CM} changing as mentioned above. The common-mode voltage of the proposed CMVS switching scheme starts from $V_{DD}/2$ as shown in Fig. 5.4. At $T = 300\,K$, both the double-tail comparator and the gain boosting DCA based comparator can operate at high speed at the beginning. However, those comparators, which are common-mode sensitive, will suffer from speed degradation due to the increased V_{th} at $T = 4\,K$. The increased V_{th} results in the V_{GS} becoming small. It is equivalent to the V_{CM} decreasing at RT. The CLK-Q delay of the proposed gain boosting DCA based comparator is stable and, therefore, is suitable

for both RT and $T = 4\,K$ thanks to the common-mode insensitivity. It also allows the proposed SAR ADC to maintain high-speed operation even at $T = 4\,K$.

Fig. 5.7 (same as Fig. 4.5) shows the FoM versus the common-mode voltage V_{CM} of the proposed gain boosting DCA based comparator. The FoM indicates that to ensure the comparator operates at the best performance, it is necessary to set the common-mode input voltage V_{CM} near $V_{DD}/2$. The common-mode variation range of the switching schemes is also shown in Fig. 5.4. The proposed CMVS switching scheme not only has less common-mode variation but also keeps the variation in the region that has the best FoM, which is about $V_{CM} = 0.6 \sim 0.8V$. The tri-level alternative switching scheme, however, lets the common-mode voltage at a relatively low region and has large common-mode variation. It indicates that it may not be suitable for the NMOS-only input pair comparator, such as the double-tail or regeneration enhancement comparator. Although the proposed gain boosting DCA based comparator having CMOS input pair can work at the region smaller than $V_{DD}/2$ and have good FoM, the large common-mode voltage variation of the tri-level alternative switching scheme still degrades not only the performance of the comparator but also the performance of the SAR ADC, e.g. speed degradation, increasing offset. At $T = 4\,K$, it is expected that the equivalent V_{CM} will decrease due to the increased V_{th}. It means that the common-mode variation range of the switching schemes shit to the left to some level. The tri-level alternative switching scheme thus further degrades the performance of the SAR ADC. On the other hand, the proposed CMVS switching scheme still operates in the best FoM region. It performs stable utilizing the proposed comparator thanks to its common-mode variation insensitivity feature. Also, thanks to the proposed switching scheme slightly increasing the common-mode voltage, even though the V_{th} increases, the proposed comparator still operates at the best FoM region. Therefore, the proposed SAR ADC still achieves high-performance operation.

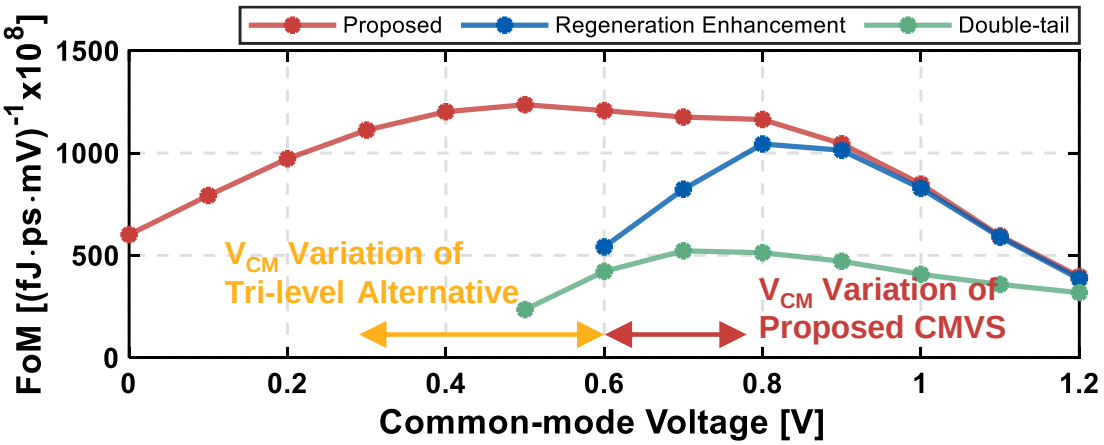


Figure 5.7: FoM versus common-mode voltage.

5.2.3 SAR Logic

The proposed SAR ADC utilizes asynchronous timing control, as mentioned before. This not only avoids the need for a high-speed clock generator but also releases the limitation of the slowest conversion period. Fig. 5.8 shows the counter, which serves as an internal clock generator, and the waveform of the asynchronous operation of the SAR ADC. Here, the reset of the D flip-flop is omitted. The F_s is the external sampling clock signal with a duty cycle of 20%. When the sampling is completed, the F_s turns from HIGH to LOW and generates the first comparison clock for the comparator. Once the comparison is done, the signal $READY$ goes $HIGH$, triggering the counter. The counter then generates the internal clock $CK_{9\sim0}$ to control the switch of CDAC for data storage and output. Fig. 5.9 shows the D flip-flop bank for data storage. The reset of a D flip-flop is also omitted.

As mentioned before, the proposed CMVS switching scheme has three types of switching. The control circuits and the truth table for double-side switching are shown in Fig. 5.10 (a). The bootstrapped switch (BSSW) is utilized for delivering the reference voltage V_{CM} at $T = 4\,K$. At RT ($T = 300\,K$), there is no problem utilizing an NMOS switch or transmission gate. However, the threshold voltage V_{th} of the MOSFET becomes higher at $T = 4\,K$. Thus the overdrive voltage becomes closer

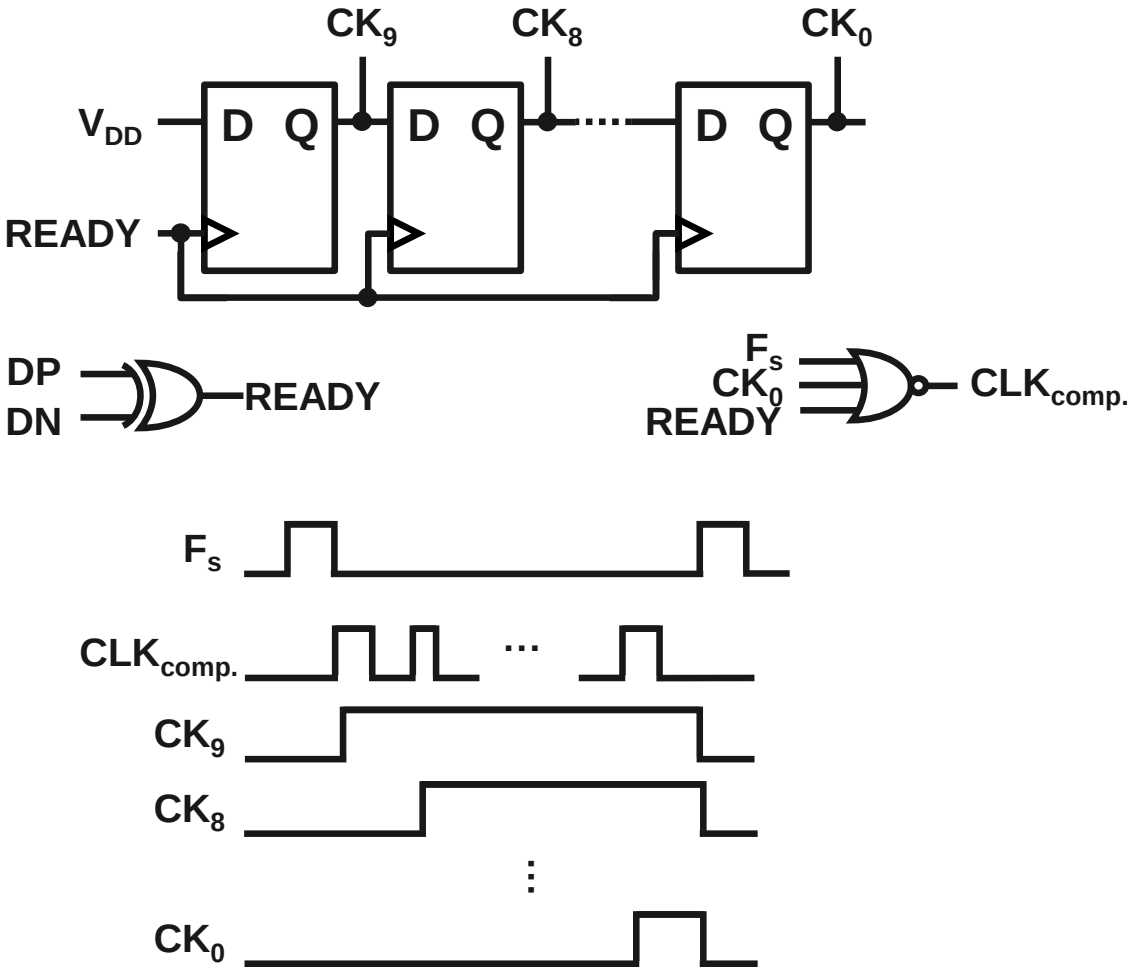


Figure 5.8: Asynchronous timing control circuits and waveform.

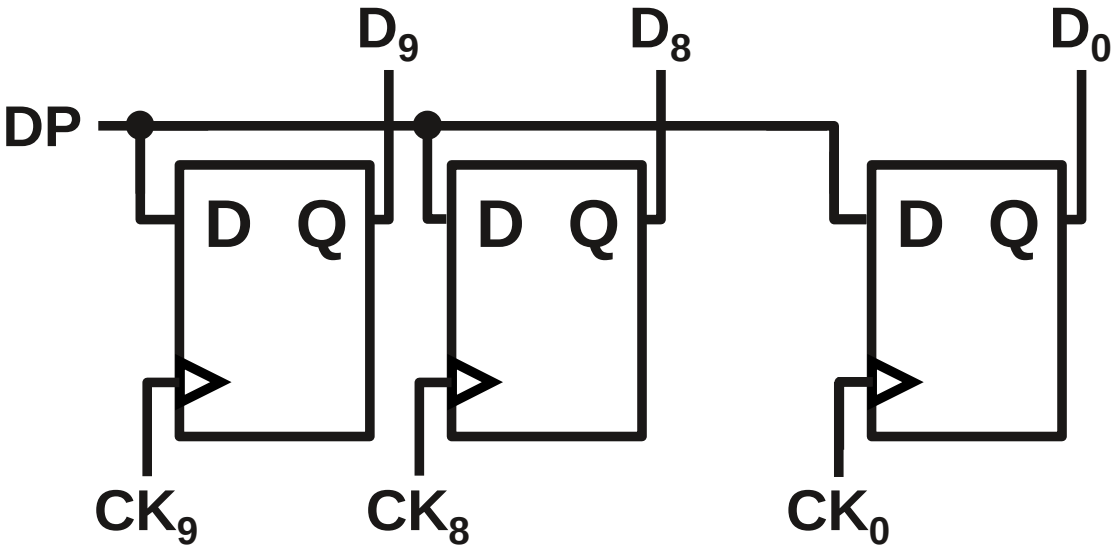
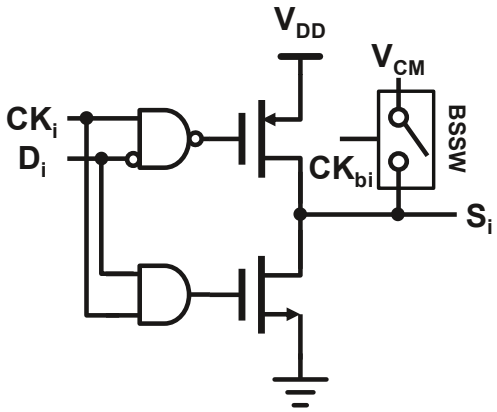


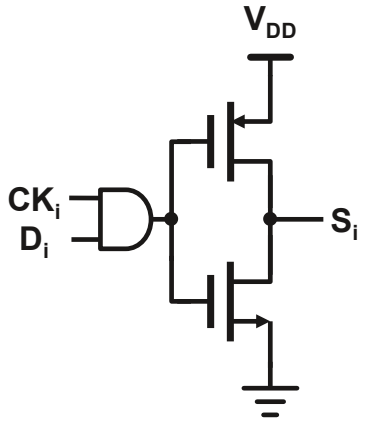
Figure 5.9: D flip-flop bank for data saving.



Ck_i	D_i	S_i
0	0	1
0	1	1
1	0	0
1	1	1

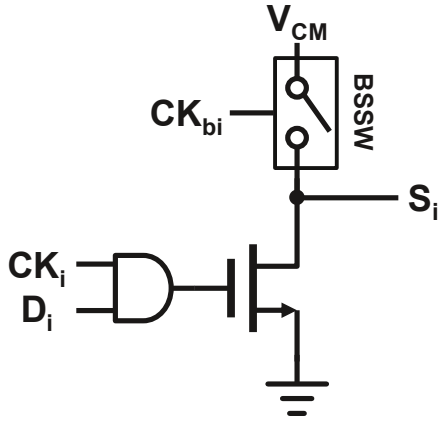
Ck_i	D_i	S_i
0	0	0
0	1	0
1	0	0
1	1	1

(a)



Ck_i	D_i	S_i
0	0	1
0	1	1
1	0	1
1	1	0

(b)



Ck_i	D_i	S_i
0	0	0
0	1	0
1	0	0
1	1	1

(c)

Figure 5.10: Control circuits and the truth table for (a) double-side switching (b) one-side-up switching (c) one-side-down switching.

to the threshold voltage and makes the MOSFET hard to turn on, which means the on-resistance is high. This causes the time constant RC to become too long. As a result, it needs a very long settling time to charge the bottom plate of CDAC to V_{CM}. The overdrive voltage of the BSSW is always V_{DD} ideally. Although utilizing BSSW increases the area and a little power consumption, it is a good solution to ensure SAR ADC operates properly both at $T = 300\,K$ and $4\,K$.

Fig. 5.10 (b) shows The control circuits and the truth table for one-side-up switching. This switching does not need V_{CM}, so the circuits are more simple. When the $CK = 1$, if $D_i = 1$, the PMOS turns on and charges the bottom plate of N-side CDAC from V_{SS} to V_{DD}. If $D_i = 0$, the bottom plate of P-side CDAC is charged from V_{SS} to V_{DD}. The NMOS is for reset. Fig. 5.10 (c) shows the control circuits and the truth table for one-side-down switching for the dummy capacitor of CDAC. The BSSW is utilized for resetting to V_{CM}. When the $CK = 1$, if $D_i = 1$, the NMOS turns on and discharges the bottom plate of P-side CDAC from V_{CM} to V_{SS}. If $D_i = 0$, vice versa.

5.3 Simulation Results

The proposed single-channel 10-bit 60-MS/s SAR ADC has been designed and simulated utilizing 65-nm cryo-CMOS technology with $V_{DD} = 1.2V$ at $T = 300\,K$ and $T = 4\,K$. The design and simulation are utilizing Virtuoso Custom IC Design Environments and MATLAB.

Fig. 5.11 shows the layout of the proposed SAR ADC. Considering the limitation of the kT/C noise and the conversion speed, the unit capacitance is designed to be 1.6 fF. The total capacitance is 409.6 fF, which is implemented utilizing metal-insulator-metal (MIM) capacitors.

Fig. 5.12 and Fig. 5.13 shows the 1024-point FFT results of the post-layout simulation at $T = 300\,K$ and $T = 4\,K$ with transient noise. At $T = 300\,K$, the proposed SAR ADC operates at 55-MS/s, with the input signal is at Nyquist frequency. The

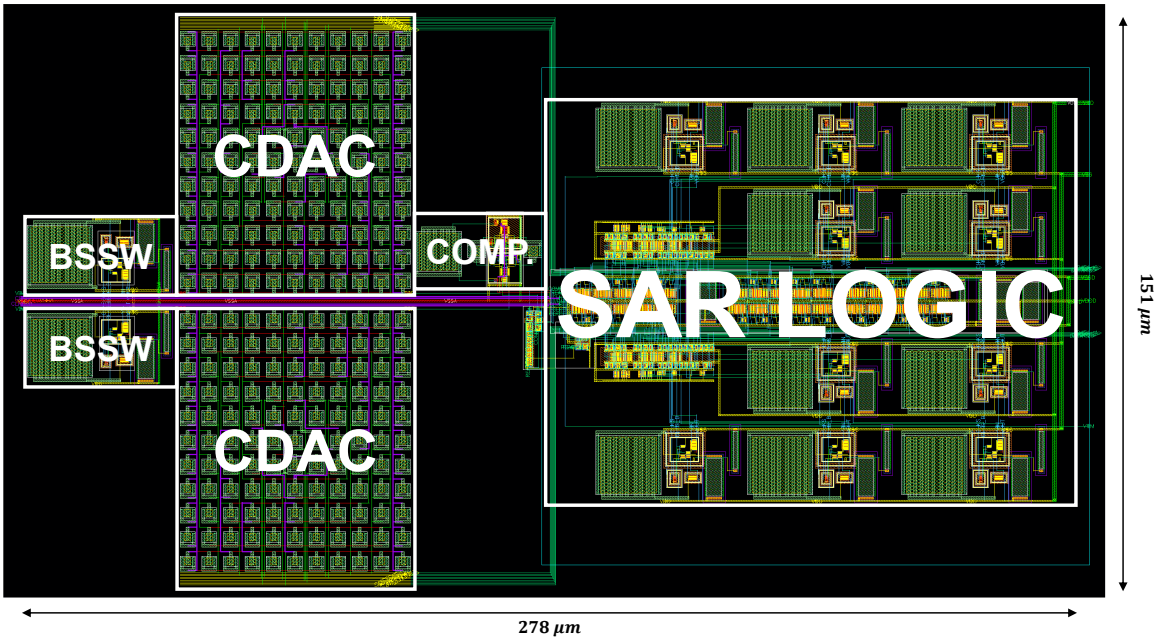


Figure 5.11: The layout of the proposed SAR ADC.

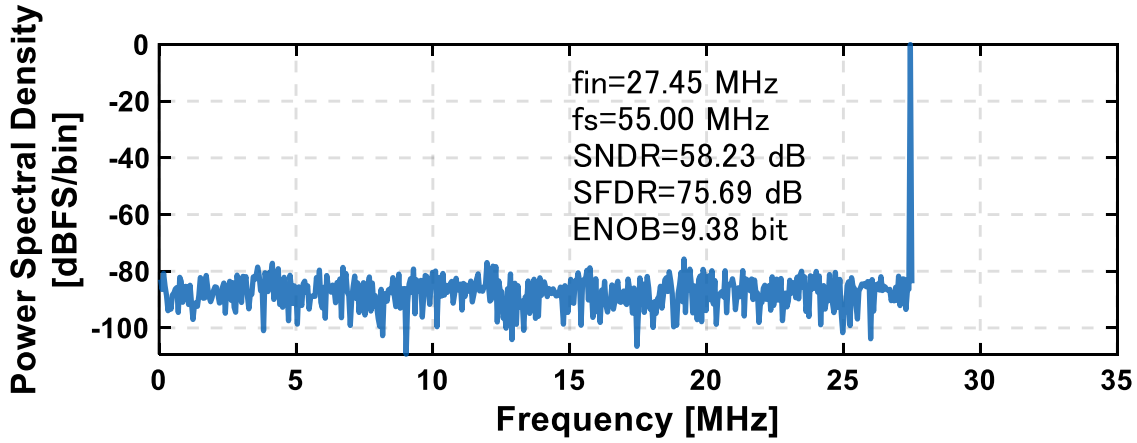


Figure 5.12: Simulated FFT spectrum at $T = 300\,K$.

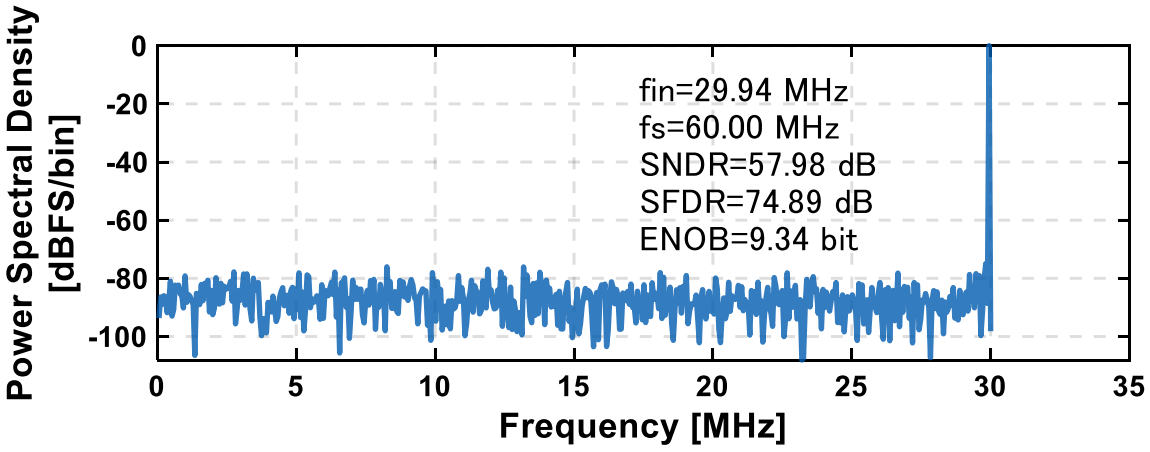


Figure 5.13: Simulated FFT spectrum at $T = 4\,K$.

Table 5.4: Performance at different corner @ $T = 300\,K$.

Supply Voltage [V]	Corner	Sampling Frequency [MHz]	ENOB [bit]	SNDR [dB]	SFDR [dB]
1.1	SS	35	9.67	59.98	76.79
	TT	60	9.73	60.35	77.92
	FF	95	9.78	60.63	76.84
1.2	SS	40	9.74	60.40	78.65
	TT	70	9.69	60.06	75.32
	FF	105	9.68	70.02	77.35
1.3	SS	50	9.66	59.90	74.69
	TT	80	8.97	55.74	74.32
	FF	120	9.70	60.15	76.56

effective-number-of-bits (ENOB) is about 9.38-bit. At $T = 4\,K$, the speed degradation due to the increased V_{th} and the speed improvement due to the increased drain current cancel each other out to some extent. As a result, the ADC operates at 60-MS/s. The ENOB is about 9.34-bit. The proposed SAR ADC has achieved a performance that is as good as that of RT.

Table 5.4 shows the sampling frequency, ENOB, SNDR, and SFDR at different supply voltages and corners at $T = 300\,K$. Although the proposed comparator with the proposed CMVS switching scheme is robust against the V_{th} variation to a certain extent, the speed of digital circuits is significantly affected. Thus, the conversion speed changes across different corners. The proposed SAR ADC is designed to be robust for temperature. This robustness is demonstrated in Fig. 5.14, which presents simulation results under different temperatures. Fig. 5.14 shows the results of SNDR and SFDR, while Fig. 5.15 shows the ENOB at different temperatures. The SNDR, SFDR, and ENOB remain consistently stable across a wide temperature range. This robustness shows that the proposed SAR ADC can operate in a wide temperature range.

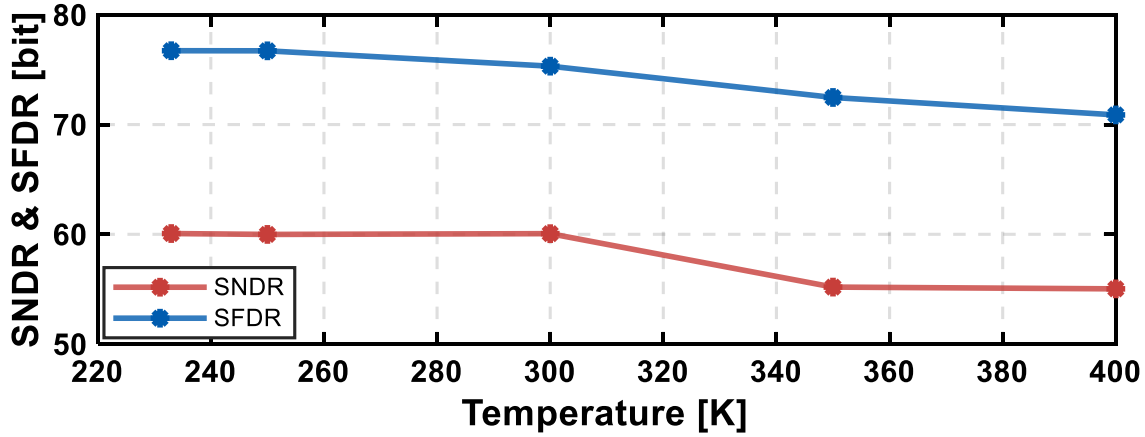


Figure 5.14: Simulated SNDR and SFDR versus temperature.

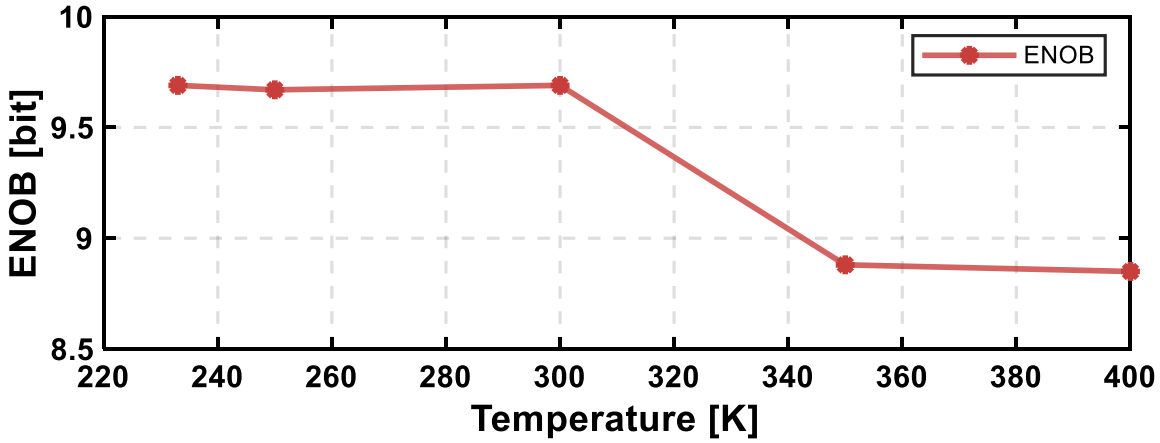


Figure 5.15: Simulated ENOB versus temperature.

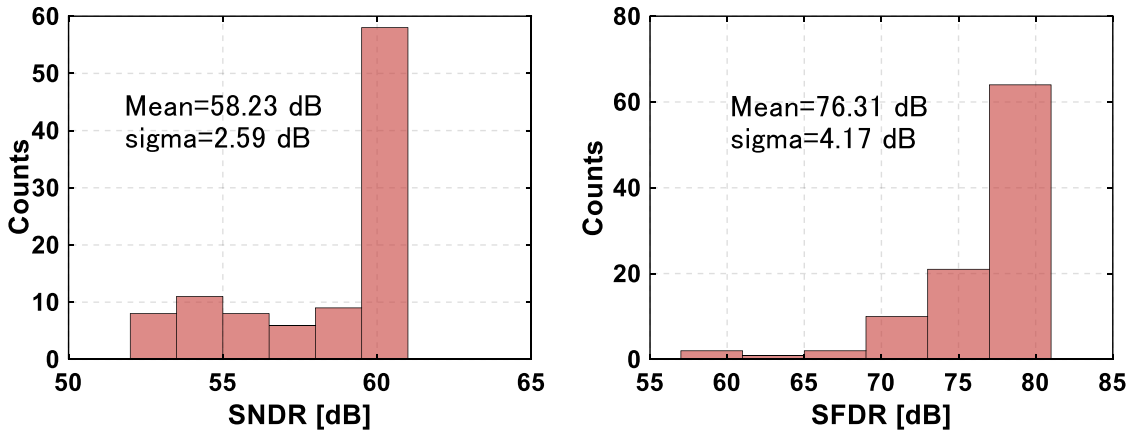


Figure 5.16: Monte Carlo simulation results of SNDR and SFDR.

Table 5.5: Performance comparison of SAR ADC.

	This work (Post-layout Simulation*)		ESSCIRC '14 [77]	TVLSI '16 [78]	TCAS II '20 [79]	ESSCIRC '23 [54]	JSSC'23 [55]		TCAS I'24 [56]	
Architecture	**SAR**		SAR	SAR	SAR	TI SAR (4x)	TI SAR (2x)		TI SAR (2x)	
Temperature [K]	**300**	**4**	–	–	–	4	300	4.2	300	4.2
Technology [nm]	**65**		180	90	65	40	40		40	
Supply Voltage [V]	**1.2**		1	0.5	0.5	1/1.25	1.1 (core) 2.5 (clock)		1.1	
Sampling Rate [MS/s]	**55**	**60**	1	1.28	3	500	900	1000	900	1000
Resolution [bit]	**10**		11	10	10	7-10	6-8		7	
ENOB [bit]	**9.38**	**9.34**	10.3	9.17	8.78	8.03[a]	5.26	5.72	6.05	6.14
SNDR [dB]	**58.2**	**58**	63.4	57	54.6	50.1[a]	33.4	36.2	38.2	38.7
SFDR [dB]	**75.7**	**74.9**	76.6	68.8	71.8	59.1[a]	48.4	48.5	>50	>50
Power Dissipation [uW]	**563.93**	**550.29**	24	3.45	3.09	5910[a]	700[b] (10300[c])	800[b] (10600[c])	1870	1790
FoM [fJ/conv.-step]	**15.39**	**14.15**	19.9	4.68	2.34	45.1[a]	20[b] (260[c])	15[b] (200[c])	31.3	25.4
Area [mm^2]	**0.042**		0.1	0.06	0.022	0.147	0.045		0.042	

*Except for this work, the other works are the measurement results.
[a]10b, 500 MS/s [b]6b, ADC core [c]6b, ADC core + clock receiver + sampling switch

Fig. 5.16 shows the 100-time Monte Carlo simulation results of SNDR and SFDR at $T = 300\,K$. Compared to the V_{CM}-based switching scheme with mismatch calibration [97], the results show that the proposed switching scheme has a smaller standard deviation of the SFDR. The proposed SAR ADC achieves high linearity and accuracy despite not adopting any mismatch calibration techniques. Therefore, the results show sufficiently the effectiveness of the proposed switching scheme.

Table 5.5 compares the proposed SAR ADC with the other ADC. Although the results shown are post-layout simulation results, it still shows that the proposed SAR ADC is competitive at both $T = 300\,K$ and $T = 4\,K$. The proposed SAR ADC stands out with the best FoM at $T = 4\,K$, making it a good candidate for low-power and high-speed TI SAR ADC. The prior art utilizing the tri-level alternative switching scheme [77] is unsuitable for cryogenic application due to the expected significant performance degradation at $T = 4\,K$, as discussed earlier. The prior art [78] achieves a good FoM by utilizing the near-threshold voltage (NTV) optimized design. However, the performance of NTV-optimized circuits is expected to degrade significantly

due to the increased V_{th} at $T = 4\,K$. Therefore, the proposed SAR ADC is suitable for low-power and high-speed cryogenic applications.

5.4 Conclusion

In this chapter, a 10-bit 60-MS/s SAR ADC utilizing the proposed energy-efficient common-mode variation suppression (CMVS) switching scheme is present. The proposed CMVS switching scheme can suppress the common-mode variation to no greater than $0.166V_{DD}$. It also saves much reset energy of only $28.5CV_{ref}{}^2$. It reduces about 92% of energy consumption than the conventional switching scheme. The common-mode voltage of the proposed CMVS switching scheme ensures that the comparator operates in the best-FoM region. The simulation results show the proposed SAR ADC achieved FoM of 15.39 fJ/conversion-step with 55-MS/s and 14.15 fJ/conversion-step with 60-MS/s at $T = 300\,K$ and $T = 4\,K$.

Chapter 6

Conclusion

6.1 Thesis Summary

This thesis presented a cryo-CMOS low-power and high-speed SAR ADC as a part of the read-out circuits for qubits reading. FTQCs, for general-purpose applications, require more than several thousands of qubits, while the number of qubits of the latest QC has just achieved around one thousand. The number of cables that interface with a quantum processor operating at several mK between the classical control & read-out circuits placed at room temperature ($T = 300\,K$) thus increases and causes the limitation for increasing qubit. A low-power and high-speed cryo-CMOS read-out circuit operating at cryogenic temperatures ($T = 4\,K$) addresses these issues and is required to reduce the number of cables.

Chapter 1 described the principle of the QCs and summarised the popular types of qubits. The target specification for the control & read-out circuits of quantum computers was also described. The limited cooling capacity of the dilution refrigerator determines the power consumption of the control & read-out circuits to be below 1 W. The limited coherence time and the number of qubits determine the required sampling frequency of ADC. Therefore, the read-out circuit requires a low-power (several mW) and high-speed (several tens MS/s ~ several GS/s) ADC.

Chapter 2 described the characteristics of cryogenic CMOS based on semiconductor physics. It indicated the challenges and issues in cryogenic circuit design, such as the increased threshold voltage V_{th} and mismatch. The critical cycle of SAR ADC was addressed. It indicated that improving the performance of the comparator is a straightforward approach to improving the performance of SAR ADC. Dynamic comparators were reviewed and discussed, primarily focusing on popular pre-amplifier architectures. The power consumption and speed of the pre-amplifiers were mainly discussed. Some low-power switching schemes of SAR ADC were reviewed. Although these have achieved low power consumption, the performance degrades due to the increased V_{th} at cryogenic temperatures. This chapter indicated that cryo-CMOS SAR ADC requires a design that addresses those cryo-CMOS issues.

Chapter 3 described the proposed high-speed and low-power CMOS two-stage dynamic comparator. The pre-amplifier achieves low power consumption thanks to the dynamic bias technique while suffering from speed degradation. Increasing the output voltage difference by inserting a StrongARM latch in the pre-amplifier improves the speed of the latch in the 2^{nd} stage and thus increases the speed. The latch also achieves low power consumption by replacing the tail current source as the input pair, which suppresses the through current. The cross-coupled inverter pair and the auxiliary input pair in the latch enhance the regeneration and thus improve the speed.

The delay analysis was given. It showed that the above techniques are effective in increasing speed. The dual latch structure is effective in increasing speed. Also, it provides a deep understanding and good intuition for circuit design. Considering the design of the pre-amplifier, increasing C_t for dynamic bias, increasing the tail current, and decreasing the capacitance at the drain node of the input pair reduce the delay. Considering the design of the latch in the 2^{nd} stage, decreasing the tail current and increasing the transconductance g_m of the input pair reduce the delay.

Note that there are trade-offs in the tail current design and mismatch considerations.

The proposed comparator achieves a CLK-Q delay of 162.1 ps and 295.4 ps at $V_{id} = 1\,mV$ and $V_{CM} = 0.7\,V$ with $V_{DD} = 1.2\,V$ and $f_s = 1\,GHz$ in $T = 300\,K$ and $4\,K$. The energy per comparison is 34.04 fJ/comparison and 27.75 fJ/comparison. It is at the same level as the dynamic bias comparator while being faster than both the dynamic bias and double-tail comparator.

Chapter 4 described the proposed gain boosting dynamic capacitive pre-amplifier (DCA) based comparator. The proposed comparator achieves low power consumption thanks to the dynamic bias and current reuse techniques adopted in the DCA. Also, the cross-coupled pair boost the gain and thus speeds up the comparison. The isolated voltage domain formed by utilizing a reservoir capacitor achieves the common-mode variation insensitivity and thus alleviates performance degradation due to common-mode variation. Full-scale input range operation is achieved by the larger initial drain-source voltage and CMOS input pair. Thanks to these techniques, the proposed comparator achieves a relatively stable and high performance even operating at $T = 4\,K$.

Chapter 5 described the proposed 10-bit 60-MS/s SAR ADC with the proposed energy-efficient common-mode variation suppression (CMVS) switching scheme. The proposed CMVS switching scheme reduces energy consumption by about 92% compared to the conventional scheme. It also saved much reset energy of only 28.5 $CV_{ref}{}^2$. It suppresses the common-mode variation to 16.6% full scale. The narrow common-mode variation makes the comparator and SAR ADC operate in the highest-performance region, thus achieving high accuracy. At $T = 4\,K$, the increased dynamic common-mode voltage alleviates the performance degradation of SAR ADC due to the increased V_{th}. The post-layout simulation results show the proposed SAR ADC achieved FoM of 15.39 fJ/conversion-step with 55-MS/s and 14.15 fJ/conversion-step with 60-MS/s at $T = 300\,K$ and $4\,K$. It shows that the proposed SAR ADC is suitable for low-power and high-speed cryogenic applications.

6.2 Future Works

To achieve FTQCs that require more than several thousands of qubits, the control & read-out circuits adopt the frequency multiplexing technique. Therefore, a high-speed (several hundred MHz ~ several GHz) ADC is required. This research has achieved a low-power 10-bit 60-MS/s SAR ADC. A time-interleaved ADC adopting the proposed SAR ADC is expected to increase speed and achieve low power consumption. The proposed SAR ADC can operate in a wide temperature range. It is better to adopt some PVT-robust techniques to improve the stability of the performance. It is an important issue such as for extreme environmental applications. The proposed CMVS switch scheme reduces the effect of the comparator's mismatch. It is a systematic approach. To further reduce the effect of mismatch, that is, to reduce the offset, it is better also to add a mismatch calibration technique to the comparator. These possible improvements must accelerate the realization of FTQCs and broaden the application.

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Publication List

Journals

1. Chia-Wei Pai, Ken Uchida, Munehiro Tada, and Hiroki Ishikuro, "A Cryo-CMOS 10-bit 60-MS/s SAR ADC with common-mode variation suppression switching scheme and gain boosting dynamic comparator," *Microelectronics Journal*, vol. 153, p. 106435, Nov. 2024.

2. Chia-Wei Pai, Ken Uchida, Munehiro Tada, and Hiroki Ishikuro, "Design and analysis of a high-speed low-power comparator with regeneration enhancement and through current suppression techniques from 4 K to 300 K in 65-nm Cryo-CMOS," *Microelectronics Journal*, vol. 144, p. 106066, Feb. 2024.

International Conferences

1. Chia-Wei Pai and Hiroki Ishikuro, "A High-Speed Low-Power Two-Stage Comparator with Regeneration Enhancement and Through Current Suppression Techniques", *Proceedings of the 66th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2023, Phoenix, USA)*, pp.79-83, 2023.

International Conferences (Other Works)

1. Chia-Wei Pai, Tatsuya Ishikawa, and Hiroki Ishikuro, "A Highly Linear Sensor System Using SEIR for Distortion Evaluation of Sensor Front-end", *The 23rd workshop on Synthesis And System Integration of Mixed Information technologies (SASIMI 2021, Online)*, pp. 14-18, 2021.

2. Tatsuya Ishikawa, Chia-Wei Pai, and Hiroki Ishikuro, "A Linearity Testing of Cascaded Analog Mixed-Signal Blocks Using SEIR Method," *Proceedings of the IEEE International Instrumentation and Measurement Technology Conference (I2MTC 2020, Online)*, pp. 1-6, 2020.