Load-Adaptive Active Gate Driver Integrated Circuit for Power Device

July 2023

Shusuke Kawai

A Dissertation for the Degree of

Doctor of Philosophy

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July 2023

Graduate School of Science and Technology

Keio University

Shusuke Kawai

Abstract

The electrification and automation of various devices will continue to advance toward the realization of a carbon-neutral society. One of the most important components to realize a carbon-neutral society is the power converter. The power converter consists of a power semiconductor and a control circuit. Power semiconductors have a loss-noise tradeoff. As power semiconductors become more advanced, the converter becomes more efficient, but noise is more likely to occur. To cope with noise, losses increase. Active gate techniques are a solution to break the trade-off between power device loss and noise. It solves the tradeoff by driving the power semiconductors with waveforms that match their condition. However there is no research on active gate driver techniques with load-adaptive functions integrated in a chip.

This thesis is a study of chip-integrated active gate drivers with load-adaptive functions. Chip-integrated active gate drivers were developed for both analog feedback and digital feedforward techniques.

Chapter 1 provides an introduction to this thesis. An overview of power electronics is given, and the importance of power converters is presented in terms of applications and power.

In Chapter 2, the fundamentals of active gate technique are presented, including the characteristics of each power device, the relationship between switching waveform and noise. Issues in terms of the characteristics of active gate technique and power devices are summarized.

In Chapter 3, an analog active gate driver IC using discrete-time feedback technique is proposed. Two resistors are controlled by the feedback technique to control the turn-on dV_d/dt of the SJMOS. Since the proposed technique feeds back the feedback result to the next switching, it can control the dV_d/dt that depends on the reverse recovery current. The results of successfully reducing the switching losses by 25% using the prototype IC are described.

In Chapter 4, an active gate driver IC using digital feed-forward technique is proposed, and a turn-off simulation analysis is performed considering the non-linearity of SiC-MOSFET capacitance. The active gate waveform that reduce the surge voltage is proposed based on the analysis. In addition, a time resolution extension circuit that reduce the amount of memory and

time resolution of the driver IC is proposed. The ADC integrated in the driver IC is used to detect the SiC-MOSFET load and output the active gate waveform according to the load, and the turn-off voltage surge is reduced by 51% without increasing the loss.

Chapter 5 presents the conclusions of this part and future research directions.

Acknowledgement

I would like to express my sincere gratitude and respect to my advisor, Professor Hiroki Ishiguro of the Faculty of Science and Technology at Keio University, for giving me this opportunity. I would like to thank Professor Ishiguro for his patience, inspiration, and encouragement.

I would also like to express my sincere gratitude to Professor Nobuhiko Nakano of Keio University, Full-time Lecturer Kentaro Yoshioka of Keio University, and Professor Makoto Takamiya of the University of Tokyo for agreeing to serve on the thesis committee, taking the time to review the paper, and providing valuable comments and suggestions that helped to make it more complete.

I would like to express my sincere gratitude to Dr. Kohei Onizuka, an experienced senior staff member of Toshiba Research and Development Center, and currently Deputy Director of Bristol Innovation Laboratory, Toshiba Europe Limited. He has provided me with opportunities and encouragement for my sometimes reckless design challenges, not to mention useful technical discussions. I greatly appreciate it. I would also like to express my heartfelt thanks to Mr. Takeshi Ueno of the Wireless System Laboratory, Toshiba Research and Development Center. Without Mr. Ueno, who accepted my technical discussions without refusal under any circumstances and did not hesitate to engage in lengthy discussions, this research could not have been carried out.

I would like to thank Dr. Tsuguhide Aoki, former head of the Wireless Systems Laboratory at Toshiba Research and Development Center, Dr. Ryoko Matsuo, current head of the laboratory, and Mr. Hiroaki Ishihara, program leader of my group, for their understanding and opportunities regarding my doctoral research. In particular, I would like to thank Mr. Hiroaki Ishihara for his various insights on design as well as technical discussions. I would like to express my gratitude to him.

I would like to thank Dr. Toshiya Mitomo, Dr. Koutarou Miyazaki, and Dr. Satoshi Takaya. I

am especially grateful to Dr. Mitomo for teaching me various techniques, of which I had no knowledge when I first joined the company.

Last but not least, I would like to thank my wife Saki and my son Kento for their constant support and cooperation, without which my research in this doctoral program would not have been possible.

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Chapter 1 Introduction

1.1 Power electronics

Power electronics is a technology related to the elements, circuits, and controls used in power converters [1]. As shown in Figure 1.1, power converters that convert electrical power into mechanical power or convert the quantity or type of electricity are used everywhere, including in electric equipment in the industrial field, in the generation and stabilization of renewable energy, in highly reliable power sources supporting the information society, and in social infrastructure such as power and mobility. Power converters are one of the most important devices supporting modern society. Figure 1.2 shows global power consumption by application [2]. Motors, which are a type of power converter, account for 40% to 50% of the world's total power consumption. In Japan, the number of motors for residential, commercial, and industrial use is approximately 100 million units, and their annual power consumption accounts for about 55% of the total power consumption in Japan. In 2020, the Japanese government announced the "2050 Carbon Neutral Declaration," which calls for a decarbonized society and virtually zero greenhouse gas emissions by 2050 [3]. The electrification and automation of equipment is expected to advance toward the realization of a carbon-neutral society. The importance of research and development in power electronics is increasing with the aim of improving the performance of power converters, which play a central role in the electrification and automation.

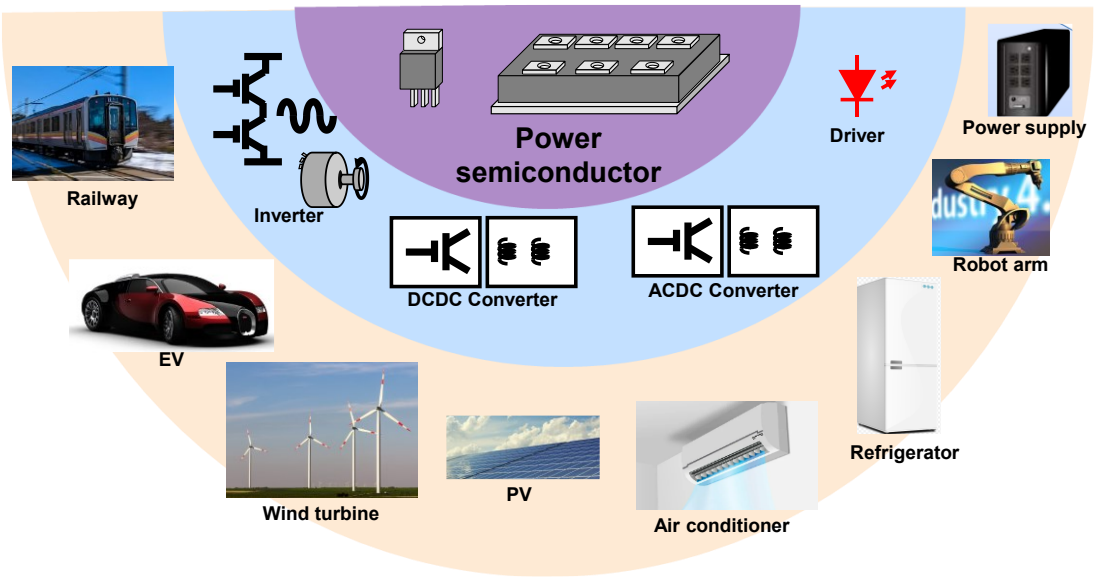


Figure 1.1: Power semiconductors and power converters used in various applications in society.

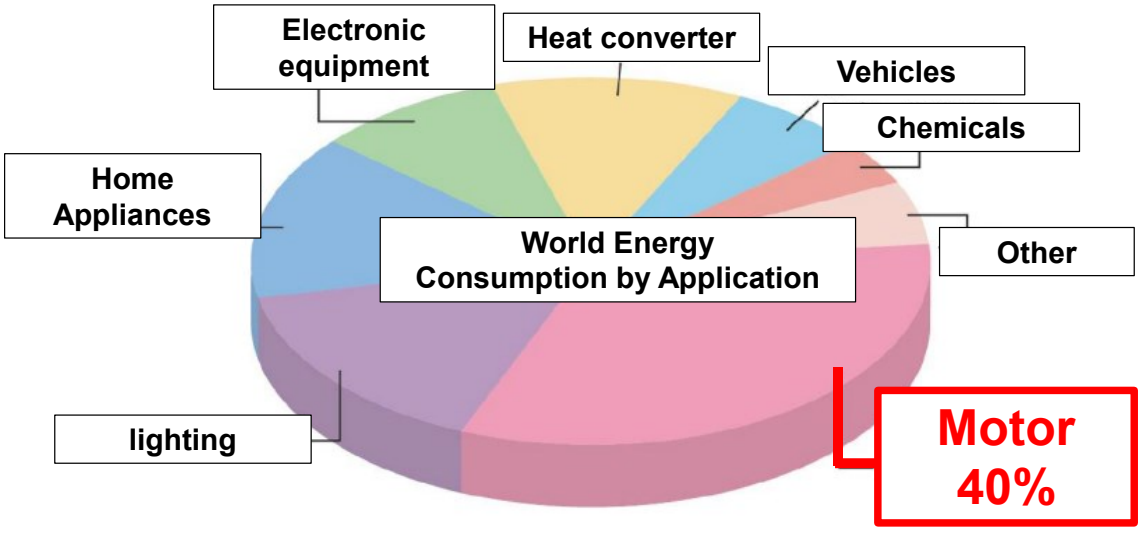


Figure 1.2: Global power consumption by application.

Figure 1.3 shows the technology s curve for power electronics and the technologies that have broken the limits of the curve [4]. In the past, power electronics has improved converter performance with the introduction of new devices such as IGBTs [5] and Superjunction MOSFETs (SJMOS) [6] and new modulation methods such as vector control [7]. Even today, various efforts are being made to improve converter performance.

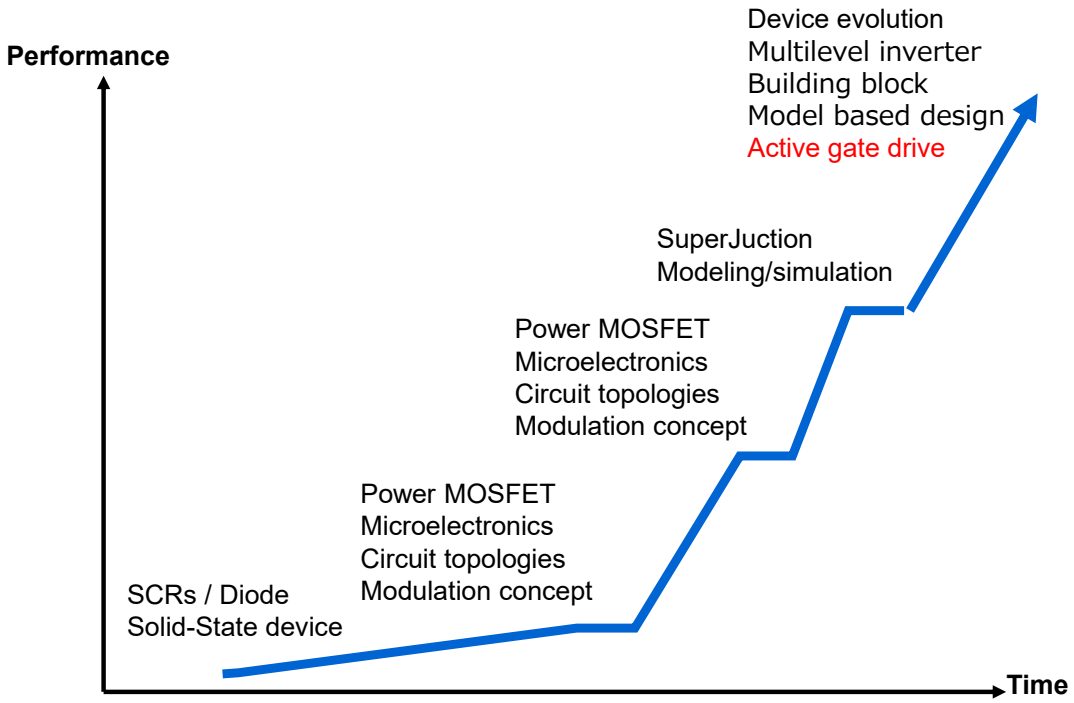


Figure 1.3: The technology s curve for power electronics and the technologies that have broken the limits of the curve.

Figure 1.4 shows each technology. Device evolution is one of the most important aspects of power electronics. Wide bandgap devices such as SiC-MOSFETs and GaN, which have lower on-resistance and faster switching than conventional silicon and IGBT, have been commercialized in recent years, contributing to improved converter performance [8] [9]. Multilevel inverters have an output closer to a sinusoidal waveform than conventional two-level inverters, contributing to smaller filters and reducing losses and noise by lowering the switching voltage of the device [10] [11] [12]. Also, derived from this technology, power electronics building blocks are a technique to realize arbitrary converters with short turnaround time (TAT) by combining the number of converter units in series or parallel [13] [14] [15]. Model-based design is a method of conducting co-design and virtual testing from system design to actual manufacturing and system evaluation of converters by utilizing multi-domain simulation technology. And it is a method of reducing man-hours required to ensure increasingly complex specifications, advanced safety, and reliability of converters, and improving the performance of

the system including the converters [16].

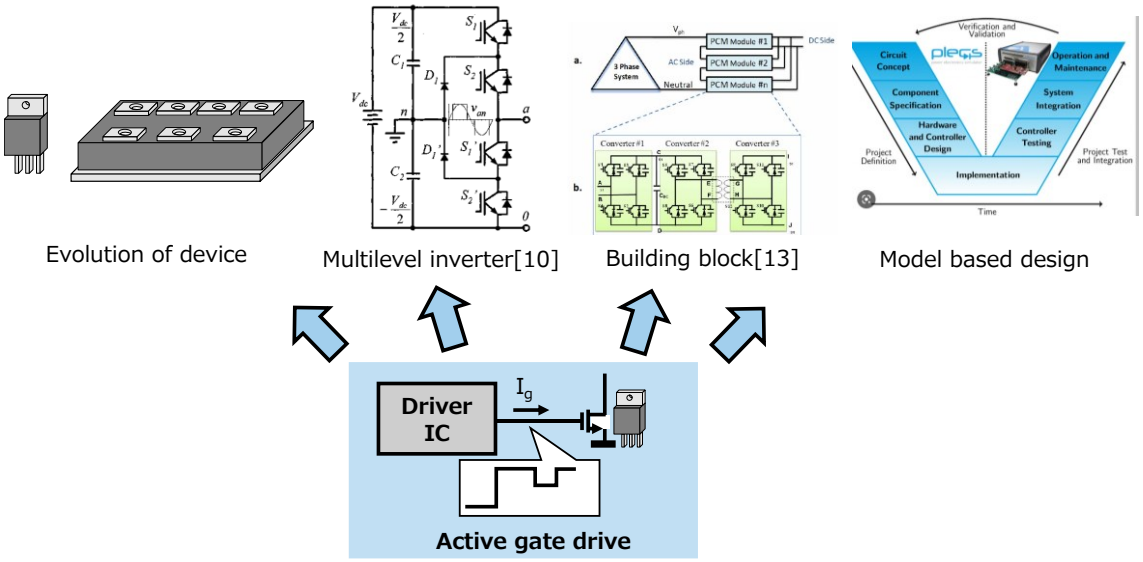


Figure 1.4: Technologies for the advancement of power electronics.

Figure 1.5 shows active gate technique, which we focus on as a technology to improve converter performance [17]. Active gate technique brings the characteristics of power devices closer to those of ideal switches by modifying the signals input to the gate that control the on/off switching of the power devices. This technology contributes to downsizing and higher efficiency of converters by reducing losses and controlling switching waveforms to reduce noise. When driving power devices, drive current is conventionally controlled by resistance. Smaller resistances allow power devices to be switched at higher speeds, thereby reducing losses. However, the transition speed between current and voltage becomes faster, and ringing occurs in the waveform, generating noise. Noise can cause peripheral devices and one's own devices to malfunction. On the other hand, if the resistance value is increased to reduce noise, the waveform transition speed decreases and ringing does not occur, but the loss increases. In other words, there is a tradeoff between loss and noise. Active gate technique solves the above trade-off and was proposed in 2005 [17]. By optimizing the waveform of the gate current supplied to the power device to match the characteristics of the power device, switching is performed with high switching speed, no ringing, and low loss. Active gate technology can extend the performance evolution of power devices as stand-alone switches, and at the same

time, it can contribute to the reduction of components such as filters by reducing noise. It is an important technology that affects everything from the device level to the system architecture level, centered on the driving circuits.

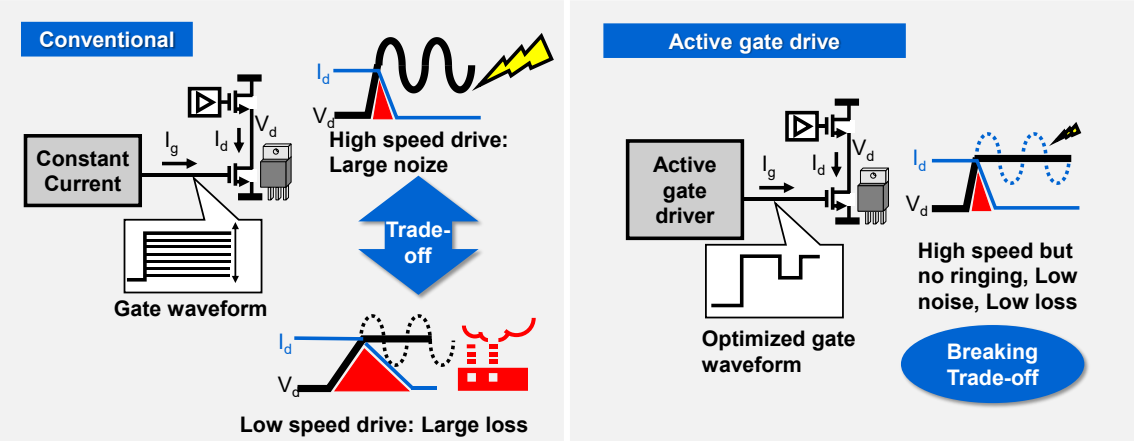


Figure 1.5: Active gate drive technique.

1.2 Power devices and active gate drive technology

Figure 1.6 shows the relationship between types of power devices, converter power, switching frequency, and applications. The most appropriate power device is used according to the speed and power required for the converter. For applications such as power transmission and distribution or railroad motors that require high power and high switching speed, Insulated Gate Bipolar Transistors (IGBT) and Gate Turn-Off thyristors (GTO) are used because they can achieve low conduction losses. On the other hand, power devices used in AC adapters and lighting fixtures use GaN, which offers low power and high switching speeds. Si-MOSFETs and Superjunction MOSFETs (SJMOS) are used in compressor converters for home appliances because they have low power requirements, can be operated without increasing the switching speed, and are low cost. In recent years, Silicon Carbide MOSFETs (SiC-MOSFETs) have been used in automotive applications, such as e-mobility, to achieve high-speed and low-loss switching, resulting in high-performance converters.

Active gate technique is applicable to all hard-switching converters. On the other hand, different power devices and end-uses require different specifications for active gate drive

circuits. In this paper, we focus on two of the above four areas, the low-power, low-switching area and the high-power, high-speed switching area, to develop active gate technology. In the high-speed, high-power region, advanced active gate technology is required. On the other hand, low-speed, low-power regions require low-cost active gate technology with simple technology. This thesis section will research and develop these two distinctive areas.

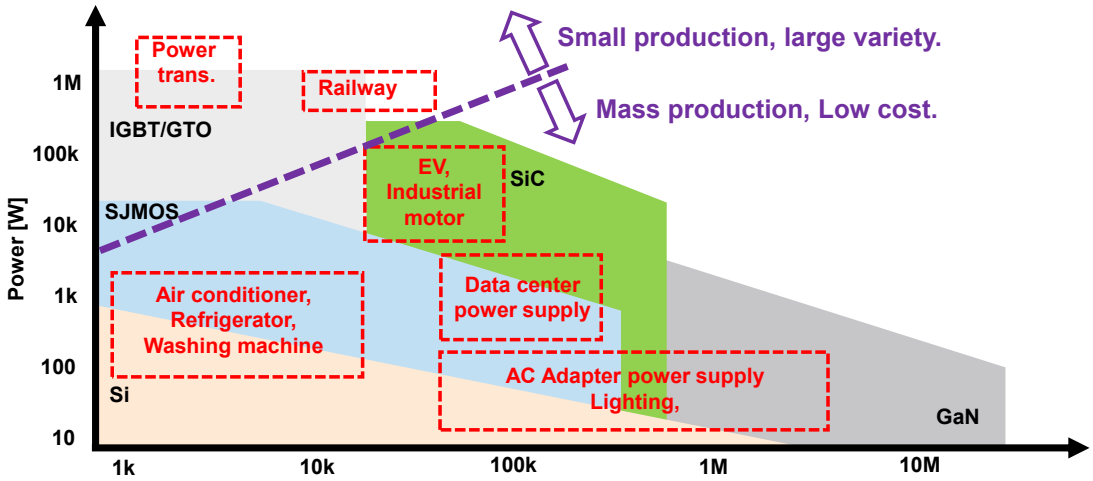


Figure 1.6: The relationship between types of power devices, converter power, switching frequency, and applications.

1.3 Structure of this paper

The structure of this thesis is shown in Figure 1.7. This thesis is organized as follows.

Chapter 2 describes the characteristics of power devices and the fundamentals for developing active gate technology, including device switching characteristics and an overview of active gate technology. The relationship between device characteristics and the applications used is clarified. The switching characteristics of power devices are presented. The impact of each waveform on the performance to the converter, e.g., loss and noise are shown. In addition, existing research on active gate technique are reviewed to identify target devices for which active gate technique will be applied and the applications.

Chapter 3 describes a slew-rate (SR) control technique for SJMOS using analog feedback technology, focusing on the recovery current, which is a phenomenon unique to SJMOS, and controlling the peak recovery current to keep the turn-on drain voltage transition rate constant.

In Chapter 4, we describe a ringing suppression technique for next-generation SiC devices using digital feed-forward technology to break the trade-off between loss and drain voltage transition speed. Theoretical analysis, simulation, and measurements are used to comprehensively demonstrate the waveforms that reduce ringing. Chapter 5 provides a summary of this study and future work.

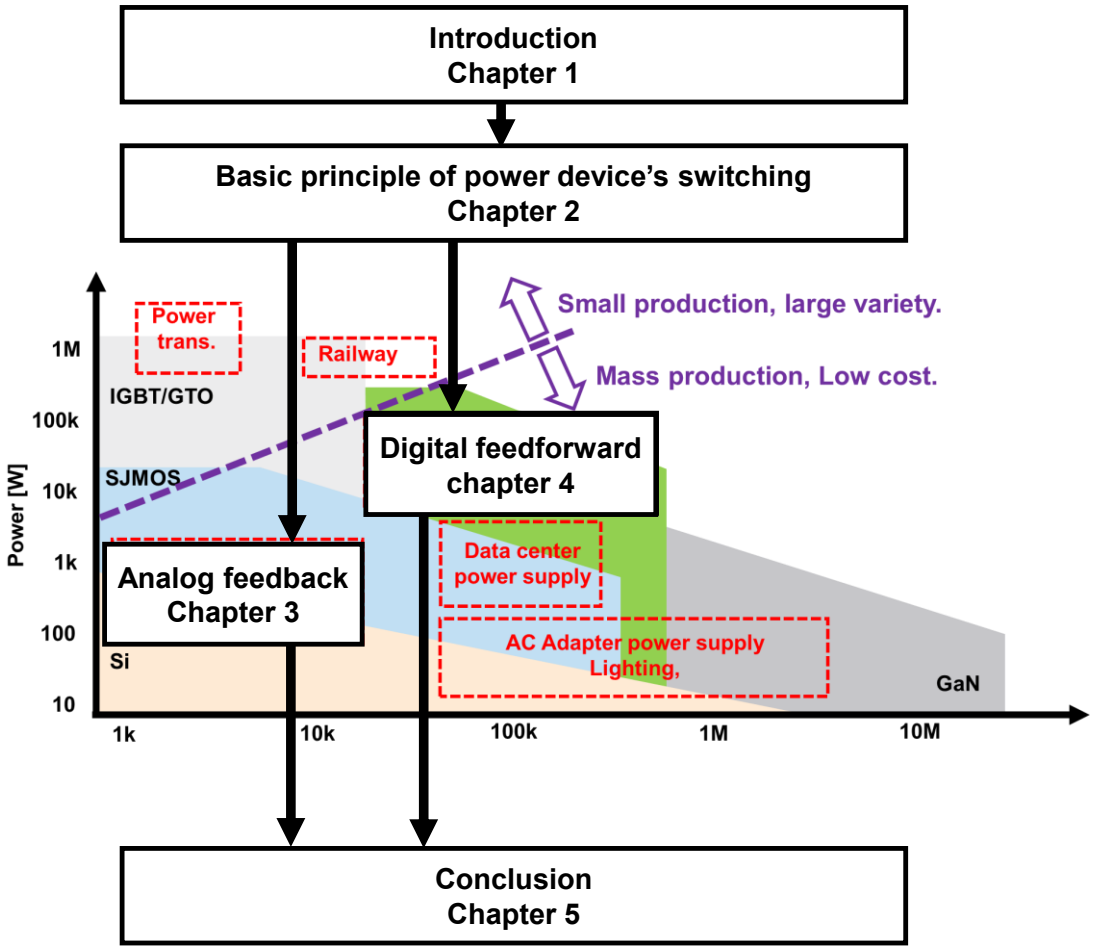


Figure 1.7: Structure of this thesis.

Chapter 2 Overview of power device and active gate drive technology

2.1 Overview of this chapter

This chapter provides an overview of power device switching principles and active gate technology. First, characteristics of power devices are described as basic knowledge to explain switching principles. Specifically, characteristics of SJMOS, IGBT, and SiC-MOSFETs are described. Next, the switching principles of power devices are described. Furthermore, we describe how the switching waveforms of the power devices represent the influence on the noise of the converter system. This is followed by a technical classification of active gate technologies.

2.2 Power device characteristics.

In this section, the characteristics of each power device are described. silicon, SJMOS, IGBT, and Silicon Carbide (SiC) are described in this order.

2.2.1 Si-MOSFET

Figure 2.1 shows the cross-sectional structure of a silicon power MOSFET. A power MOSFET consists of small cells arranged in a row, covering a silicon wafer. Current flows vertically from top to bottom. Metal gate and source electrodes are formed on the top surface of the wafer shown in Figure 2.1, and metal drain electrodes are formed on the bottom surface of the wafer. When the device is turned off, a depletion layer appears as shown in Figure 2.2(a). When the device is turned on, a channel is formed, and current flows as shown in Figure 2.22(b). In devices with large breakdown voltage, the resistance is mainly determined by the n- diffusion layer. There is also a parasitic diode at the position shown in Figure 2.2(c). This parasitic diode conducts when the drain-source voltage is negative. This diode allows the power MOSFET to conduct current in both positive and negative directions. However, this diode is not optimally

designed to have a small recovery current, so a large recovery current may occur.

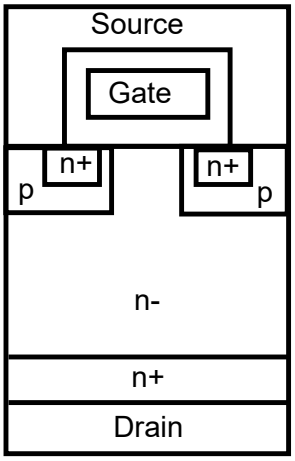


Figure 2.1: Cross-sectional structure of a silicon power MOSFET.

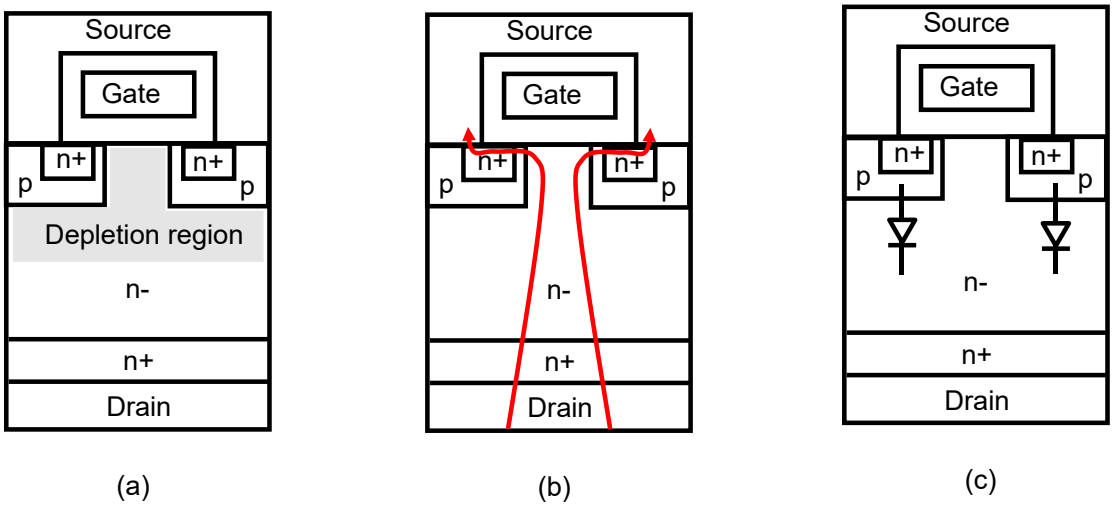


Figure 2.2. Cross-sectional structure of a silicon power MOSFET. (a) Turn-off, (b)Turn-on, (b) Parasitic diode.

2.2.2 SJMOS

SJMOS were proposed to reduce on-resistance while maintaining the breakdown voltage of power MOSFETs [18] [19]. Figure 2.3(a) shows a cross-sectional view of standard power MOSFET and Figure 2.3(b) shows a cross-sectional view of SJMOS. The electric field of power MOSFET and SJMOS are also shown in Figure 2.3. The super junction MOSFET consists of a p-layer formed in columnar strips on a portion of the n-layer, with the p-layer and n-layer

arranged alternately. Conventional power MOSFETs have a depletion layer that extends vertically as shown in Figure 2.3. The depletion layer thickness determines the electric field strength, and the depletion layer thickness is roughly inversely proportional to the drift layer concentration. On the other hand, the on-resistance of the drift layer is also inversely proportional to the concentration, so if the field strength is increased, the breakdown voltage cannot be maintained. In a super junction MOSFET, as shown in Figure 2.3(b), the drift layer consists of alternating P and N layers. When voltage is applied, the depletion layers spread horizontally and eventually unite to form a depletion layer equivalent to the groove depth. Since a depletion layer equivalent to the groove depth can be obtained with only half the groove spacing depletion layer spread, low ON-resistance is achieved. On the other hand, there is a problem of large recovery charge due to the increased area of parasitic diodes. The area where the p-layer and n-layer are in contact is increased, resulting in a large recovery current.

Due to their low ON-resistance, SJMOS are often used in low-power and low-speed motors for home appliances, etc. The voltage transition rate in the above application is about 5 V/nsec.

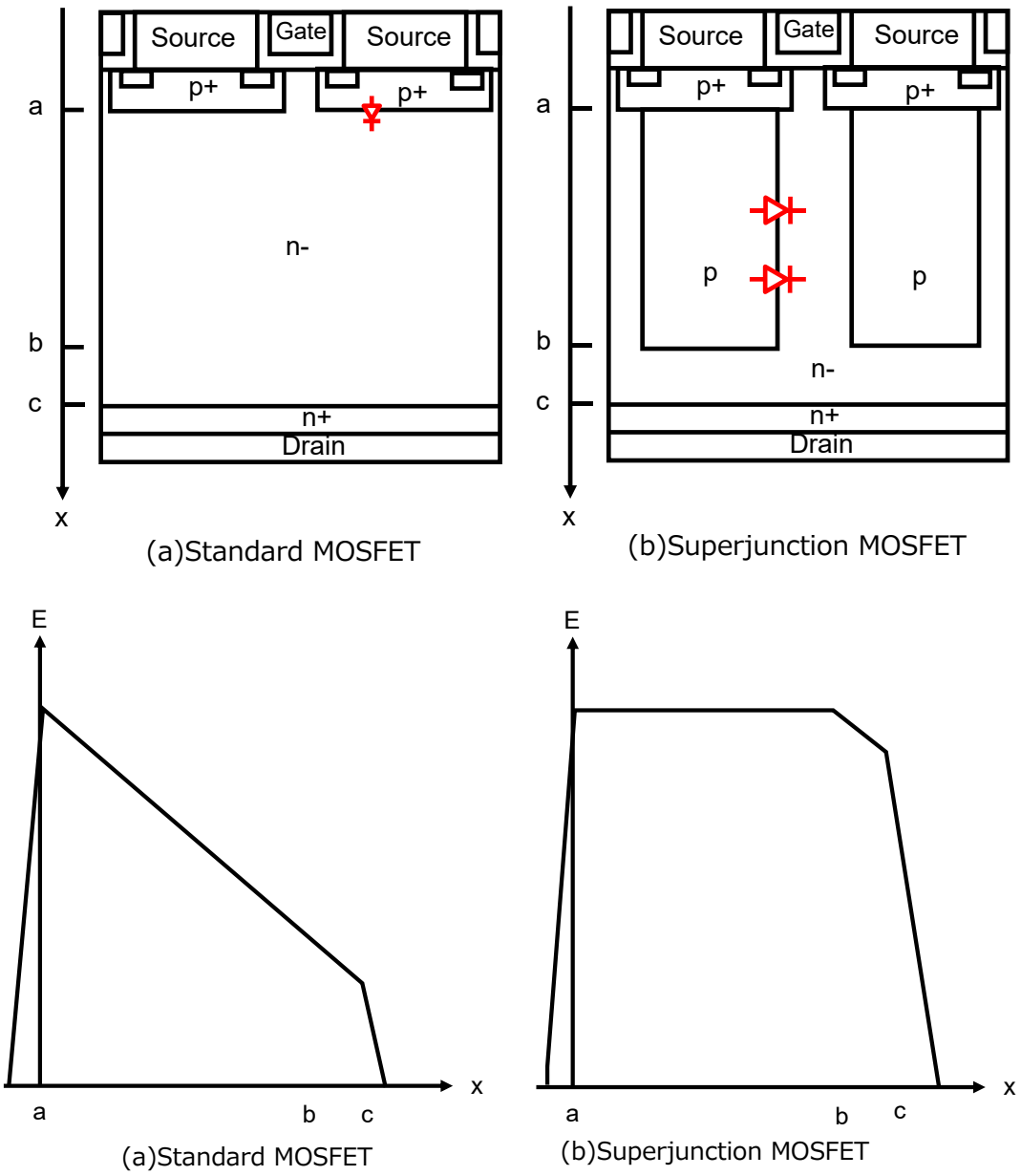


Figure 2.3: Cross-sectional structure and electric field of a silicon power MOSFET and Superjunction MOSFET(SJMOS).

2.2.3 IGBT

Figure 2.4 shows a cross-sectional view of an IGBT. As shown in Figure 2.4, the cross-sectional view of an IGBT is similar to that of a power MOSFET, the difference being that the P layer is connected to the collector. The role of the added P layer is to inject a minority

charge into the N layer when the IGBT is conducting. When the P and N layers are forward biased during conduction and the minority charge is injected into the N layer, conductivity modulation occurs [20]. This reduces the resistance of the N layer, resulting in an IGBT with high breakdown voltage and low resistance. On the other hand, because a P layer is added to the collector, the IGBT has a forward PN junction between the collector and emitter. This causes a certain amount of loss even when the collector current is small. IGBTs are not suitable for high-speed operation and cause extra switching losses. IGBTs are often used in low-speed, high-power converters for electric railways and industrial applications because of their high current capability and lower on-resistance than SJMOS. The voltage transition speed is approximately 5 V/nsec.

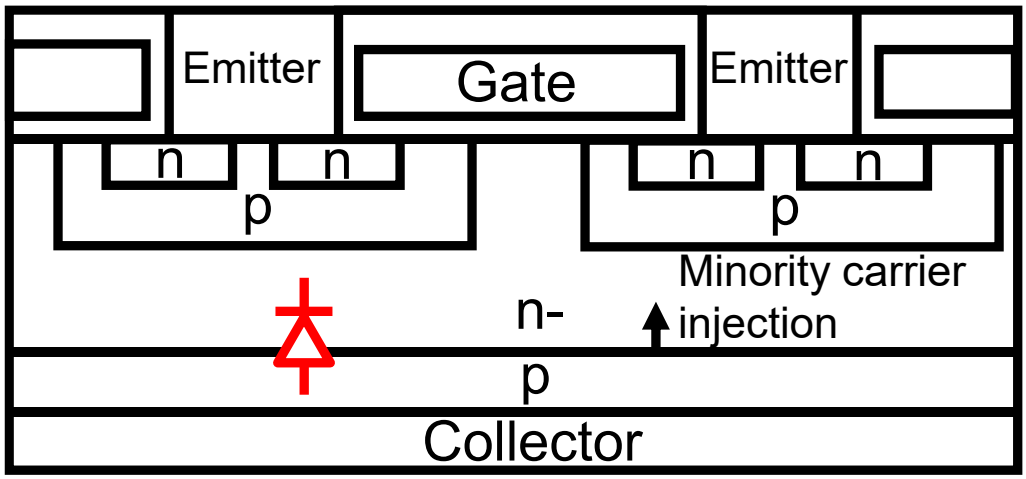


Figure 2.4: Cross-sectional structure of IGBT.

2.2.4 SiC-MOSFETs

SiC with a wide band gap enables MOSFETs with higher breakdown voltage, lower on-resistance, and faster switching than power MOSFETs. SiC-MOSFETs offers low ON-resistance in a small area in the high voltage range of 600V or higher. It also enables high switching due to reduced parasitic capacitance. The device structure is similar to the power MOSFET shown in Figure 2.1. Comparing SiC and Si with respect to electron mobility only, Si has a higher mobility than SiC. On the other hand, SiC has a large critical electric field and can

achieve low on-resistance at voltages above 600V [21]. In addition, SiC has small characteristic fluctuation with temperature and can be operated up to 300°C. Temperature characteristics restrictions of package technology typically limit SiC-MOSFETs operating temperatures to 175°C. Similar to power MOSFETs, SiC-MOSFETs also have parasitic diodes, but parasitic diodes of SiC-MOSFETs have a large forward voltage of 3 to 4 V, and another diode is connected in parallel. SiC-MOSFETs can switch faster than IGBT and requires smaller inductors, etc., so SiC-MOSFETs has been replacing IGBT in applications with 600 V or more and higher power. SiC-MOSFETs are smaller in area and have smaller parasitic capacitance than other devices, so the voltage switching speed exceeds 10 V/nsec.

2.2.5 Summary of each device's features

The characteristics of each device are summarized in Table 2.1. Power-MOSFETs are used in low-voltage inverters and converters; SJMOS have higher losses due to recovery current, but can achieve lower ON-resistance in the high-voltage range than Power MOSFETs and are used in high-voltage, low-power applications; IGBTs have losses due to saturation voltage and are not suitable for low-voltage, low-power applications. IGBTs are not suitable for low-power applications due to saturation voltage losses, but are used in high-voltage, high-power applications. SiC-MOSFETs are replacing IGBTs in high-voltage, high-power applications.

Table 2.1: Summary of each power device's characteristics.

	Breakdown voltage	Pros	Cons	Main application
Power MOSFET	<400V	Low on-resistance at low voltage.	High on-resistance at high voltage	Used in low-voltage inverters and converters.
SJMOS	>500V	Lower on-resistance than power MOSFET.	Large loss due to reverse recovery charge	Used for high-voltage, low-power household compressors.
IGBT	>500V	Lower on-resistance than silicon device.	Large loss compared to SJMOS at low current due to saturation voltage. Large turn-off loss.	Widely used in high voltage and high power regions. Not suitable for low-power areas due to saturation voltage.
SiC-MOSFET	>1.2kV	Lower on-resistance than silicon and IGBT at high voltage. Low input capacitance allows high-speed operation.	Characteristics such as threshold voltage change significantly when electrical load is applied. Sensitive to short-circuit.	IGBTs are being replaced by SiC-MOSFET in the high-voltage, high-power region.

2.3 Switching waveforms of power devices and the effect of each waveform on noise

In this section, we describe what waveforms are generated when a power device switches. Next, the current-voltage waveforms of turn-on and turn-off are classified, and how the waveforms in each section affect the noise is described. Figure 2.5 shows the power device and drive circuit used in an inverter. This section describes the turn-off and turn-on operation of low-side power devices. Since the high-side power devices are turned off, only the diodes are considered. The low-side drive circuit is modeled with a current source. The load inductor acts as a current source.

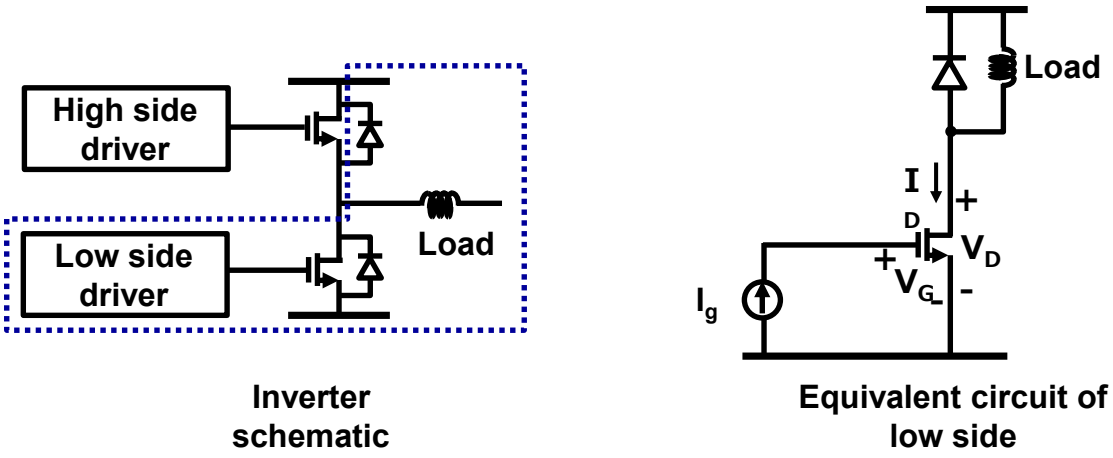


Figure 2.5: The power device and drive circuit of the inverter and its equivalent circuit

2.3.1 Turn-on waveform

Figure 2.6 shows the waveforms at turn-on. At the end of section a, gate current begins to flow. The gate voltage increases in section b. At the end of section b, the gate voltage reaches the threshold voltage of the power device. Then drain current begins to flow. In section c, the drain current increases. At this point, the drain voltage is equal to the supply voltage. This is because the diode is turned on and the drain voltage and supply voltage are connected in a low impedance state. As the drain current increases, the current flowing through the diode decreases. At the end of section c, when the drain current becomes equal to the current charged to the load, the current flowing through the diode becomes zero and the diode turns off. The drain voltage then drops in section d. As the drain voltage drops, the parasitic drain-to-gate capacitance of the power device increases due to the Miller effect, and the gate voltage remains unchanged. At the end of section d, when the drain voltage reaches the ground voltage, the Miller effect disappears and the gate voltage rises again. When the gate voltage reaches the power supply voltage of the driver side, the turn-on operation is completed.

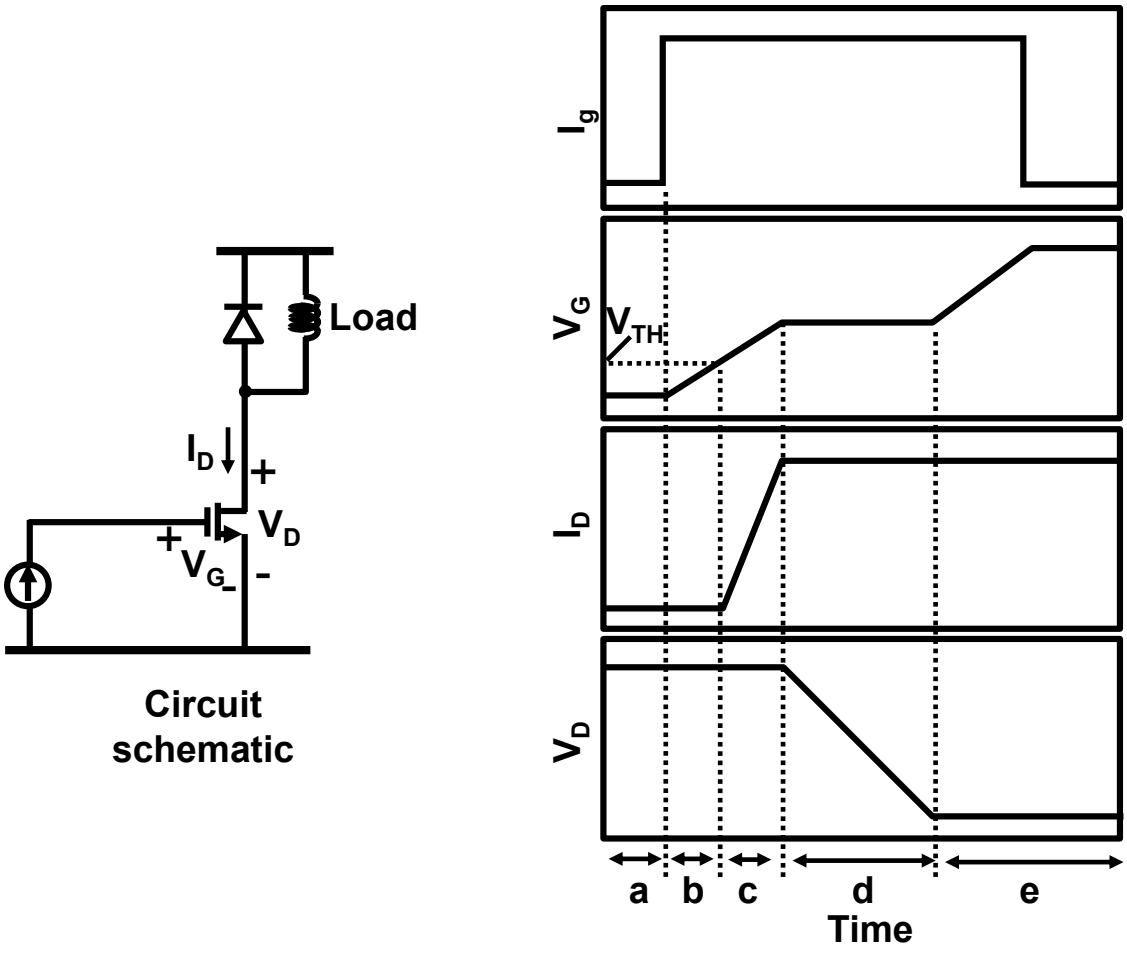


Figure 2.6: Waveforms at turn-on.

2.3.2 Turn-off waveform

Figure 2.7 shows the turn-off waveform. At the end of section a, the gate voltage flows in the direction of charge draw from the gate. The gate voltage begins to decrease. In section b, the power device is operating in the linear region, and the drain voltage increases slowly as the gate voltage decreases. At the end of section b, the power device transitions from the linear region to the saturation region, and the drain voltage rises at a faster rate in section c. Then, in section c, the gate voltage does not change due to the Miller effect. At the end of interval c, when the drain voltage becomes larger than the threshold voltage of the diode, the diode turns on and the drain current decreases. When the gate voltage becomes less than the threshold voltage at the end of section d, the drain current becomes zero. When the gate voltage reaches 0, the turn-off

operation ends.

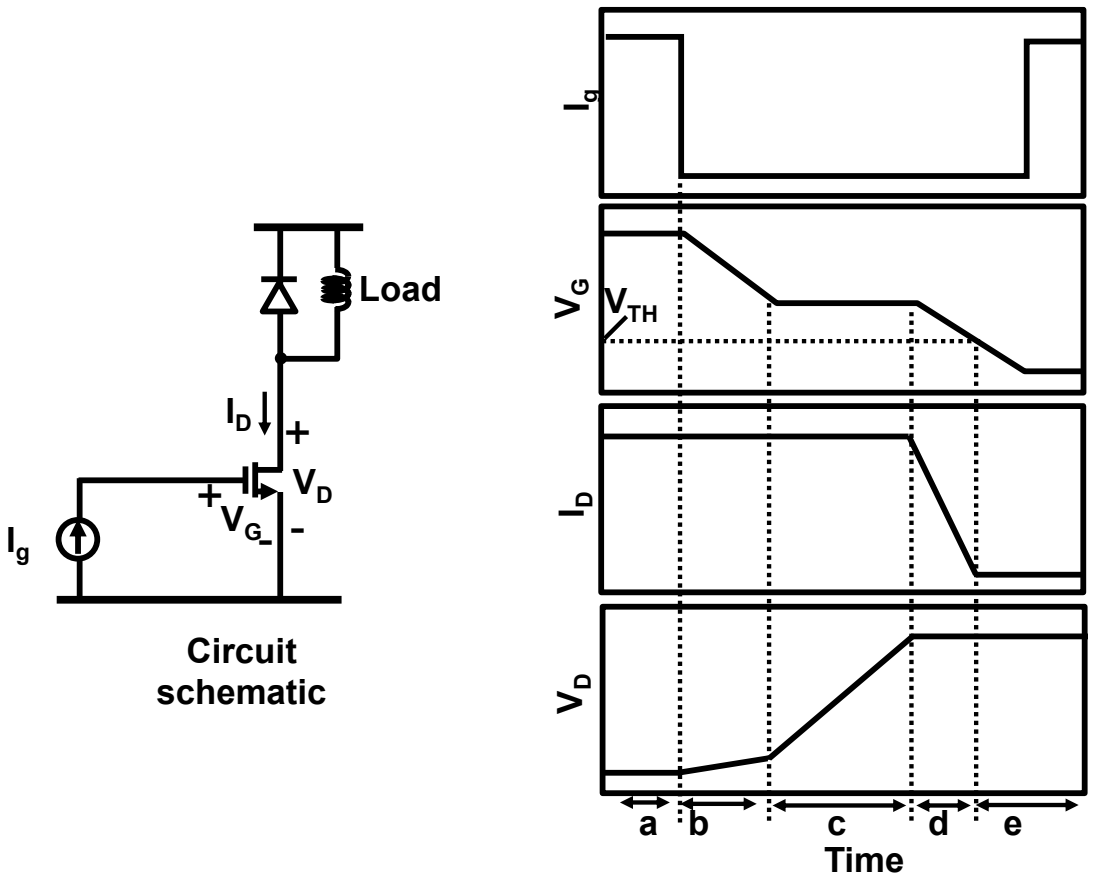


Figure 2.7: Waveforms at turn-off.

2.3.3 Effect of switching waveform on noise spectrum

This section shows how the waveforms of the power devices identified in Section 2.3.2 affect the noise. Figure 2.8(a) shows the switching waveform of a power device. The turn-off waveform is shown as an example. Figure 2.8(b) shows an example of the noise spectrum. There are various types of noise in converters, such as radiation noise mainly caused by current and conduction noise caused by voltage.

In the switching waveform of a power device, there are three components that affect noise: A. Slew Rate (SR) of current voltage, B. Surge or ringing of current voltage, and C. Noise due to harmonic components in the waveform. Figure 2.8 shows how each component affects the noise spectrum. Assuming that the slew rate of the switching waveform of the power device is a first-order function of time, the current-voltage SR affects the frequency at which the slope of

the noise spectrum changes from -20 dB/dec to -40 dB/dec. The slower the transition rate, the lower the noise level at higher frequencies [22]. Ringing present in the current-voltage waveform shows up as a peak in the noise spectrum. As the ringing voltage or current peak decreases, the level in the noise spectrum shown in Figure 2.8(b), B, also decreases. Examples of noise due to harmonic components in the waveform can be found in reference [23]. Due to the nonlinearity of the parasitic capacitance of the power device, a steep current is generated, amplified by the resonant circuit of the power stage, and appears as a peak in the noise spectrum [23].

The characteristics of A, B, and C shown in Figure 2.8(b) all depend on the magnitude of the gate current of the power device. If the gate current is small, the inflection point on the spectrum moves to lower frequencies, reducing noise at high frequencies, as well as the peak value of current-voltage ringing and the peak value derived from harmonic components. Since a reduction in drive power leads to an increase in switching losses, there is a trade-off between noise spectrum and losses.

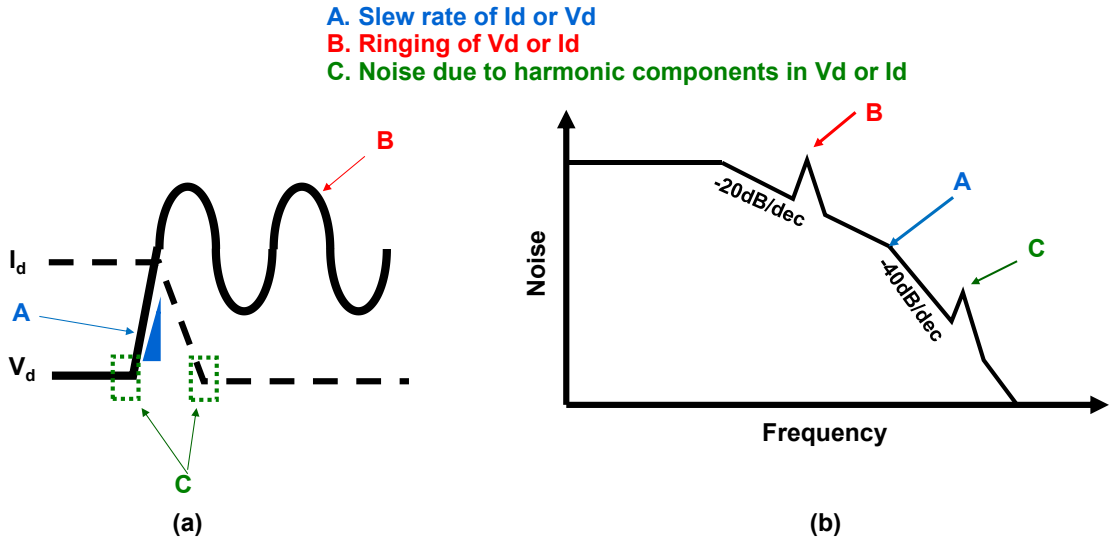


Figure 2.8: (a)The switching waveform of a power device and (b) noise spectrum.

2.3.4 Comparison of turn-on and turn-off loss

This subsection compares the turn-on and turn-off losses of SiC-MOSFETs and SJMOS, which is the focus of this paper. Figure 2.9 shows the turn-off and turn-on losses of SJMOS and

SiC-MOSFETs. Figure 2.9(a) shows the turn-on and turn-off losses of the SJMOS. The device model number is TK8A60W5, and the measured turn-on and turn-off losses are shown under the conditions of 3 V/nsec absolute slew rate and 1 A drain current of the load. As shown in the Figure 2.9(a), the value of turn-on loss is 35uJ, while the value of turn-off loss is 3.5uJ. Since the turn-on loss is 10 times larger than the turn-off loss, it is important to reduce the turn-on loss in SJMOS. Figure 2.9(b) shows the measured turn-on and turn-off losses of a SiC-MOSFET. The device model number is SCT3080KR, and the measurement results were obtained under the condition of 11V/nsec absolute slew rate. The turn-on loss was measured at a drain current of 12A and the turn-off loss was measured at a drain current of 15A. The turn-on loss is 0.16mJ and the turn-off loss is 0.115mJ. Although the drain current values are under different conditions, the turn-on and turn-off losses are of similar values. In SiC-MOSFETs, it is important to reduce both turn-on and turn-off losses.

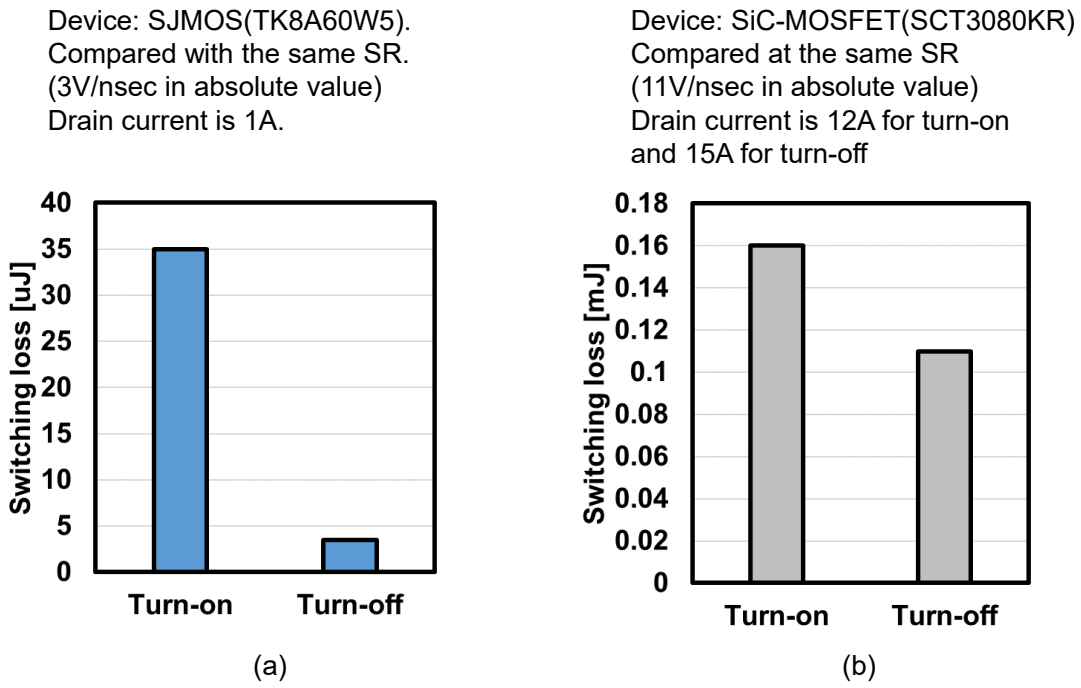


Figure 2.9: Comparison of turn-on and turn-off loss.

2.4 Current-voltage waveform of the converter and the load adaptive operation.

This section describes the current-voltage waveforms of converters in which power devices are used and the load adaptive functions. Figure 2.10 shows an example of an AC-DC converter used in a Power Factor Correction circuit (PFC). In a PFC, the load current varies from time to time in a sine wave shape. The active gate waveform input to the power device must change according to the current value of the power device. This is because the condition of the power device changes in response to the current in the power device. This function is called load adaptive. How to realize the load adaptive function is one of the key points in the development of active gate technique.

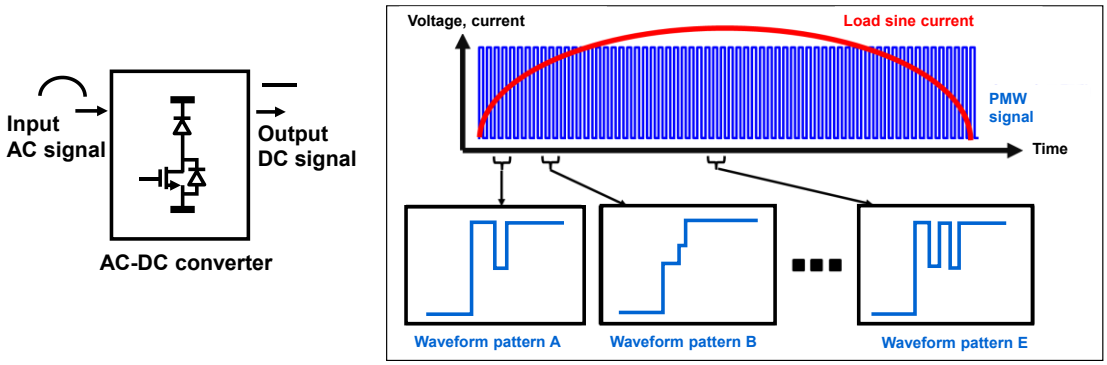


Figure 2.10: Voltage and current waveform of AC-DC converter and load adaptive function of active gate drive.

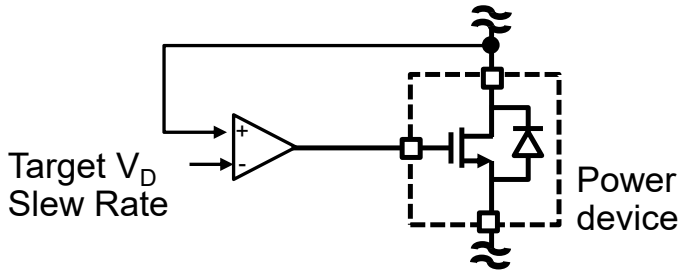
2.5 Active gate driving

This section provides an overview of active gate drive techniques that resolve the tradeoffs presented in the previous section. First, the active gate drive techniques studied to date are classified into analog feedback and digital feedforward techniques, and the characteristics of each technique are described.

2.5.1 Analog feedback active gate drive

Figure 2.11 shows an active gate using analog feedback technique. The current or voltage of

the power device is detected and compared with a reference voltage by an operational amplifier (OP-AMP) to control the gate voltage or current of the power device. The advantage of this method is that robust control is possible regardless of variations in power devices and ICs. Since the drain voltage or current waveform is detected and instantaneously fed back to the gate, it has the load adaptive function described in Section 2.4. Furthermore, if the bandwidth of the feedback loop is wide enough, the waveform can be kept constant even if the operation of the power device is not fully understood. On the other hand, the disadvantage is that the waveform is less flexible, and each circuit must be prepared independently for the noise issues presented in Section 2.3.3. Also, as the slew rate transition speed becomes faster, the OP-AMP bandwidth needs to be wider.



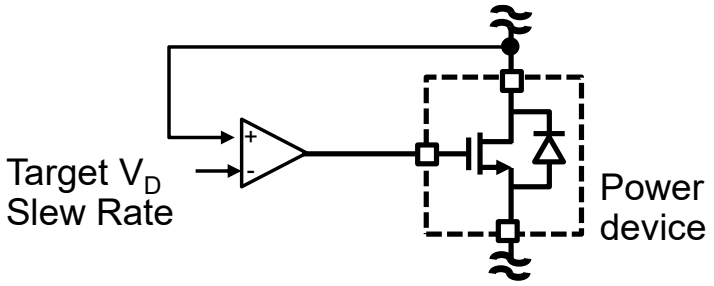
☺Merit
Robust control with feedback
Control independent of power device variations
Highly accurate models of power devices are unnecessary
☹Demerit
Less degree of drive waveform optimization
High BW OP-AMP is necessary

Figure 2.11: Active gate drive using analog feedback technique.

2.5.2 Digital feedforward active gate drive

Figure 2.12 shows an active gate technique using digital feed-forward technology. Digital data is sent out to an arbitrary waveform output circuit in response to the edge of a PWM signal, which is a gate control signal. The waveform output circuit outputs the gate waveform. Fine control of the waveform is possible, and the noise issues described in Section 2.3.3 can be addressed with a single circuit. On the other hand, the output waveform must be generated in a certain method. In addition, the output waveform must be changed according to the variations of

power devices and waveform output circuits. In addition, it is necessary to output waveforms that follow the load of the power device. When load adaptive function is performed, the digital waveforms need to be stored in memory.



☺Merit
Robust control with feedback
Control independent of power device variations
Highly accurate models of power devices are unnecessary
☹Demerit
Less degree of drive waveform optimization
High BW OP-AMP is necessary

Figure 2.12: Active gate drive using digital feedforward technique.

2.5.3 Issues and technology to be developed in this paper

- **IC Integration**

Chip integration is essential for the application of active gates to consumer electronics and automotive products, which are expected to be mass-produced. However, there are challenges to integration with respect to existing technologies.

In the literature using analog feedback technology [24] [25], a 300 MHz wideband operational amplifier is required to control the low-speed SR of 2 V/nsec for IGBTs. For SiC-MOSFETs, there is also a study to balance the current imbalance of parallel drive, which can be applied to slew rate control, but requires a wideband OP-AMP with a bandwidth of 320MHz [26] [27]. Based on the concept in the literature [28], an example of a 300-MHz OP-AMP integrated on a chip with active gate control has been reported [29], using GaN as the target power device. However, the required gate voltage for GaN is 5 V, which is not compatible with the 10 V to 20 V voltages required by other devices such as SiC-MOSFETs and SJMOS.

ICs that can arbitrarily control the drive waveform of power devices have been reported in products [30] [31] [32] [33] [34] [35] [36] [37] [38] and papers [39]. In product [30] [31] and literature [40], the gate current control is shown and the switching of the power device is not described. Also, in products [32] [34] [35] [36], the assumed device voltage are below 100V, which is low. Products [37] [38] and literature [41] only make the driver section variable, and a separate waveform memory for load adaptive is required.

An example of integration of a driver stage to drive a power device and a memory circuit has been reported [42]. In the literature [42] [43], only one waveform memory is provided, and it is not possible to control following the load of the power device. Even in the example using an external FPGA, it cannot be applied to follow a load that changes in about 1 msec [44] [45]. There are several examples of load adaptive control [46] [47]. However, in reference [46], the driver IC is controlled using an external measuring device, and the IC alone has not succeeded in load adaptive function. In reference [48], the current and voltage slew rates are sensed by an analog circuit and feedback signals are generated by an FPGA. The waveform is output to the gate of the power device by a mixed analog-digital circuit including an OP-AMP and DAC to achieve 800 V switching. However, the output stage requires a 300 MHz op-amp, which is difficult to integrate in the chip. In the literature [49], feedback control is performed by analog voltage/current threshold detection and digital time measurement, and many ideas are incorporated, such as using PI control and LUT, but the control part is a digital configuration using FPGA and has not been integrated. Reference [47] uses a driver that can generate positive and negative binary gate currents, and the optimal waveform is generated by feedback with an ADC. However, the switching voltage of the power device is as low as 48 V. The digital feedback method for IGBTs has a maximum SR of 0.0004 V /nsec, about three orders of magnitude lower than the speed normally used [50]. In the product [33], the emitter current is detected and the gate resistor is switched, but a separate current-sense pin must be provided on the power device side, and the trade-off between loss and noise has not been successfully overcome. The work [51] based on the concept of [52], has succeeded in reducing current ringing during turn-on by integrating a gate drive circuit with variable output current, a sensor circuit to determine appropriate timing, and a control circuit to change the current waveform, all

on a single chip. However, this was demonstrated with IGBTs, and the optimal gate waveform could not be output due to malfunction of the sensor circuit caused by noise during turn-on. In addition, this technology is not applicable to turn-off. Other active gate technologies that have been proposed include driving with a boost converter [53], detailed analysis of the relationship between switching losses and current [54], load current estimation from gate waveforms [55], and waveform generation by directly observing noise [56]. However, there are no examples of integrated chips and load adaptive function at high voltages of 100 V or higher. The main issues are that load detection is difficult due to the effects of noise from power device switching and the need to switch memories that store complex waveforms.

- **Analysis that takes into account nonlinearities.**

In analog feedback technique, even if some difference in power device operation exists between simulation and actual measurement, the current and voltage of the power device can be controlled as long as the power device is operating within the feedback bandwidth. On the other hand, in digital feedforward technique, theoretical support for active gate waveforms is essential. Studies have been conducted to derive the waveform using optimization algorithms [39] [46] [57]. However, these studies do not explain why the optimal waveform can reduce ringing of drain current and voltage, making it difficult to apply to other devices. Reference [58] also considers the relationship of the drain waveform to noise, but does not logically explain the logic of waveform generation.

Since the capacitance of power devices strongly depends on the drain voltage [59] [60] [61] [62] [63], analysis that takes nonlinearities into account is essential. In the literature [64], the turn-on current is analyzed, but the capacitance nonlinearity is not analyzed. Furthermore, the literature [64] models the power device as a voltage source, which leads to incorrect conclusions. In reference [44], both turn-on and turn-off analyses are performed, but again capacitance nonlinearities are not taken into account. Reference [65] mentions the analysis of SiC-MOSFET turn-off and capacitance nonlinearity, but the verification by simulation is incomplete. As a result, no gate current patterns are shown in the simulations to break the trade-off between surge voltage and losses. In addition, no experiment results are shown to break the trade-off. Even if one tries to generate the optimal waveform for each device variation, it is not realistic, as it

requires 2500 measurements in reference [39] and about 500 seconds in reference [46]. In addition, the generated waveforms would be excessively complex and require excessive memory size. On the other hand, once theoretical analysis is performed, the arbitrary waveform generation capability of digital feedforward technology can be used to apply active gate waveforms in a variety of devices to solve the tradeoff between loss and noise. It is possible to know what waveforms should be input when the threshold voltage and capacitance of power devices vary.

- **Reverse recovery current specific to SJMOS**

Active gate control for revers recovery currents unique to SJMOS has not yet been developed. Reverse recovery current occurs when carriers in the drift layer move when the diode turns off [19] [20]. Modeling the recovery current of a diode is difficult, and differences exist between the SPICE models provided by various vendors and the values in the data sheets. There is no precedent for a studied example of active gate control of a SJMOS due to the difficulty of controlling the recovery current.

- **Active gate drive technique proposed in this paper**

We will discuss how the technology proposed in this paper relates to the challenges presented above.

Figure 2.13, Figure 2.14 and Figure 2.15 show the challenges presented in this subsection and the active gating technology proposed in this paper as a solution. Figure 2.13 shows the relationship between the issue and the analog FB active gate technology proposed Chapter 3. Figure 2.14 and Figure 2.15 show the relationship between the issue and the digital FF active gate technology proposed in Chapter 4. The challenges can be broadly classified into two categories: chip integration and device characteristics. The challenges of chip integration can be categorized into the need for wideband OP-AMP in analog technique and the lack of logical support for complex active gate waveforms in digital technique. The issues of device characteristics can be categorized as follows: for SJMOS, active gate control corresponding to reverse recovery current is necessary, and for both SJMOS and SiC-MOSFETs, control that takes into account the nonlinearity of parasitic capacitance is a common issue.

The discrete-time feedback technique proposed in Chapter 3 enables active gate control that

also accommodates the reverse recovery current unique to SJMOS and does not require a wideband OP-AMP. The digital feedforward technique logically derives the active gate waveforms by analyzing the capacitance nonlinearity. The time resolution extension technique eliminates the need for wideband amplifiers. Furthermore, the backward gate current injection technique enables active gate control to accommodate the capacitance nonlinearity of power devices.

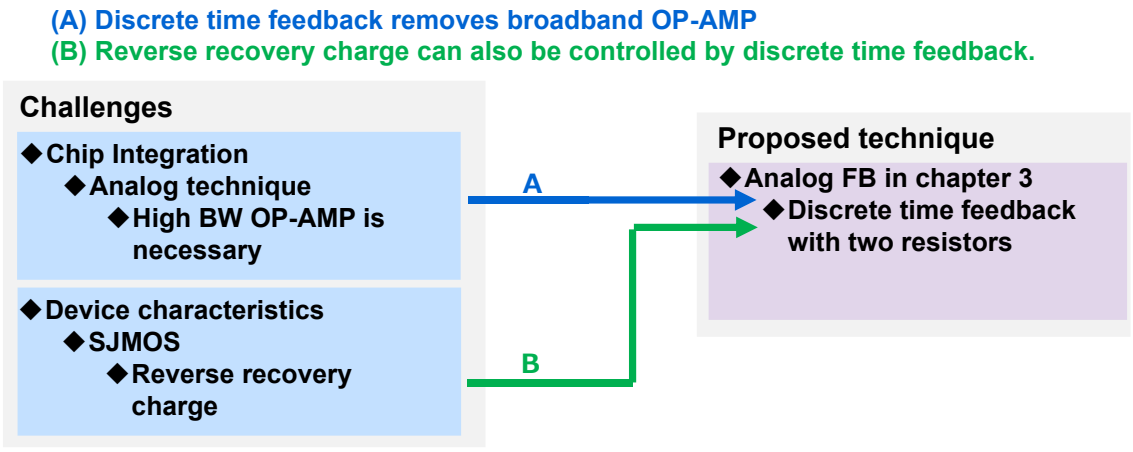


Figure 2.13:The relationship between the issue and the analog FB active gate technology proposed Chapter 3.

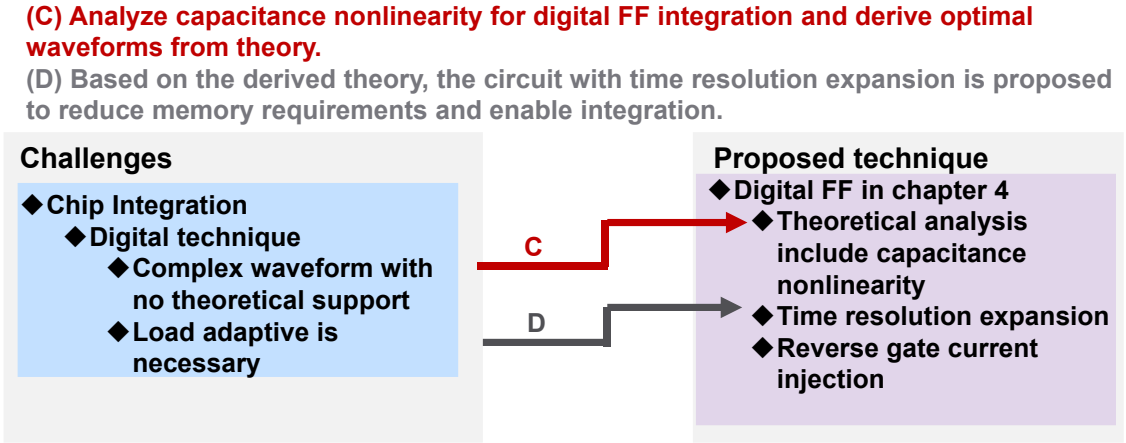


Figure 2.14: The relationship between the issue for chip integration and the digital FF active gate technology proposed in Chapter 4.

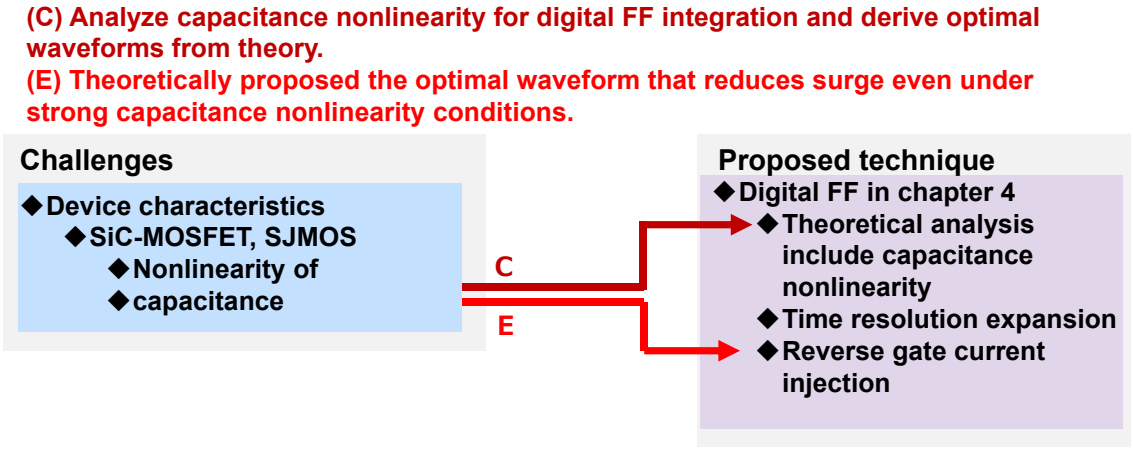


Figure 2.15: The relationship between the issue for device characteristics and the digital FF active gate technology proposed in Chapter 4.

2.6 Summary

In this chapter, the switching principles of power devices and active gate technology were outlined. The characteristics of SJMOS, IGBT, and SiC-MOSFETs were described as basic knowledge to explain the switching principles. In addition, the switching principle of power devices was described. Furthermore, we described how the switching waveforms of power devices represent the influence on the noise of the converter system. Then, the technical classification of active gate technology is described and the current issues are summarized. We then described how the technologies proposed in Chapters 3 and 4 relate to each of these issues.

Chapter 3 Analog feedback active gate drive for Superjunction MOSFET

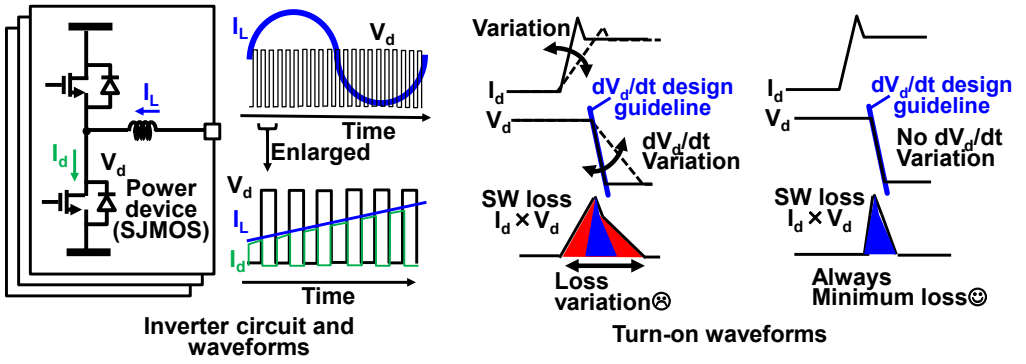
3.1 Introdutcion

This chapter describes an active gate driver IC that uses analog feedback technology. This chapter describes an active gate driver IC that uses analog feedback technology. The target device is SJMOS. The target device is a converter that handles power used in home appliances.

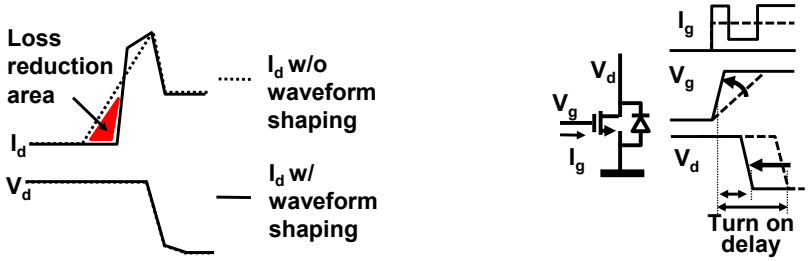
In conventional gate driver design for the converter that handles power used in home appliances, the converter designer selects a fixed value of gate resistance to ensure that the slew rate (SR) of the drain voltage V_d, or dV_d/dt, does not exceed the noise suppression design guidelines for each application or use case. The guidelines or maximum SR is mainly determined from the conduction noise of each application because conducted noise depends on dV_d/dt. Minimizing the gate resistance within the range where dV_d/dt does not exceed the guideline value results in lower switching losses. However, the effect is limited because dV_d/dt becomes uncontrollable because of changes in load current, temperature, and V_{th} of the power transistor. The maximum dV_d/dt must be less than the guideline value in all conditions and there is an extra loss in conditions other than those where dV_d/dt is high. If dV_d/dt can be fixed for all load currents and environments by active gate control, the extra losses can be reduced as shown in Figure 3.1(a). Furthermore, if the drain current rise dI_d/dt can be improved while keeping dV_d/dt constant, losses can be further reduced as shown in Figure 3.1(b). In order to improve the efficiency of the converter, the turn-on delay shown in Figure 3.1(c) must also be reduced.

Superjunction MOSFET (SJMOS) has a low on-resistance among devices with a breakdown voltage of several hundred volts and, unlike IGBTs, does not have a saturation voltage between collector and emitter. For this reason, SJMOS are often used in inverters with several hundred volts and several amperes. In the case of the IGBT, the dV_c/dt can be controlled by the gate current I_{gcnt} during the V_{cd} transition as shown on the left in Figure 3.1(d). However, dV_d/dt of SJMOS is determined by the peak reverse recovery current (I_{RR}) of the diode in the other-side

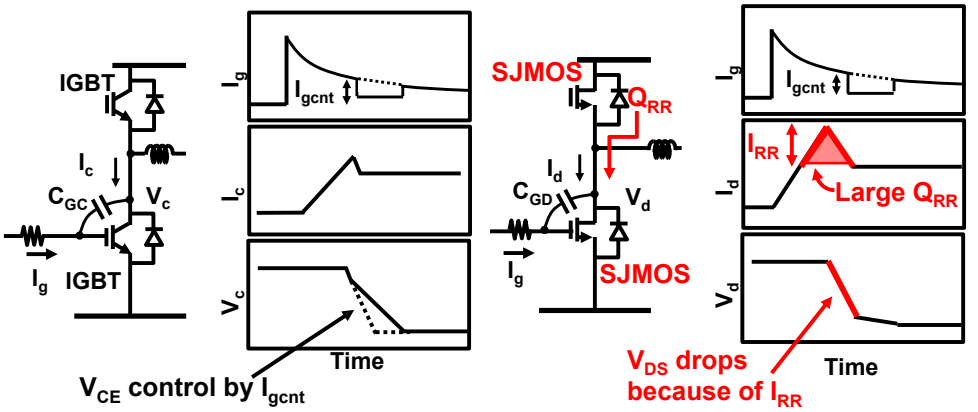
device. For example, the dV_d/dt of the low-side device is determined by the I_{RR} of the high-side device as shown on the right in Figure 3.1(d). The I_{RR} generated on the high-side SJMOS must flow to the low-side SJMOS. When the low-side current returns to the value of the load current after the I_{RR} reaches its peak, the drain voltage must change. The dV_d/dt depends on the I_{RR} peak and the active gate control should be focused on the I_{RR} peak. The determination of dV_d/dt by I_{RR} is a phenomenon unique to SJMOS and does not occur in devices such as IGBTs. As shown in Figure 3.1(d), the method of controlling gate current I_g in accordance with the transition of V_C, which is possible with IGBTs, cannot be applied to dV_d/dt control of SJMOS.



(a) Loss minimization by eliminating dV_d/dt variation



(b) Loss minimization by waveform shaping of I_d (c) Turn-on delay minimization



Current and voltage waveform of IGBT Current and voltage waveform of SJMOS

(d) I_{RR}-originated dV_d/dt control for SJSMO

Figure 3.1: Motivations of the active feedback in chapter 3.

Figure 3.1 summarizes the requirements and motivations for the active gate SR or dV_d/dt control for SJMOS discussed above. As shown in Figure 3.1(a), dV_d/dt variation due to device variation and environmental variations can be reduced to reduce losses. In the turn-on sequence, by improving the current dI_d/di during rise time, the loss can be further reduced as shown in Figure 3.1(b). Compared to resistive control, turn-on delay time shown in Figure 3.1(c) can

also be reduced by using active gate technology. For devices with large recovery current I_{RR} such as SJMOS, control based on I_{RR} is required because the dV_d/dt strongly depends on I_{RR} as shown in Figure 3.1(d).

In this work, a discrete-time background feedback that overcomes the challenges and satisfies all the motivations summarized in Figure 3.1(a)-(d) simultaneously is proposed. The proposed method controls the peak value of I_{RR} by switching between two resistors. A discrete-time feedback technique using capacitors and integrators can control the voltage SR depending on the I_{RR} by changing the resistor value at the next switching.

The remainder of this chapter is organized as follows. Section II shows the feature of the proposed discrete-time feedback scheme. The mechanism to control the SR and analysis to reduce loss are described in Section III. Section IV shows a detailed schematic of the discrete-time feedback. The measurement result is shown in Section V. Section VI concludes the paper.

3.2 Discrete-time feedback scheme

The feature of the discrete-time feedback scheme [66] is shown in Figure 3.2(a). The technique is based on time-domain switching of two values of gate resistance, namely, R_1 and R_2, where R_2 is much smaller than R_1. R_2 is activated in the initial part and the latter part of the switching cycle to boost the gate charging and shorten the turn-on delay. The duration of the intermediate high gate resistance state in which only R_1 feeds the gate current is controlled so that dV_d/dt reaches the maximum allowable SR and minimizes the switching loss. dV_d/dt originating in I_{RR} can be controlled as well thanks to the background feedback feature. Background here means that the loop samples the dV_d/dt in the previous cycle, reflecting it in duration of the high gate resistance state of the following cycles and achieving convergence in multiple switching cycles. As shown on the right in Figure 3.2(c), the pulse width of V_2 is modulated based on the sample results of V_d from previous cycles. In the loop, the transition period of V_d is translated into the voltage domain and sampled by the SR detector and held until the next switching cycle. The error voltage V_{err} indicates the integrated difference between the

sampled voltage and the reference voltage V_{ref_dvdt}, which reflects the target dV_d/dt. The V_{err} modulates pulse width of V_2 at the next switching cycle. The dV_d/dt is gradually increased in each switching cycle and finally settles to the target value as shown in Figure 3.2(b). The proposed SR Control (SRC) technique keeps the SR or dV_d/dt constant regardless of changes in the load current or temperature. And this minimizes the switching loss while the original dV_d/dt decreases and the loss increases as the load current or temperature decreases without SRC. As shown in Figure 3.2(c), the proposed feedback provides short turn-on delay without violating the SR guideline thanks to the fast gate charge by R_2 and regulating I_{RR} by R_1.

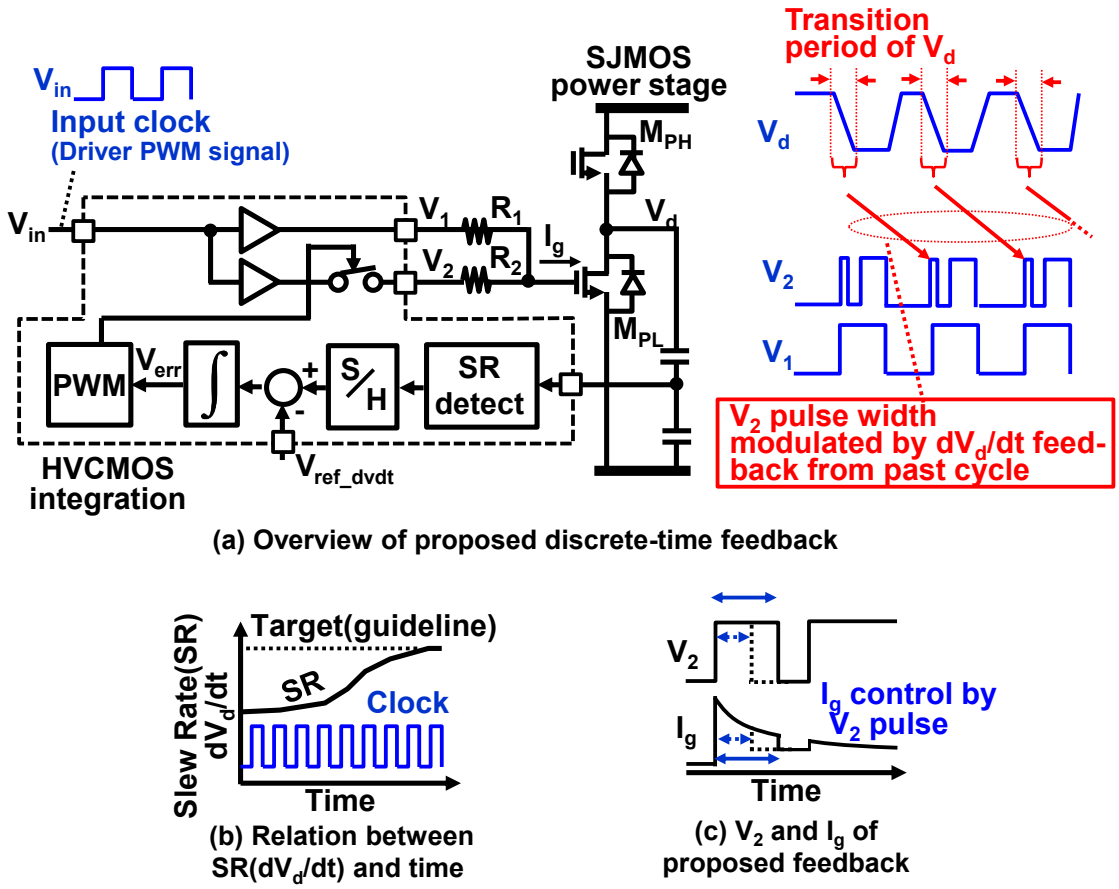


Figure 3.2: Proposed slew rate control gate driver with feedback.

3.3 The mechanism to control SR

The mechanism to control SR and shorten the turn-on delay is described in more detail in

Figure 3.3 and Figure 3.4 based on the waveform comparisons with and without the feedback. Figure 3.3 shows the waveform of a conventional gate driver and Figure 3.4 shows the waveform of the proposed gate driver. The turn-on sequence is shown in Figure 3.3 and Figure 3.4. The voltage V_1 is same as the gate driving PWM signal in Figure 3.3 and Figure 3.4. In the conventional control using a single resistor R_0 as shown in Figure 3.3, the gate voltage is charged by the resistor R_0 and the rise rate of the drain current I_d is determined by R_0. When the current value exceeds the load or inductor current I_{D0}, the recovery current starts to flow. The reverse recovery current (I_{RR1}) of the parasitic diode in M_{PH} and the load current I_{D0} flow in to the low-side device M_{PL} simultaneously. When all the recovery current has finished flowing, the current value returns to I_{D0} and the drain voltage decreases in proportion to the value of I_{RR}.

In the proposed gate driver shown in Figure 3.4, the voltage V_2 whose first pulse width is controlled by SRC rises at the same edge as voltage V_1, which represents the original gate drive PWM signal. At this point the gate-source capacitor of M_{PL} is mainly charged via the R_2 smaller than R_1. The reverse recovery current (I_{RR1}) of the parasitic diode in M_{PH} and the load current I_L=I_{D0} flow in to the low-side device M_{PL} simultaneously before the drain voltage V_d starts to fall. The peak of the I_d is the summation of I_{D0} and I_{RR1}. The V_2 falls to zero at t_2 and the gate voltage of the M_{PL} is charged via the large resistor R_1 and hence the speed of the I_d increment slows down. The I_d starts to decrease at t_3 and the V_d whose SR depends on I_{RR1} starts to decrease as well. When the falling edge of V_2 is moved from t_2 to t_1, the peak of I_d is decreased from (I_{D0}+I_{RR1}) to (I_{D0}+I_{RR2}). The speed of voltage transition that starts at t4 slows down because I_{RR2} is smaller than I_{RR1}. The SR can be controlled by modulating the falling edge of V_2. When compared with the waveforms by constant gate resistance shown in Figure 3.4, the SRC feedback clearly shortens the turn-on delay thanks to the fast charge via R_2.

Although there are several oms of parasitic gate resistance in the power device, the resistance value R_2 should not be too low to prevent gate oscillation. On the other hand, after the voltage transition is completed, the gate is again driven with a small resistance R_2. This is because if the gate is driven with a large resistance, it may malfunction due to noise from other inverters.

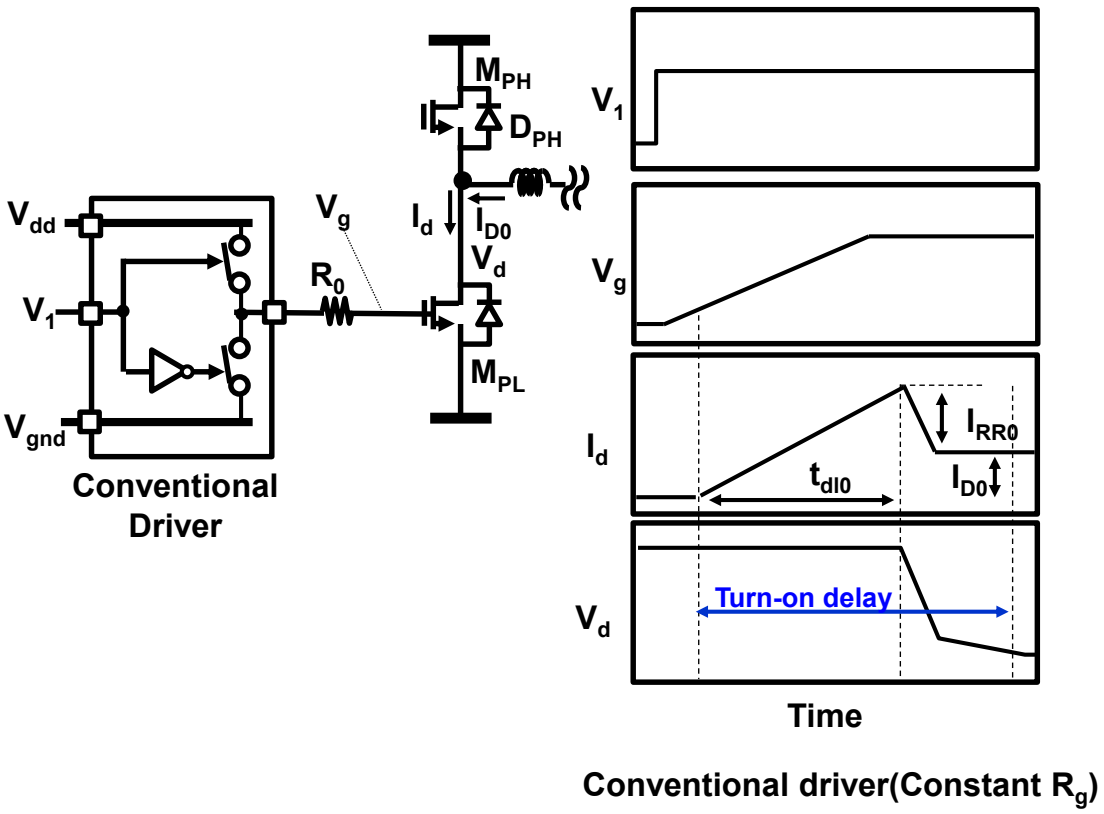


Figure 3.3: Time waveform of conventional gate driver.

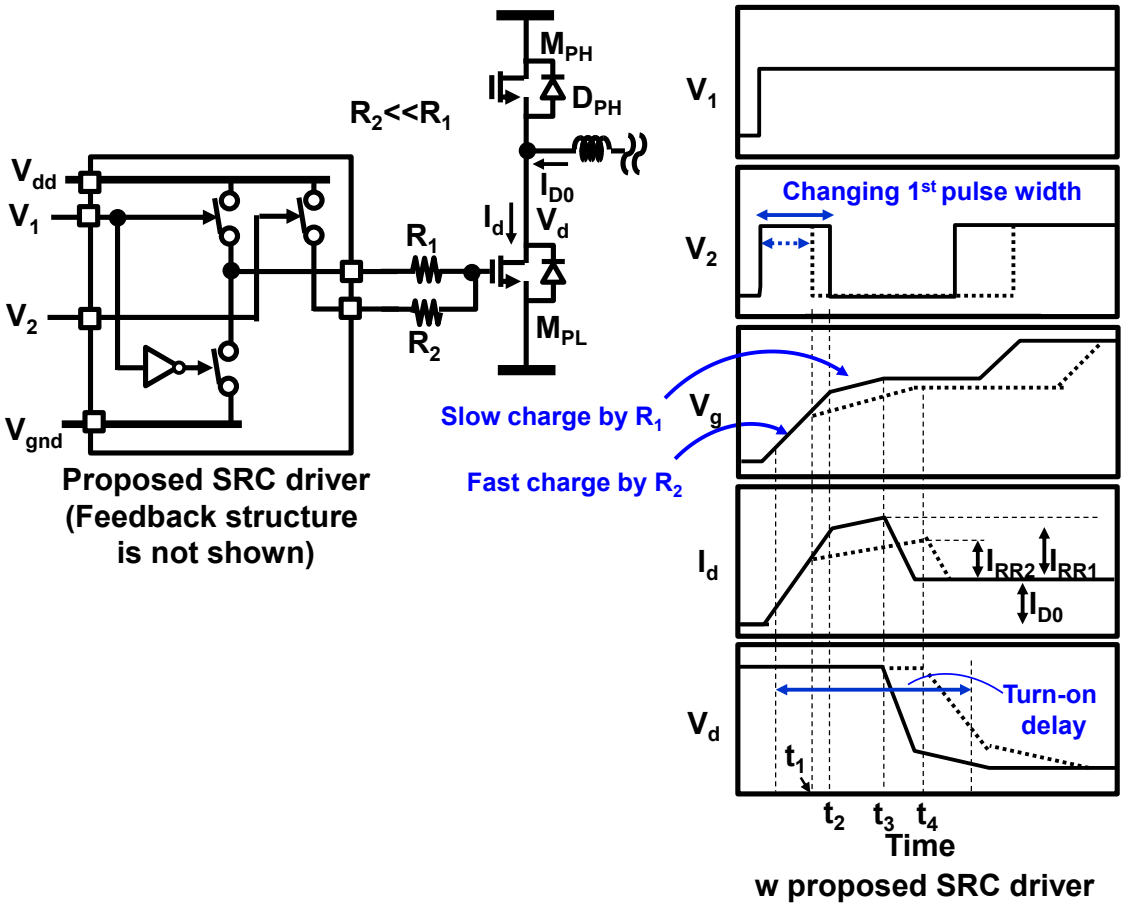


Figure 3.4: Time domain waveform of proposed gate driver.

3.4 The analysis of switching loss

The effect of loss reduction using SRC technology is explained using Figure 3.5. Figure 3.5(a) and Figure 3.5(b) show the drain current I_d and the recovery charge Q_{RR} of the conventional and the proposed gate driver, respectively. The comparison of drain current waveforms when dV_d/dt is equal is shown in Figure 3.5(a) and Figure 3.5(b). Therefore, the value of I_{RR} is equal in Figure 3.5(a) and Figure 3.5(b). The recovery charge is obtained by the area of the region where the drain current exceeds the load current I_{D0}. In Figure 3.5(a), the recovery charge of the conventional gate driver is $Q_{RR,cnv}$. In Figure 3.5(b), the recovery charge of the proposed gate driver is $Q_{RR,prp}$.

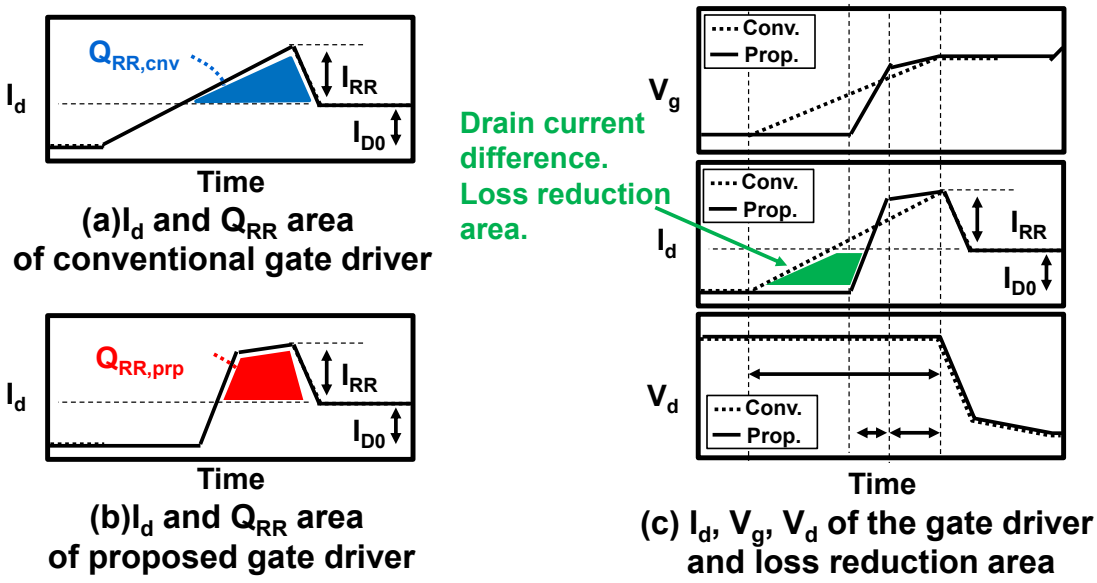


Figure 3.5: Loss reduction by waveform shaping of drain current.

It has been shown in previous work that the Q_{RR} can be given by the following equation [67].

$$Q_{RR} = k_{QRR}\sqrt{I_{D0}} \tag{3.1}$$

I_{D0} is the drain current and k_{QRR} is a coefficient related to the junction temperature and turn-off dI_d/dt. The turn-off dI_d/dt of the high-side diode corresponds to the turn-on dI_d/dt of the low-side SJMOS. As for the dI_d/dt, in the proposed method, the dI_d/dt is high in the section driven by a small resistance R_2, and the dI_d/dt is low in the section driven by a large resistance R_1. There is no previous work on Q_{RR} when the dI_d/dt is switched in the middle of the turn-on process. In this section, two cases are assumed and discussed. First, we will discuss the case where Q_{RR} is not sensitive to dI_d/dt and $Q_{RR,prp}$ and $Q_{RR,cnv}$ are equal. Next, we discuss the case where the Q_{RR} is sensitive to dI_d/dt and the Q_{RR} of the proposed method is not equal to the Q_{RR} of the conventional method. Finally, the simulation results will be used for discussion.

First, we discuss the loss reduction method when the $Q_{RR,prp}$ of the proposed method is equal to the $Q_{RR,cnv}$ of the conventional method. Figure 3.5(c) shows the drain current, the gate voltage, and drain voltage of the conventional and the proposed gate driver. The currents and voltages of the conventional gate driver are shown as dashed lines, and those of the proposed gate driver are

shown as solid lines. Since I_{RR} is equal, the slew rate or dV_d/dt of the drain voltage is the same in the conventional and the proposed gate driver. The switching loss is defined as the multiplication of drain voltage and drain current. And since the drain voltage waveforms are equal, the drain current difference shown in green in Figure 3.5(c) is the loss reduction.

The relationship between R_1 and R_2 that minimizes the loss is introduced. Figure 3.6 shows the drain current of the proposed gate driver. The region related to the turn-on current loss can be divided into Q_{RR} and Q_x, as shown in Figure 3.6. The current rise time can be divided into the time t_A and t_B, which are determined by the values of the parallel resistances of R_1 and R_2. However, R_2 is sufficiently smaller than R_1 that it can be approximated to be determined by R_2. And the time t_C, which is determined by the large resistance R_1. The time t_D is the time when the current I_{RR0} reaches load current I_{D0} and t_D does not change if the I_{RR} is kept constant. To minimize the switching loss, the electric charge Q_{total} which is the summation of Q_x and Q_{RR}, is minimized. Q_x is a function of t_A, t_B and t_C. The charge Q_{total} can be expressed by the following equation.

$$Q_{total} = Q_{RR} + Q_x(t_A, t_B, t_C) \tag{3.2}$$

$$Q_x(t_A, t_B, t_C) = 0.5I_{D0}(t_A + 2t_B + 2t_C + 2t_D) \tag{3.3}$$

As shown in equation (3.2) and (3.3), the sensitivity of time t_B and t_C to Q_{total} is equal. On the other hand, Q_{RR} can also be expressed using t_A, t_B, t_C, and t_D, I_{RR}, I_{DR1}, where I_{DR1} is the current that rises when driven by a large resistor R_1 as shown in Figure 3.6.

$$Q_{RR} = (0.5I_{RR0} - 0.5I_{DR1})t_B + (I_{RR0} + 0.5I_{DR1})t_C + 0.5I_{RR}t_D \tag{3.4}$$

The recovery charge Q_{RR}, shown in equation (3.4), must be a constant value as long as I_{D0} is constant. And the time t_C is more sensitive to Q_{RR} than time t_B because the coefficient of t_C is larger than t_B. To reduce Q_{total} and loss under the condition of constant Q_{RR}, make the rise of I_d as fast as possible and reduce Q_X. By choosing a resistance value that makes the time t_C as long as possible and the time t_B as short as possible, we can reduce the Q_{total} while keeping Q_{RR}

constant. It is preferable to choose as large a value as possible for R_1 and as small a value as possible for R_2.

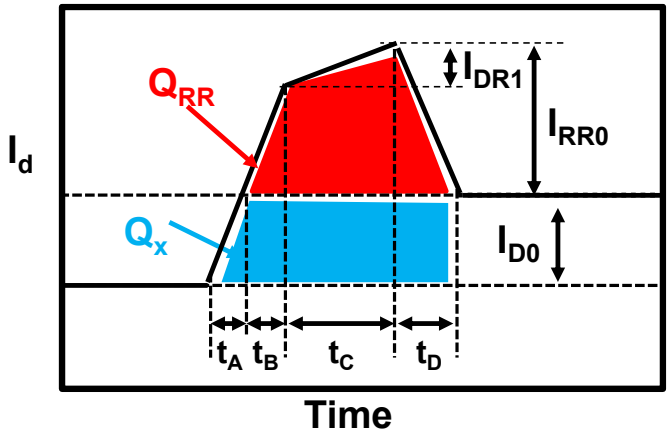


Figure 3.6: Loss calculation of proposed gate driver.

Next, the discussion of the optimal values of resistors R_1 and R_2 is given when the charge Q_{RR} is sensitive to dI_d/dt. By reducing both the charge Q_{RR} and Q_x, the loss can be reduced. From equation (3.3), when the resistance value R_2 is decreased, Q_x decreases as the time t_a decreases. On the other hand, decreasing resistance value R_2 increases dI_d/dt, which increases Q_{RR}. When the charge Q_{RR} is not sensitive to dI_d/dt, the smaller the resistance R_2, the lower the loss. When the charge Q_{RR} is sensitive to dI_d/dt there is an optimum value for resistance R_2. This is because as resistance R_2 is decreased, Q_x is decreased and Q_{RR} is increased. Increasing the resistance R_1 also reduces Q_x by decreasing the time t_c and increasing the time t_b. However, as the time driven by the resistance value R_1 increases, the charge Q_{RR} increases, and the loss increases. There is an optimum value for resistance R_1 as well.

Next, the discussion is presented using the simulation results. First, the characteristics of power devices are introduced and the accuracy of the models used to simulate power devices is discussed. Then, simulations are performed on multiple devices to verify that the proposed control works. Next, the relationship between two gate resistance values and power dissipation is clarified. The Cadence Spectre was used as the simulator. The power device used in the simulation is 600 V-class superjunction MOSFETs (TK8A60W5). The device TK8A60W5 [68] is often used in compressors for household appliances that have a large market size. The

specifications such as breakdown voltage, current rating, and charge Q_{RR} are shown in Table 3.1. In this simulation, the system was configured such that the drain current I_{D0} does not exceed half of the maximum current value listed in the specification. In other words, the drain current I_{D0} should be between 0 and 4A. Also, the charge Q_{RR} of this device is 3.5 uC. The device TK39N60W5 [69], which has a higher current rating, was also used in the simulation for comparative. The high-accuracy model presented in the literature [70] is used for the simulation, and the nonlinearity of the parasitic capacitance is modeled within an error of 2% [70]. Therefore, the transient characteristics of the rising drain current and falling drain voltage can be simulated with high accuracy. On the other hand, the recovery charge Q_{RR} of the diode is not described in the literature [70]. Therefore, the recovery charge Q_{RR} described in the datasheet of each device was compared with the recovery charge Q_{RR} obtained by simulation. Table 3.2 shows the results of the charge Q_{RR} comparison. As shown in Table 3.2, differences exist in the amount of charge Q_{RR} between the simulated and datasheet values, with a ratio of 37% for TK8A60W5 and 50% for TK39N60W5. The accuracy of the model is low with respect to the recovery charge Q_{RR}, which is a note of caution when considering the simulation results.

Table 3.1: Specification of the device used in the simulation.

Device name	**TK8A60W5**	**TK39N60W5**
Breakdown drain-source voltage	**600 V**	**600 V**
Maximum drain current	**8 A**	**39 A**
On resistance	**0.44 ohm**	**0.062 ohm**
Reverse recovery charge Q_{RR}	**0.35 uC**	**1.2 uC**
Peak reverse recovery current I_{RR}	**9.2 A**	**13 A**
Internal gate resistance	**7.5 ohm**	**2 ohm**

Table 3.2: Comparison of charge Q_{RR} and current I_{RR} value from simulation and datasheet.

	TK8A60W5		TK39N60W5	
	Datasheets value	**Simulation**	**Datasheets value**	**Simulation**
Reverse recovery charge Q_{RR}	**0.35 uC**	**0.22 uC**	**1.2 uC**	**2.4 uC**
Peak reverse recovery current I_{RR}	**9.2 A**	**7.7 A**	**13 A**	**40 A**

Figure 3.7 shows the results of the proposed feedback control using devices TK39N60W5 and TK8A60W5. When the control voltage of resistor R_2 reaches 5 V, resistor R_2 is enabled. Table 3.3 also shows the values of R_1 and R_2 used and the value of dV_d/dt. The dV_d/dt is the absolute value of the slope of the drain voltage from 90% to 20% of the power stage supply voltage. The devices TK39N60W5 and TK8A60W5 differ in the value of charge Q_{RR} by a factor of 10 or more, however, the feedback works to keep dV_d/dt constant.

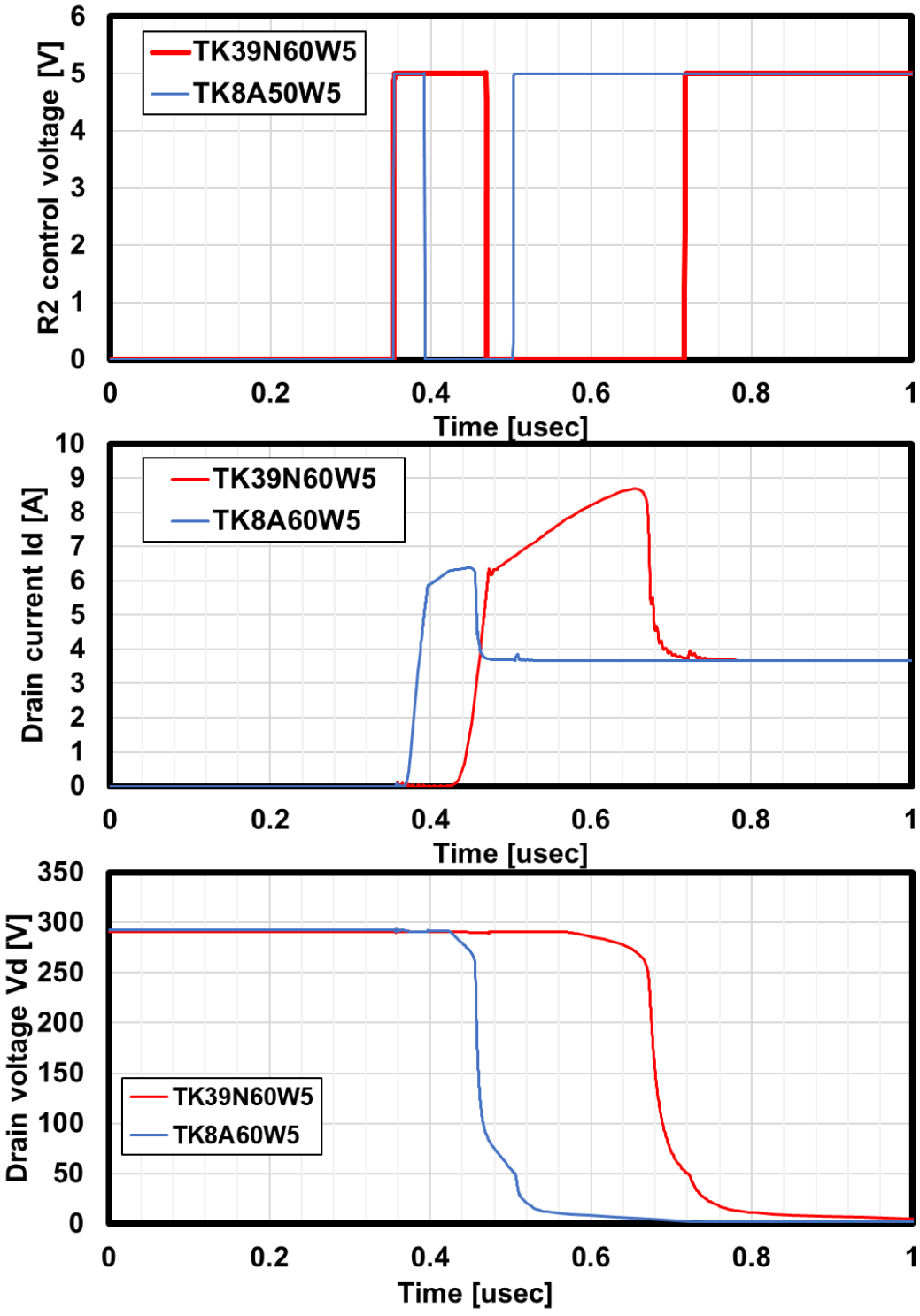


Figure 3.7: Simulation of the proposed feedback control with device TK39N60W5 and TK8A60W5.

Table 3.3: The resistance and dV_d/dt value of simulation in Figure 3.7.

Device name	TK8A60W5	TK39 N60W5
R1	450 ohm	450 ohm
R2	10 ohm	10 ohm
dV_d/dt (90% to 20%)	5.3V/nsec	5.4V/nsec

Next, the relationship between two gate resistance values and power dissipation is clarified by using the device TK8A60W5. Figure 3.8 shows the simulation results with R_1 fixed and R_2 swept, where R_1 is fixed at 450 ohm and R_2 is 50 ohm, 100 ohm and 210 ohm. The drain voltage V_d and drain current I_{D0} in the simulation are 290V and 3.7A, respectively. Figure 3.8 also shows the simulation results when the device is driven with a resistance value of 220 ohm without feedback. Table 3.4 also shows the values of Q_{total}, Q_{RR}, Q_x switching (SW) loss, time t_a+t_b driven by resistance value R_2, and time t_c driven by resistance value R_1 for each simulation result. According to the simulation results, when resistance R_2 is 100 ohm and resistance R_1 is 450 ohm, the time t_a+t_b and t_c are 0.08 us and 0.036 us respectively. The peak value of the recovery current, I_{RR0}, is 2.9A, and the time t_d is about 0.01us. As shown in Table 3.2, using the model of device TK8A60W5, the charge Q_{RR} is not constant, and the value of Q_{RR} changes with the presence of feedback. Comparing the results for different resistance values R_2 with feedback, the smaller the resistance value R_2 is, the more the time t_a and t_b decrease and the time t_c increases. The charge Q_{total} and Q_x decrease with shorter time t_a and t_b. In the device model TK8A60W5, reducing the resistance R_2 and shortening the time t_a+t_b increases the charge Q_{RR}. However, the charge Q_x can be reduced, resulting in a reduction in charge Q_{total} and switching loss.

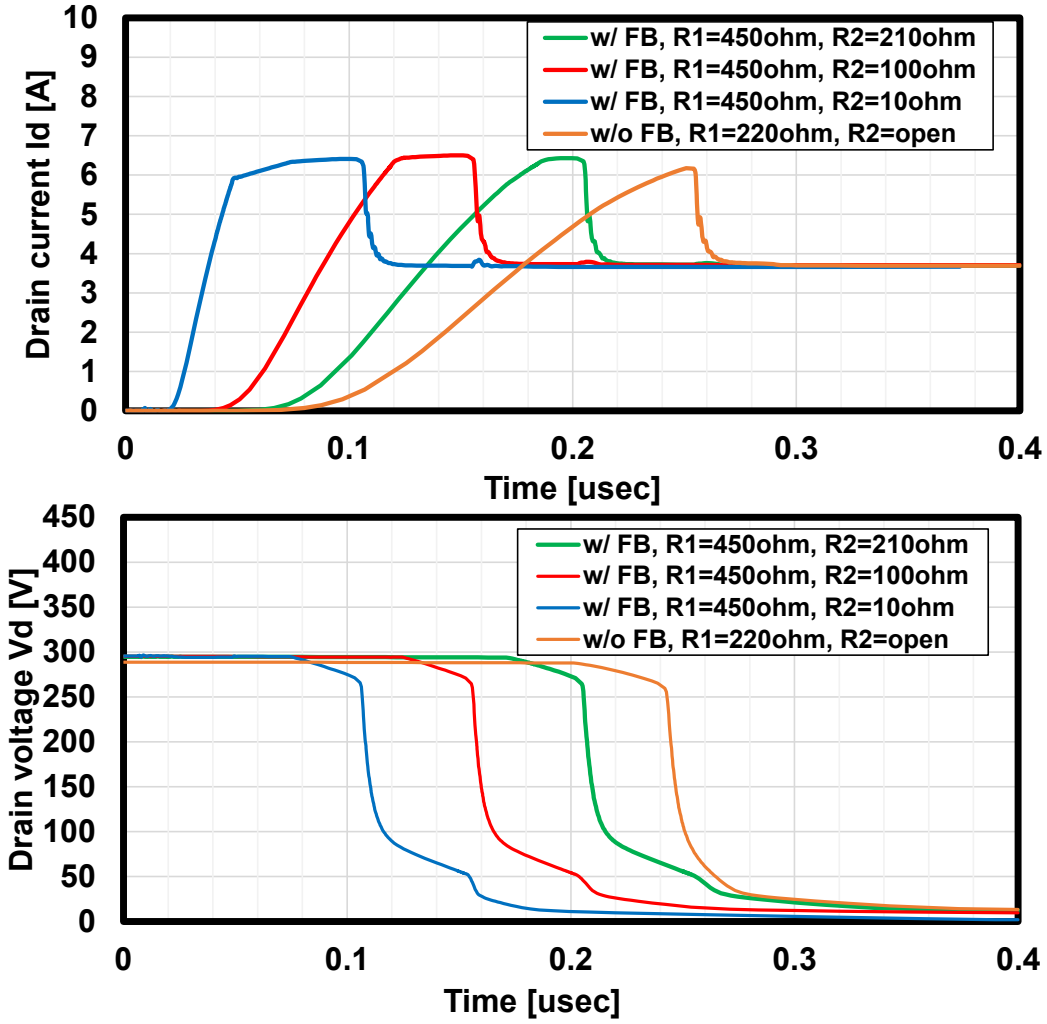


Figure 3.8: Simulation results for the case where the resistance value R_1 is fixed and R_2 is varied.

Table 3.4: Simulation results of charge Q_{total}l, Q_x, Q_{RR}, switching loss, and time t_a+t_b, t_c where resistance value R_1 is fixed and R_2 is varied.

Feedback (FB)	R_1 [Ohm]	R_2 [Ohm]	Q_{total} [uC]	Q_{RR} [uC]	Q_x [uC]	SW loss [mJ]	t_a+t_b [usec]	t_c [usec]
w/ FB	450	10	0.488	0.169	0.319	0.144	0.028	0.058
w/ FB	450	100	0.503	0.148	0.355	0.149	0.08	0.036
w/ FB	450	210	0.525	0.132	0.393	0.157	0.125	0.2
w/o FB	220	open	0.588	0.120	0.468	0.163	0.176	NA

Figure 3.9 shows the results when the resistance R_2 is fixed and R_1 is varied. The simulation results of drain current and drain voltage when resistance R_2 is fixed at 10 ohm and resistance R_1 is 450 ohm, 550 ohm and 650 ohm are shown. Table 3.5 shows the values of Q_{total}, switching loss, time t_a+t_b driven by resistance R_2, and time t_c driven by resistance R_1 in each simulation result. As resistance R_1 is increased, the amount of charge Q_{total} and switching loss decreases. Using the device model TK8A60W5, the charge Q_{RR} increases with increasing R_1. However, the charge Q_x decreases, resulting in a decrease in the charge Q_{total}. As the resistance value R_1 is increased, the time t_c is also decreased and the time t_a+t_b is increased. In case of using the device TK8A60W5, the loss can be reduced by increasing the resistance R_1 and decreasing the resistance R_2.

The loss reduction ratio with a larger resistor R_1 is 1.4%, which is smaller than the loss reduction ratio with a smaller resistor R_2, which is 12%. The resistor R_1 affects the drain current rise performance. The rise of drain current is affected by the capacitance characteristics of the power device. Since the model used in this study has highly accurate capacitance characteristics, the simulation also showed that a smaller resistor R_2 resulted in lower loss. On the other hand, the resistance R_1 mainly affects the behavior of the recovery charge. As shown in Table 3.2, the recovery charge is not accurately modeled. Therefore, the simulation confirmed the loss reduction effect of resistance R_1, however, it was as small as 1.4%. It is necessary to confirm the loss reduction effect by R_1 in measurements.

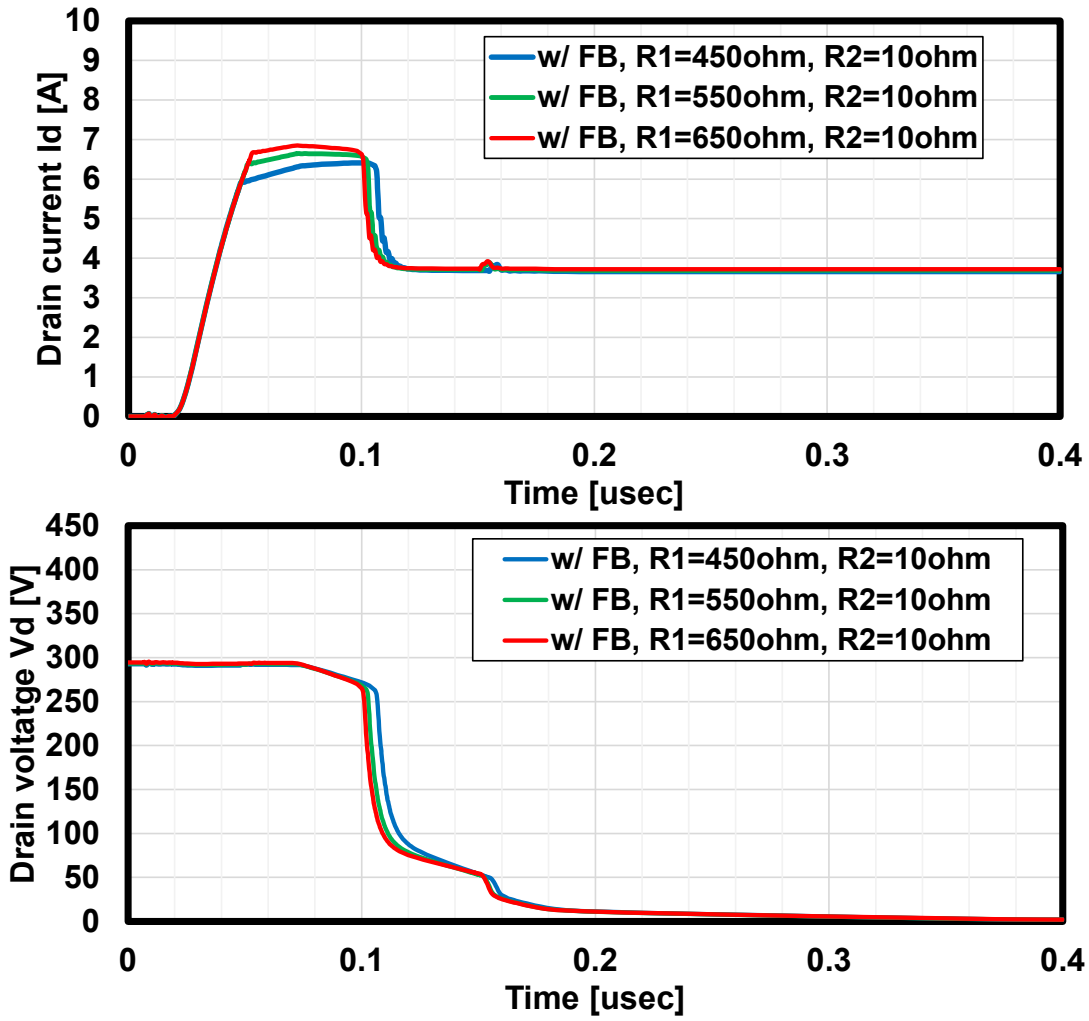


Figure 3.9: Simulation results for the case where the resistance value R_2 is fixed and R_1 is varied.

Table 3.5: Simulation results of charge Q_{total}l, Q_x, Q_{RR}, switching loss, and time t_a+t_b, t_c where resistance value R_2 is fixed and R_1 is varied.

Feedback (FB)	R_1 [Ohm]	R_2 [Ohm]	Q_{total} [uC]	Q_{RR} [uC]	Q_x [uC]	SW loss [mJ]	t_a+t_b [usec]	t_c [usec]
w/ FB	450	10	0.488	0.169	0.319	0.144	0.028	0.058
w/ FB	550	10	0.481	0.174	0.307	0.1423	0.03	0.051
w/ FB	650	10	0.479	0.176	0.303	0.1420	0.032	0.047

3.5 Detailed circuit schematic and time domain waveform

Detailed schematics of the proposed SRC feedback driver and its waveforms are shown in Figure 3.10 and Figure 3.11, respectively. It consists of SR-to-voltage sampling (SRVS) block, error amplifier, and PWM block. A voltage-domain error amplifier is adopted to provide the target SR or dV_d/dt in a voltage domain. To accommodate this, the SR information is converted to a voltage domain at the SRVS block. As discussed below, interleaving operation in SRVS reduces timing complexity of timing generation. The comparators CMP_1 and CMP_2 compare the divided drain voltage V_{d_fb} to the reference voltages, V_{refH} and V_{refL}. The switch S_1 turns-on when the divided voltage V_{d_fb} stays between the reference voltages, V_{refH} and V_{refL}, as shown in Figure 3.11. The pulse width of T_p represents the duration of the drain voltage transition and is inversely proportional to SR. The T_p is converted to the voltage V_{SL1} by charging the capacitor C_1 , with current source I_1, as shown in Figure 3.10. In this work, the capacitance C_1 and C_2 are located outside of the chip and the value is 100pF. The value of the capacitor should be chosen so that it can hold the charge while the voltage V_{in} switches two times. The charge C_1 x V_{SL1} is transferred to the capacitor C_{itg} at the timing of V_{SW3}. After a period of a half-switching cycle, V_{SL1} is reset.

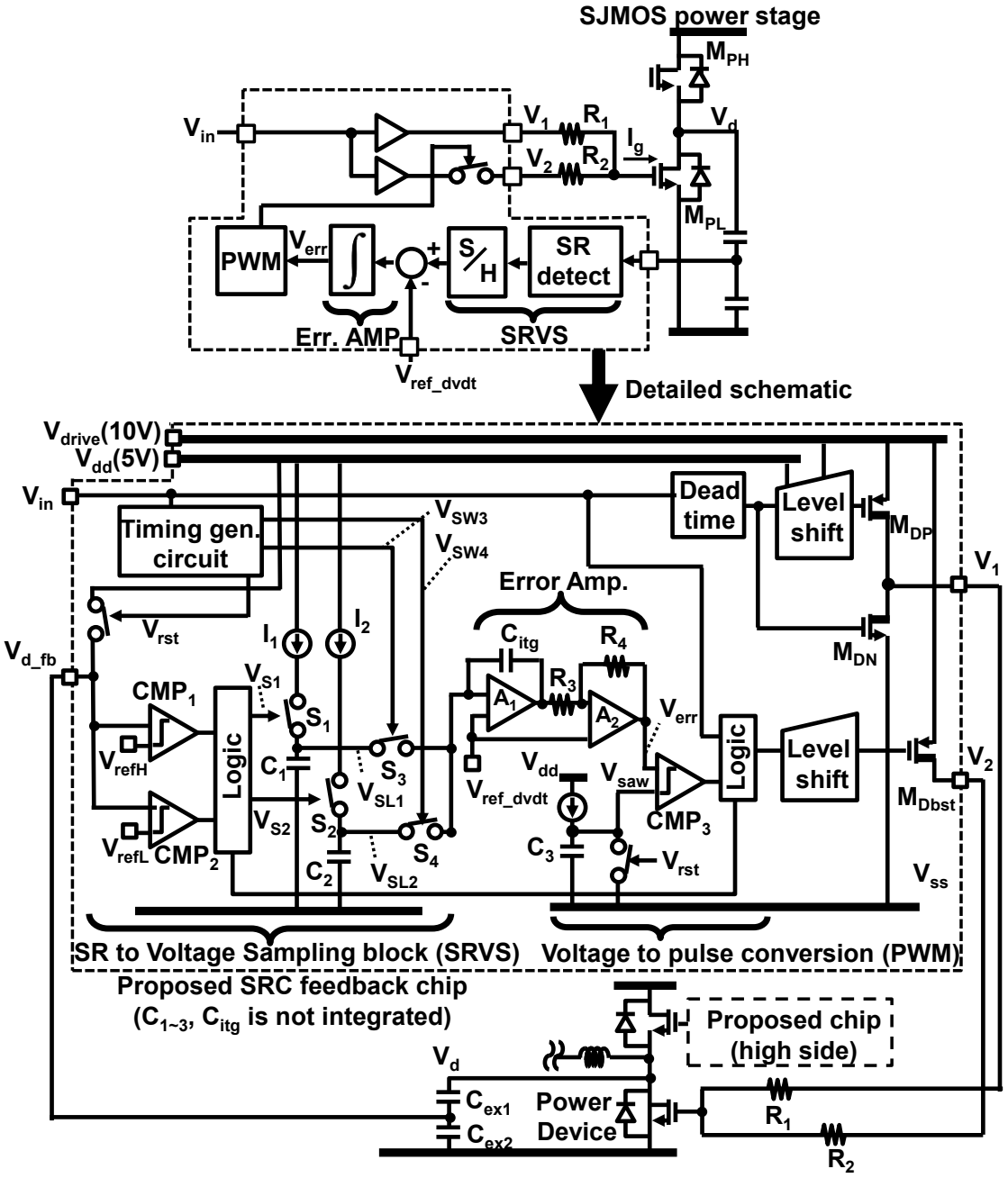


Figure 3.10: Circuit diagram.

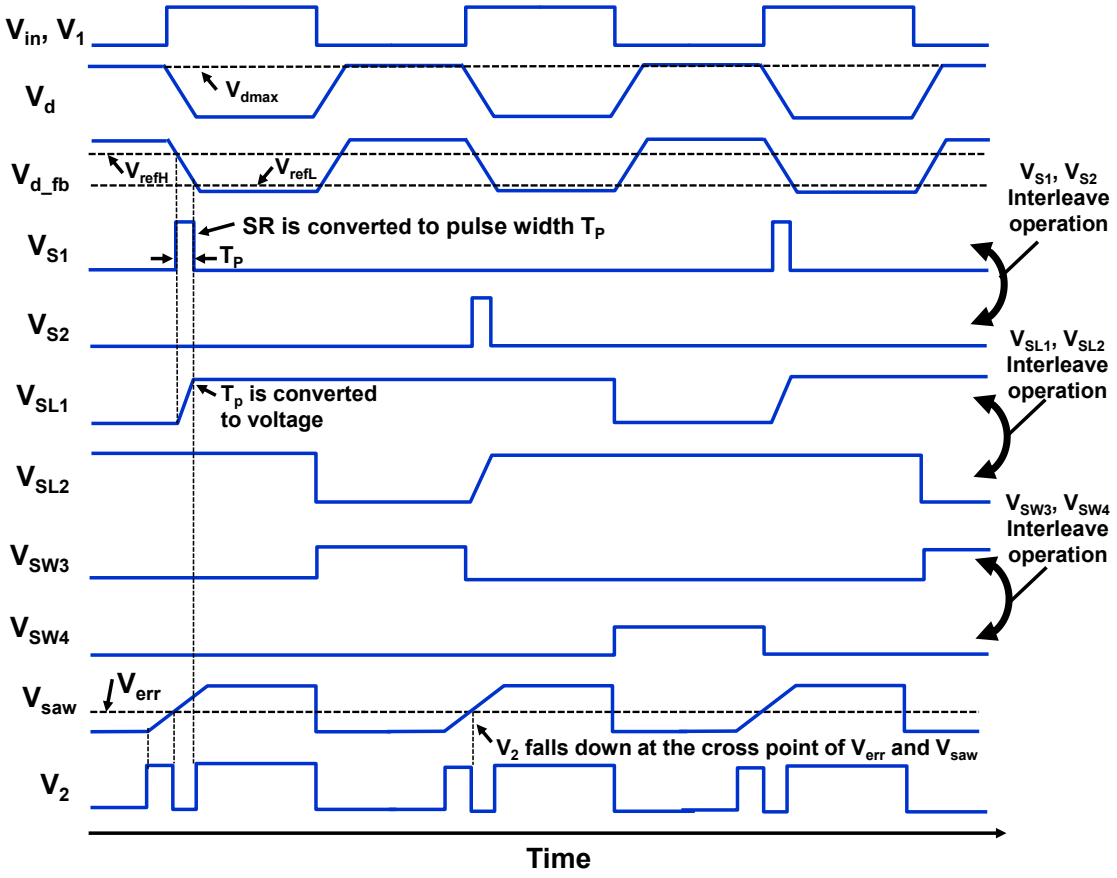


Figure 3.11: Transient waveform.

As shown in Figure 3.11, V_{S1}/V_{S2}, V_{SL1}/V_{SL2}, and V_{SW3} /V_{SW4} operate in an interleaving fashion, respectively. The interleaving operation reduces complexity of timing generation, since all of the above-mentioned switching timing can be generated based on V_{in}, which represents the original gate drive PWM signal. The output voltage of the error amplifier V_{err} represents the integrated error between the target transition indicated by reference voltage V_{ref_dvdt} and the measured transition indicated as V_{SL1} and V_{SL2}. The falling edge of V_2 is decided by the cross point of the V_{err} and the saw-tooth waveform V_{saw}. Finally, the voltage information is converted into the timing by using the comparator CMP_3. The pulse width of the V_2 is increased when the V_{err} is large, resulting in the increment of the I_{RR} and SR. The end of the transition of the drain voltage V_d is detected by comparing the voltage V_{d_fb} with the threshold voltage V_{refL} of the comparator. The V_2 rises again when the V_{d_fb} reaches V_{ref_L} so that the gate is driven via low-resistance R_2 after the power device turns on. By keeping the gate in low impedance, it

prevents malfunctions caused by noise from other inverters.

Figure 3.12 shows a circuit diagram of the timing generation circuit and error amplifier. The timing generation circuit uses a frequency divider circuit to generate interleaved signals. The error amplifier is a simple differential circuit configuration. The comparator uses a circuit that combines NMOS and PMOS differential circuits as shown in reference [13].

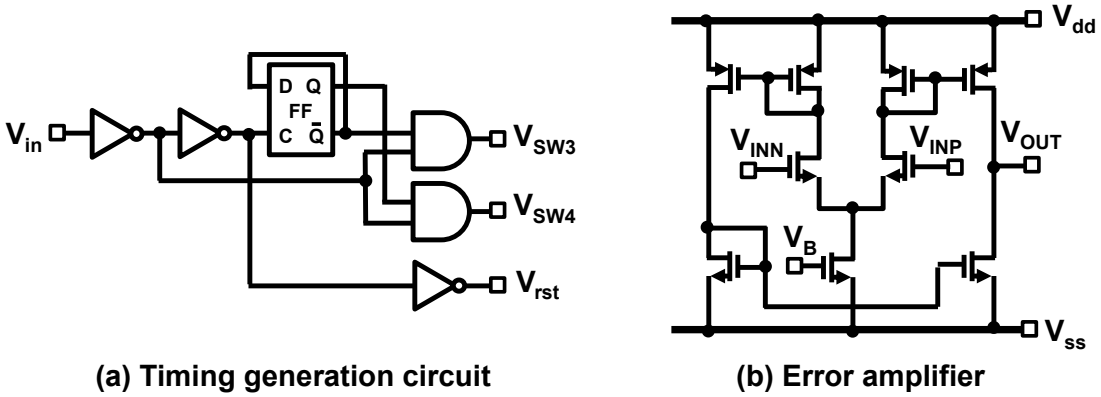


Figure 3.12: Circuit diagram of the timing generation circuit and error amplifier.

If the drain voltage V_d varies with the application, or if the target value of dV_d/dt is to be varied, the input value of the integrator's reference voltage V_{ref_dvdt} is changed. The relationship between the target dV_d/dt and the reference voltage V_{ref_dvdt} of the integrator is shown below. If target dV_d/dt is the speed at which the drain voltage V_d transitions from 90% to 10% of its maximum value V_{dmax} shown in Figure 3.11, the relationship between the sampled time T_p, the maximum drain voltage value V_{dmax}, and dV_d/dt is expressed by the following equation.

$$T_p = \frac{0.9V_{dmax} - 0.1V_{dmax}}{\frac{dV_d}{dt}} \tag{3.5}$$

The time T_p is converted to a voltage by capacitor C_1 and current I_1. The reference voltage V_{ref_dvdt} and time T_p of the integrator are expressed by the following equation.

$$V_{ref\_dvdt} = \frac{I_1}{C_1} \cdot T_p \tag{3.6}$$

From equations (3.5) and (3.6), the relationship between the reference voltage of the integrator V_{ref_dvdt} and the target dV_d/dt can be expressed by the following equation.

$$V_{ref\_dvdt} = \frac{I_1}{C_1} \cdot \frac{0.9V_{dmax} - 0.1V_{dmax}}{\frac{dV_d}{dt}} \tag{3.7}$$

When the target dV_d/dt or drain voltage changes, the reference voltage of the integrator V_{ref_dvdt} must be changed with reference to equation (3.7).

The values of capacitors C_{ex1} and C_{ex2} are 10 pF and 1000 pF, respectively, and the drain voltage V_d is divided by a factor of 100. The threshold values V_{refH} and V_{refL} should be set so that the divided voltage can be detected. When the drain voltage V_d transitions from 0V to 280V and the capacitance divider ratio is set to 1/100, a transition time of 10% to 90% can be obtained by setting V_{refH} to 2.52V and V_{refL} to 0.2 V. The comparator operates at 0V to 5V. In this work, the drain voltage is assumed to be a ramp wave. In applications where dV_d/dt exceeds 20 V/nsec ringing may occur in the drain voltage. Ringing causes the comparator threshold to be exceeded many times, resulting in false detection of the transition time. For applications where dV_d/dt is high speed, the layout of the inverter board should be carefully designed to avoid ringing.

It takes about 10 switching cycles for the feedback to converge. During the settling transient period, the value of dV_d/dt may oscillate depending on the conditions. The stability can be improved by adjusting the integrating capacitance C_{itg}. If dV_d/dt is unstable, it is necessary to control the loop by adjusting the integrating capacitance Citg by actual measurement. Increasing the value of the capacitance C_{itg} stabilizes the loop. However, it increases the number of switching cycles until the dV_d/dt reaches the desired value.

The use of multiple capacitances C_1 and C_2 to sample time may result in inconsistent sampling times due to variations in capacitance. The presence of a capacity mismatch can cause dV_d/dt to fluctuate. The effect of keeping dV_d/dt constant and reducing losses becomes compromised. By matching the capacitance values of the capacitors to the factory test, the discrepancy in sampling time can be avoided.

In this work, the device to be controlled was a low-side SJMOS. However, the high-side

SJMOS should be controlled in the same way. This is because the dV_d/dt of the high-side is determined by the Q_{RR} of the low-side.

3.6 Measurement result

To evaluate the continuous operation of the proposed SRC driver, it was implemented in a low-side switch of a boost converter. Figure 3.13 shows the photograph of the measurement setup and circuit schematic. 600 V-class superjunction MOSFETs (TK8A60W5) are utilized for both the low-side switch and the high-side diode whose gate-source terminals are shortened. Figure 3.14 shows the measured transient waveforms at a low temperature of 45 °C centigrade and a high temperature of 95 °C. The peak of the I_{RR} was kept constant by SRC feedback against temperature change. The width of the boost pulse V_2 is modulated to keep I_{RR} and dV_d/dt constant. The proposed SRC feedback that keeps dV_d/dt constant and shortens the turn-on delay is demonstrated.

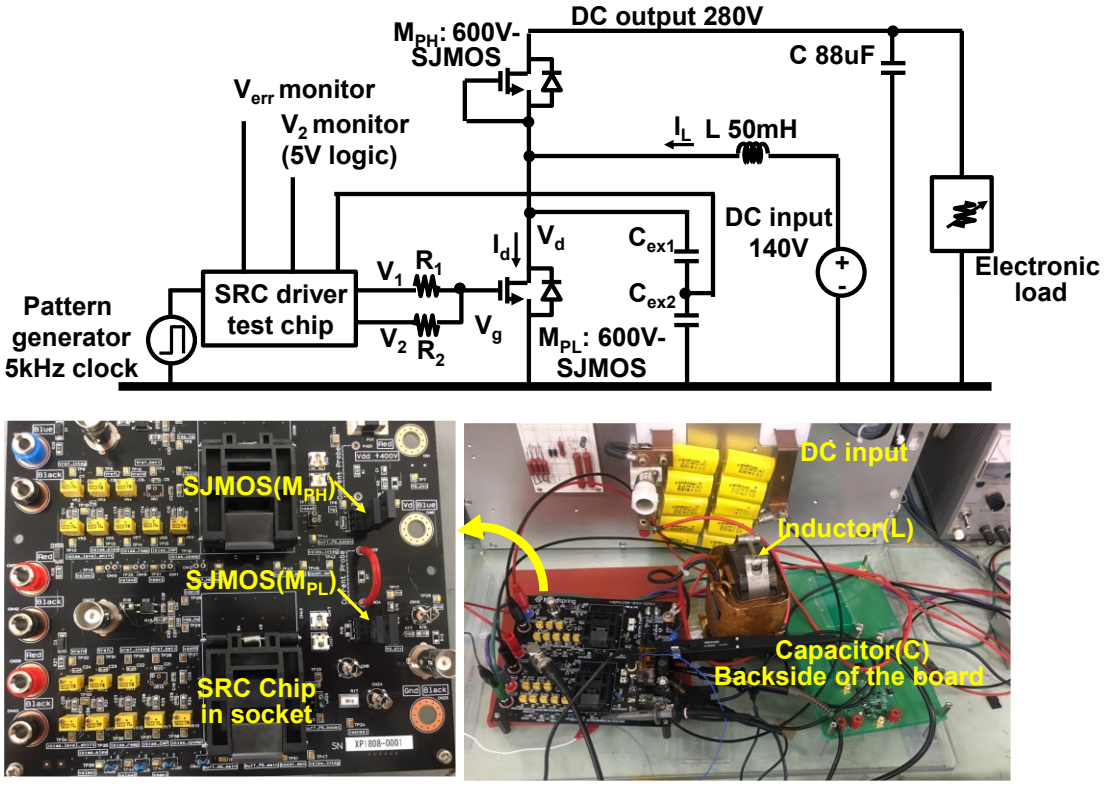
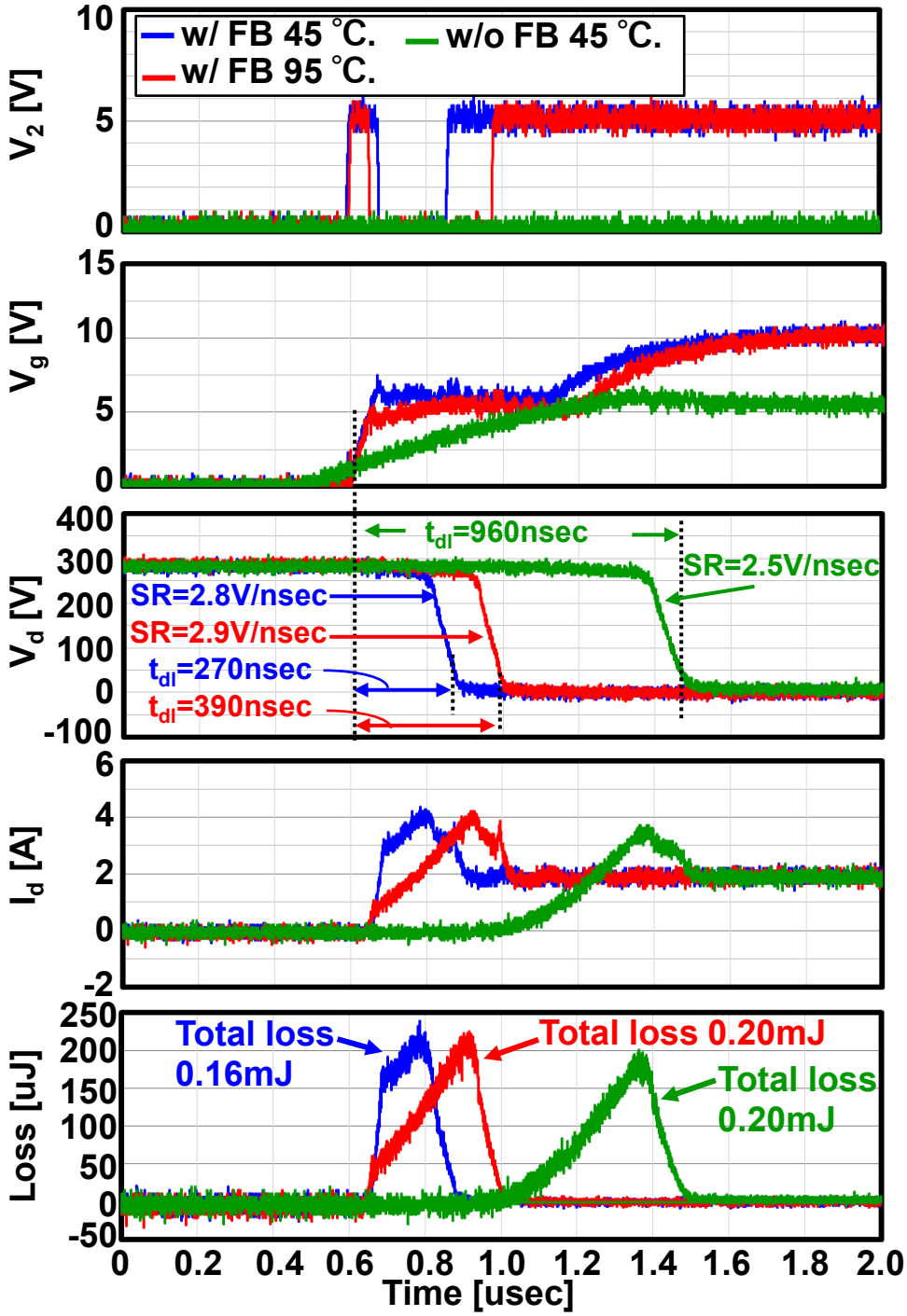


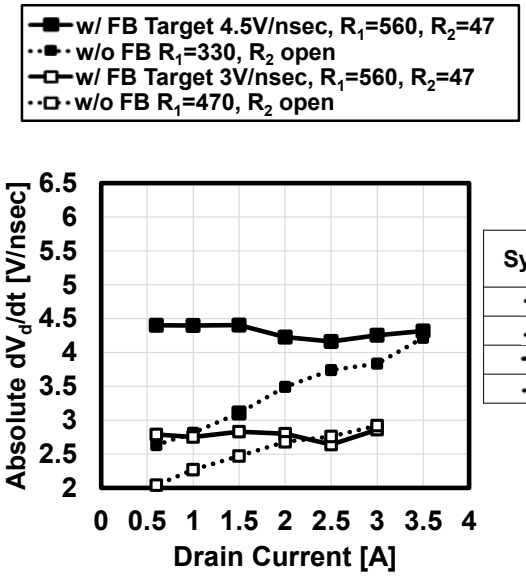
Figure 3.13: Photograph of the measurement setup and circuit schematic.



Symbol	Feedback	Target SR	R1	R2	Other
—	w/ FB	3V/nsec	560	47	Temperature＝45℃
—	w/ FB	3V/nsec	560	47	Temperature＝95℃
—	w/o FB	-	470	Open	Temperature＝45℃

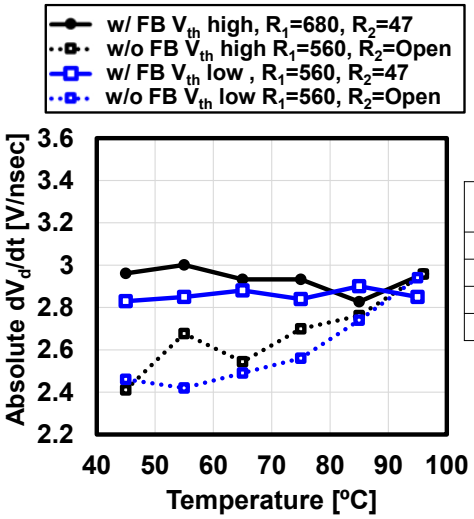
Figure 3.14: Measured waveform w/ and w/o feedback.

Figure 3.15 shows the measured dV_d/dt with different drain current. As shown in Figure 3.15, dV_d/dt is decreased as the load current decreases without SRC feedback. It is kept constant at 4.5 V/nsec or 3 V/nsec depending on the reference voltage of V_{ref_dvdt} by the SRC feedback. The dV_d/dt variation is compressed from 37% to 7% when the target is 4.5V/nsec and from 31% to 10% when the target is 3.3V/nsec. Figure 3.16 shows the temperature characteristics of dV_d/dt. Thanks to SRC feedback, dV_d/dt is kept constant. The measurement results of samples with different threshold voltage are also shown in Figure 3.16. The dV_d/dt is kept constant with different threshold voltages. In the measurements, a heat sink was connected to the metal plate on the back side of the SJMOS TO220 package. The temperature was measured by inserting a thermocouple between the heat sink and the metal plate on the backside.



Symbol	Feedback	dV_d/dt goal [V/nsec]	R_1 [ohm]	R_2 [ohm]
	w/ FB	4.5	560	47
	w/o FB	-	330	Open
	w/ FB	3	560	47
	w/o FB	-	470	Open

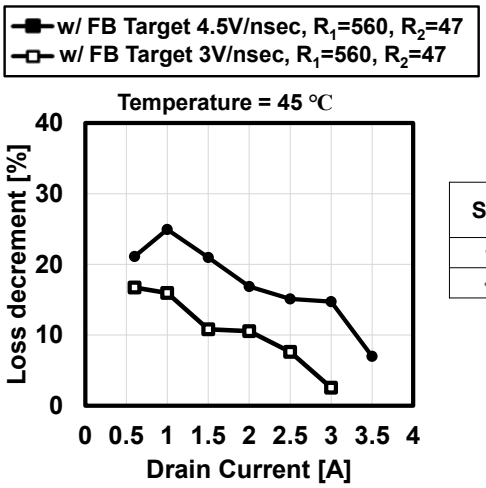
Figure 3.15: Measured dV_d/dt with drain current.



Symbol	Feedback	dV_d/dt goal [V/nsec]	R_1 [ohm]	R_2 [ohm]	Device V_{th}
	w/ FB	3	680	47	High V_{th}
	w/o FB	-	560	Open	High V_{th}
	w/ FB	3	560	47	Low V_{th}
	w/o FB	-	560	Open	Low V_{th}

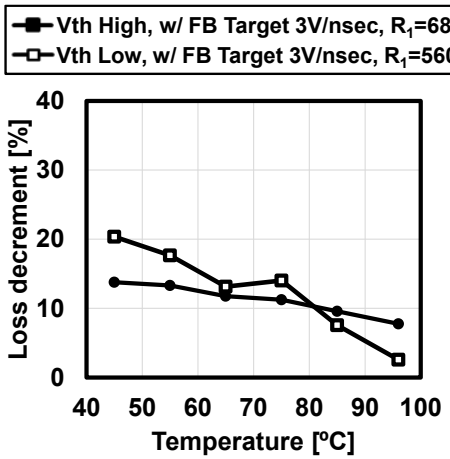
Figure 3.16: Measured dVd/dt with V_{th} and temperature.

Figure 3.17 and Figure 3.18 show the loss decrement ratio (1 - E_w/E_{wo}), where E_w and E_{wo} are the switching losses with/without SRC feedback, respectively. The maximum loss reductions are 25 % and 20 % at I_d of 1 A and temperature of 45 ºC., respectively.



Symbol	Feedback	dV_d/dt goal [V/nsec]	R_1 [ohm]	R_2 [ohm]
	w/ FB	4.5	560	47
	w/ FB	3	560	47

Figure 3.17: Measured loss decrement ratio with drain current.

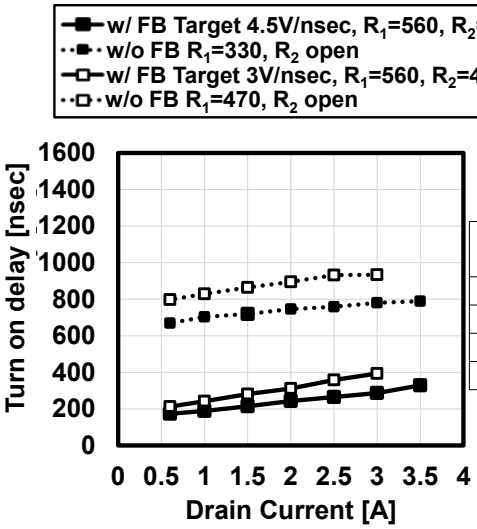


Symbol	Feedback	dV_d/dt goal [V/nsec]	R_1 [ohm]	R_2 [ohm]	Device V_{th}
■	w/ FB	3	560	47	High V_{th}
□	w/ FB	3	560	47	Low V_{th}

Figure 3.18: Measured loss decrement ratio with temperature.

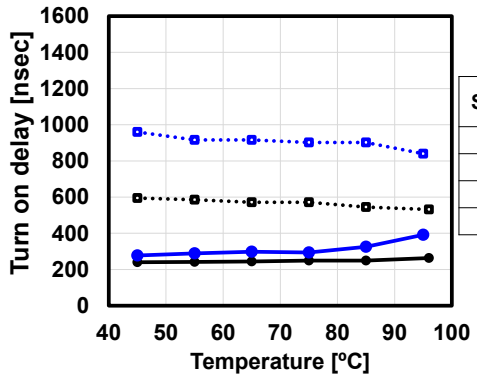
Depending on the operating conditions of the inverter, the loss reduction effect of the entire system will have various values. Based on the results in Figure 3.15 and referring to the information in Fuji Electric's application note [71], the following is an example of inverter configuration and estimated loss reduction effect. When an inverter with a maximum current of 3.5A, maximum dV_d/dt of 4.5 V/nsec, power factor of 0.8, and frequency of 10 kHz is configured with TK8A60W5 devices, the power device loss reduction effect is 7%.

Figure 3.19 and Figure 3.20 show the measured turn-on delays for different current and temperature. The turn-on delay t_{dl} is defined by the period between when the V_{gs} reaches 10% of the maximum value and when the V_d reaches 10% of the maximum value. The t_{dl} reduction of 74% is achieved by the SRC feedback.



Symbol	Feedback	dV_d/dt goal [V/nsec]	R_1 [ohm]	R2 [ohm]
	w/ FB	4.5	560	47
	w/o FB	-	330	Open
	w/ FB	3	560	47
	w/o FB	-	470	Open

Figure 3.19: Measured turn-on delay with drain current.

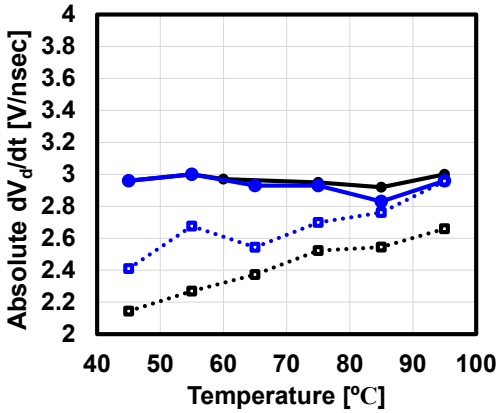


Symbol	Feedback	dV_d/dt goal [V/nsec]	R_1 [ohm]	R_2 [ohm]	Device V_{th}
	w/ FB	3	680	47	High V_{th}
	w/o FB	-	560	Open	High V_{th}
	w/ FB	3	560	47	Low V_{th}
	w/o FB	-	560	Open	Low V_{th}

Figure 3.20: Measured turn on delay with temperature.

Figure 3.21 shows the measured dV_d/dt with different gate resistance R_1 and R_2. Measured dV_d/dt is kept constant by the feedback even if the resistance is varied. The resistance values of several hundred ohms used in Figure 3.15 to Figure 3.21 are not optimal in terms of losses. Increasing R_1 and decreasing R_2 can reduce the losses for the same dV_d/dt. The discussion on the optimal resistance values R_1 and R_2 is done using a Table 3.4. Table 3.6 shows the measurement result of the dV_d/dt and switching loss with different gate resistance R_1 and R_2. The current I_L is the inductor load current shown in Figure 3.13. The top part of Table 3.4 shows the results and losses with feedback for two different dV_d/dt. The middle of Table 3.6 shows the

results for variable R_1 and fixed R_2, where larger R_1 reduces the loss for the same dV_d/dt. The bottom of Table 3.6 shows the results when the resistance value R_1 is fixed and the resistance value R_2 is varied. The load current is 0.5 A and the resistance R_1 is fixed to 1.5 K ohm. The use of smaller resistors reduces the loss, even if the dV_d/dt of 4.9V/nsec is constant, and the measurement results tend to agree with the analysis results in Chapter IV. The loss is reduced by 14% by decreasing resistor R_2 and by 19% by increasing resistor R_1. The loss reduction due to resistor R_2 is roughly consistent with the simulation, and the loss reduction due to resistor R_1 is larger than in the simulation.



Symbol	Feedback	dV_d/dt goal [V/nsec]	R_1 [ohm]	R_2 [ohm]
	w/ FB	3	560	47
	w/o FB	-	680	Open
	w/ FB	3	680	47
	w/o FB	-	560	Open

Figure 3.21: Measured dV_d/dt with different resistance.

Table 3.6: Measurement result of the dV_d/dt and switching loss with different gate resistance R_1 and R_2.

I_L=3.5A

R_1 [ohm]	R_2 [ohm]	dV_d/dt[V/nsec]	Loss [uJ]
560	47	4.31	303
560	47	2.92	301

I_L=1.0A

R_1 [ohm]	R_2 [ohm]	dV_d/dt[V/nsec]	Loss [uJ]
560	47	2.85	201
680	47	2.95	163

I_L=0.5A

R_1 [ohm]	R_2 [ohm]	dV_d/dt[V/nsec]	Loss [uJ]
1500	10	4.97	52.9
1500	82	4.94	57.5
1500	150	4.93	61.5

The measured transient waveform of the start-up is shown in Figure 3.22. The V_g and V_d shown in Figure 3.22 are the gate and drain voltages of the low-side SJMOS. Figure 3.22 also shows the output voltage of the integrator V_{err}. In the absence of environmental fluctuations or changes in device characteristics, when the voltage of the integrator V_{err} reaches a constant value, it can be determined that the dV_d/dt is converged to the target value. The error voltage V_{err} is settled to a constant value in 7 switching cycles after the gate voltage is input, which can be used for applications operating at frequencies from several kHz to several tens of kHz.

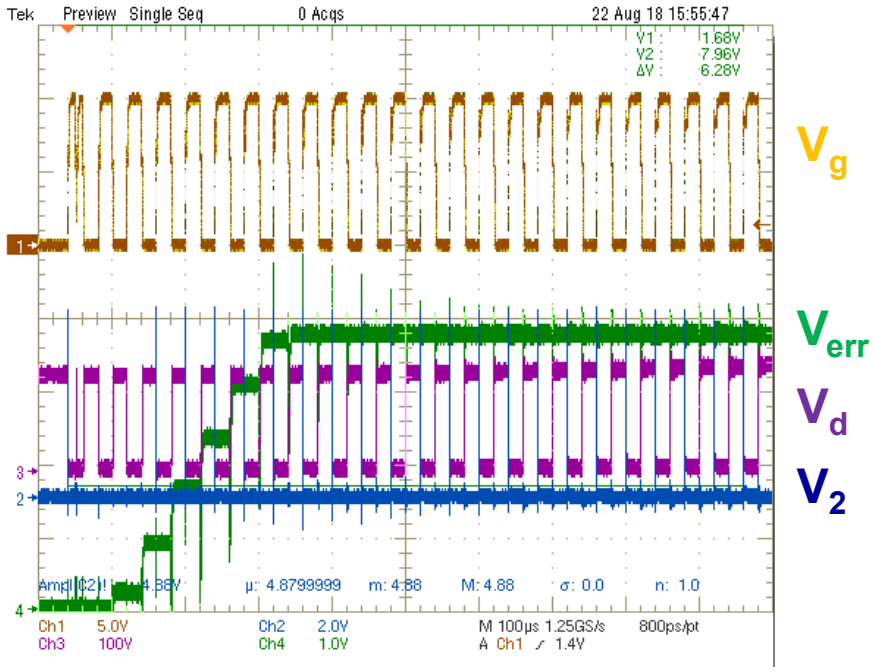


Figure 3.22: Measured transient waveform of the start-up.

Table 3.7 shows a performance comparison. The digital feedback scheme is adopted in [1] for power MOSFET but the SR of 0.0004V/nsec is slow. The digital and analog feedback technique is applied to IGBTs and GaN [4-7], and in particular, feedback technology applied to the GaN device [7] has succeeded in controlling dV_d/dt from 40 V/nsec to 4 V/nsec by integrating a 500 MHz amplifier in a CMOS. However, the output drive voltage of 4 V is low, and it cannot be adopted for SJMOS. In addition, the continuous-time analog feedback technique is not adopted to the SJMOS which the dV_d/dt depends on reverse recovery current I_{RR}. The discrete-analog feedback proposed in this work successfully controls the dV_d/dt of the SJMOS.

Table 3.7: Performance comparison of gate driver.

	TPE2015[1]	TPE2015[2]	TIA2017[15]	TPE2017[16]	ISPSD2019[3]	This work
Target dV_d/dt [V/nsec]	0.0004	2	5	1.3	40 to 4	4.5
Power device	Power MOSFET	IGBT	IGBT	IGBT	GaN	Superjunction MOSFET
Gate driver voltage	12	12	18	18	4	10
Feedback scheme	Digital	Continuous-time analog	Digital	Continuous-time analog	Continuous-time analog	Discrete-time analog
Iteration	20 (estimated)	1	2400	1	1	20
Chip integration	No	No	Driver Only	No	Driver with feedback circuit	Driver with feedback circuit
Process	NA	NA	0.18um BiCD	NA	0.18um CMOS	0.6um HV-CMOS* (18V)
Pro.	Precise control	Fast iteration	Precise control	Fast iteration	Fast iteration	Easy integration
Con.	Slow operation	High-speed opamp	Large iteration number	High-speed opamp	Low gate drive voltage	Reverse recovery dependence

*The chip was fabricated using the 0.13um 1.5V technology. However, Only 0.6um 5V transistor and 18V DMOS is used in the test chip

The chip micrograph is shown in Figure 3.23. The test chip was fabricated in 0.13 um 1.5 V HV CMOS process. However, only 0.6 um 5 V CMOS transistors and 18 V DMOS transistors are used in the test chip. The chip size is 2.87 mm x 2.87 mm.

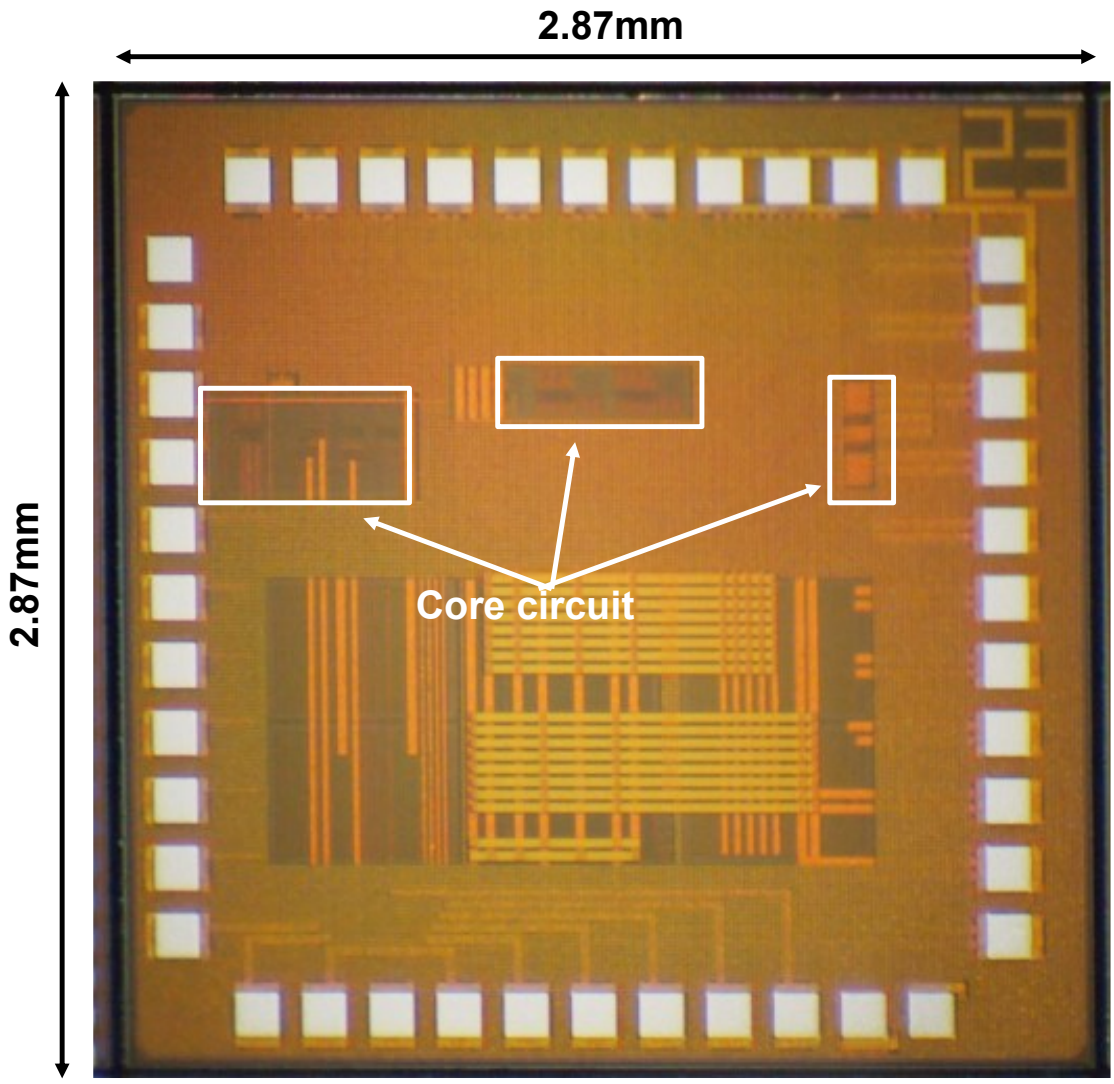


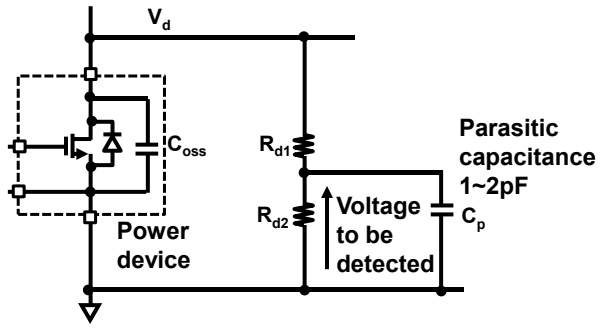
Figure 3.23: Chip micrograph

3.7 Applicability of the proposed analog FB driver IC proposed in chapter 3

This section describes the applicable scope of the discrete-time analog feedback proposed in Chapter 3. as mentioned in Chapter 1, the driver IC proposed in Chapter 3 is targeted at SJMOS used at low switching frequencies and low transducer power. The concept of discrete-time feedback can be applied to any converter as long as the switching frequency is lower than the op-amp bandwidth. From the above point of view, discrete-time analog feedback can be applied

to all converters shown in Figure 1.6. However, to apply discrete-time analog feedback, the slew rate of the drain voltage must be detected. The presence of parasitic capacitance causes difficult conditions for detecting the slew rate of the drain voltage, depending on the device type.

With the IC proposed in Chapter 3, capacitance is used for the voltage divider circuit.. A voltage divider circuit can also be formed using a resistor. Figure 3.24(a) shows the circuit diagram when a resistor is used. Figure 3.24(b) also shows the value of the capacitance C_{oss} of the power device. Furthermore, the value of the voltage divider resistor is shown. In Figure 3.24(b), the model number of the SJMOS is TK8A60W5. The resistance value shown in Figure 3.24(b) is the sum of the voltage divider resistors R_{d1} and R_{d2}. There is a substrate parasitic capacitance C_p at the drain node of the power device. The substrate parasitic capacitance C_p is 1pF to 2pF or more, even if the substrate design is sophisticated. The drain voltage (V_d) rise time in Figure 3.24(b) is calculated based on the definition that dV_d/dt is 5V/nsec, which is assumed in Chapter 3, and that dV_d/dt is the time for the drain voltage to go from 90% to 10% of the power stage voltage. The resistance value is determined so that the CR time constant, which is determined by the capacitance and resistance, is the same value as the V_d rise time. The resistance value is 25 kOhm. As a result, the power consumed by the resistor is 3.6 W. The lower limit of the switching frequency for household appliances, which is the application assumed for the driver IC in Chapter 3, is about 1 kHz. In addition, as shown in the measurement results in Chapters 2 and 3, the turn-on loss of the SJMOS is about 0.2mJ. Therefore, the switching loss per second is about 200 mW. The loss that would be generated in the voltage divider circuit is greater than 10 times the switching loss. For the above reasons, resistive voltage divider circuits cannot be used.



(a)

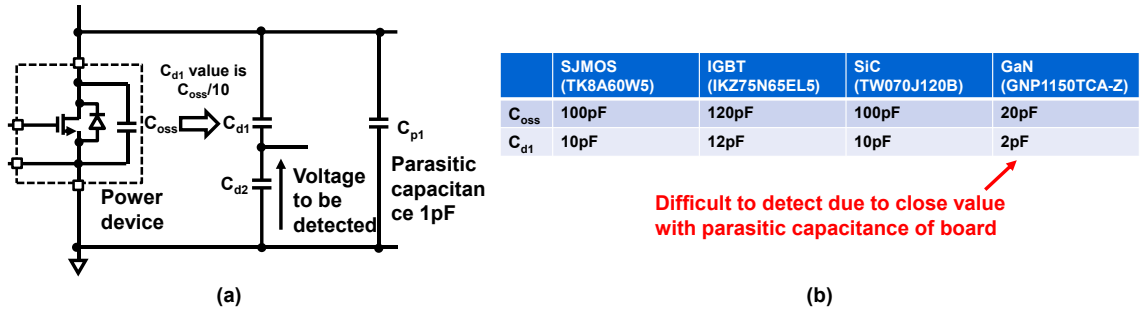
	SJMOS
V_d rise time [nsec]	44
Parasitic capacitance [pF]	2
Voltage of power stage [V]	280
Voltage divider resistance [kOhm]	25
Power consumption of resistance [W]	3.6

(b)

Figure 3.24: Voltage divider circuit with resistors and power consumption of the voltage

divider circuit

Next, discussion of the case in which capacitance is used in the voltage divider circuit is presented. Figure 3.25(a) shows a circuit for detecting the slew rate of drain voltage. The capacitance C_{oss} is the capacitance at the output of the power device. The capacitances C_{d1} and C_{d2} form a voltage divider circuit. Depending on the voltage divider ratio, the value of capacitance C_{d1} is about 1/100 of the value of capacitance C_{d2}. To avoid influence on the power stage circuit, the value of capacitance C_{d1} is designed to be less than one-tenth of the value of capacitance C_{oss}. There is also a board parasitic capacitance C_{p1} at the drain node of the power device. The parasitic capacitance C_{p1} of the board is more than 1pF even if the board design is more sophisticated. If the value of the voltage divider capacitance C_{d1} is close to the value of the parasitic capacitance C_{p1} of the board, the design of the voltage divider circuit becomes significantly more difficult.



	SJMOS (TK8A60W5)	IGBT (IKZ75N65EL5)	SiC (TW070J120B)	GaN (GNP1150TCA-Z)
C_{oss}	100pF	120pF	100pF	20pF
C_{d1}	10pF	12pF	10pF	2pF

Figure 3.25: The circuit schematic for detecting the slew rate of drain voltage and the values of capacitance C_{oss} for power devices of various materials.

Figure 3.25(b) shows the values of capacitance C_{oss} for power devices of various materials. In addition, the design values of the voltage divider capacitance C_{d1} are shown for each respective power device. In Figure 3.25(b), the model numbers of the power devices are: SJMOS is TK8A60W5 [68], IGBT is IKZ75N65EL5 [72], SiC-MOSFET is TW070J120B [73], GaN is GNP1150TCA-Z [74]. As shown in Figure 3.25(b), the capacitance of the GaN C_{oss} is as small as 20pF, resulting in a divided capacitance C_{d1} value of 2pF. The value of the capacitance C_{d1} is close to the value of the board parasitic capacitance C_{p1} (1pF), and the applicability of the analog feedback driver IC proposed in Chapter 3 to GaN is difficult because of the difficulty of

designing the voltage divider capacitance in GaN. The Figure 3.26 shows the range of possible applications of the driver IC proposed in Chapter 3, while the driver IC proposed in Chapter 3 is difficult to apply to GaN. However, the driver IC proposed in Chapter 3 can be applied to SiC-MOSFETs and IGBTs.

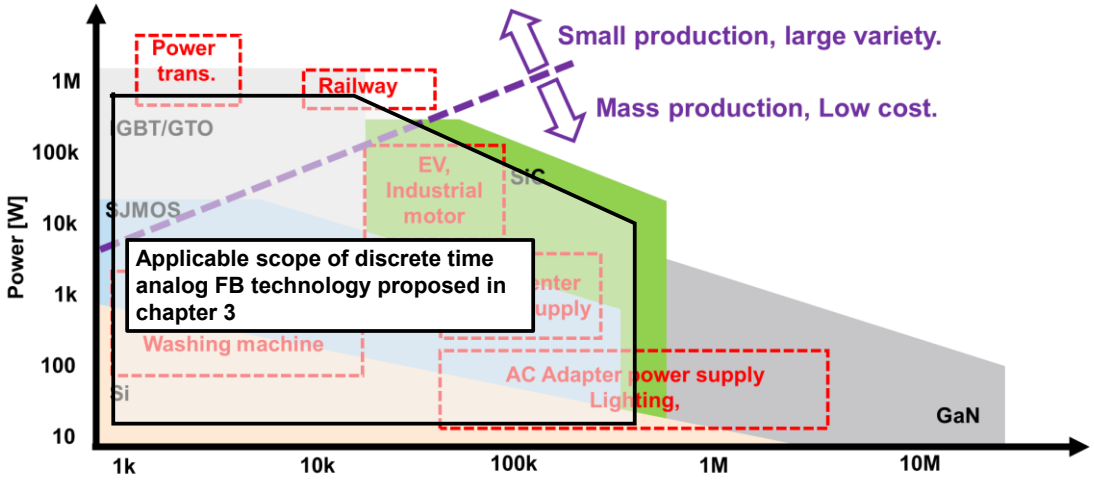


Figure 3.26: Applicable scope of discrete time analog FB technology proposed in chapter 3.

3.8 Summary of chapter 3

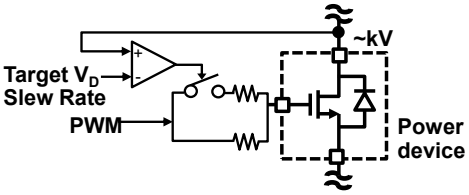
In this chapter, the active slew rate control gate driver is proposed for SJMOS. The proposed driver with discrete-time feedback technology controls the dV_d/dt of SJMOS by changing the two resistors. The proposed feedback applies feedback results to the next switching, which results in I_{RR} dependent dV_d/dt at constant value regardless of load current, temperature and threshold voltage variation. The switching loss is reduced by choosing the appropriate values of the two resistors. The driver is integrated in 0.6um CMOS technology and the measured dV_d/dt is kept constant regardless of changes in the load current or temperature. The turn-on delay reduction of 74% and switching loss reduction of 25% are achieved by proposed feedback technique.

Chapter 4 Digital feedforward active gate drive for SiC-MOSFETs

4.1 Introduction

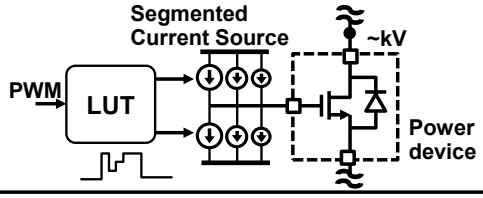
This chapter describes active gate driver ICs using digital feed-forward technology. The target device is a SiC-MOSFET. The target device is a converter that handles power such as used in electric vehicles. SiC-MOSFET allows high power density and compact system implementations, but the following three challenges manifest: 1. Large radiation noise and conduction noise caused by voltage surge and successive ringing in combination with the high-voltage slew rate, 2. Device performance degradation and failure owing to the repetitive application of surge voltage, and 3. Degradation of overcurrent tolerance for short-circuit faults. EMI and reliability degradations are critically important for power electronics in public environments for which reliability is essential.

The active gate drive technique shown in Figure 4.1 is one of the solutions for the 1st challenge, but the analog control scheme shown in Figure 4.1(a) is less effective owing to the limited arbitrariness of the gate drive waveform [66]. For example, reference [66] can only control dv_d/dt due to reverse recover current (I_{RR}) of SuperJunction MOSFETs and cannot control current or voltage ringing. In addition, the analog feedback for faster control increases costs. Reference [24] controls an IGBT dv_d/dt of 2 V/nsec and Reference [26] [27] controls the rising current waveform of SiC-MOSFETs connected in parallel by feedback. However, a 14 V 320 MHz wideband operational amplifier is required in [26] and 220MHz wideband operational amplifier with output voltage range of 20V is required in [27], making chip integration difficult, which is required for applications such as EV motors. The implementation in a discrete configuration also increases area and cost. The gate driver [29] for GaN devices is successfully integrated with 4 V 500 MHz bandwidth operational amplifiers in a CMOS to control dv_d/dt with feedback. However, this technology cannot be applied to SiC-MOSFETs because the gate voltage of 4 V required to drive GaN is lower than the 18-25 V required for SiC-MOSFETs.



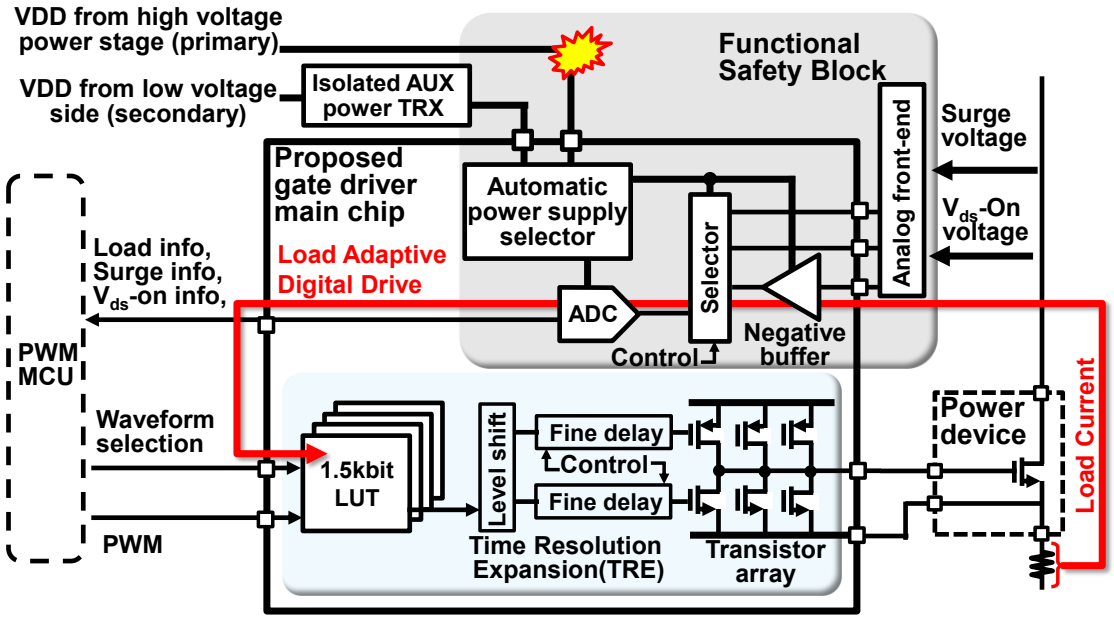
☺Feedback optimization
☹Less degree of drive waveform optimization

(a) Conventional analog active gate driver



☺Fine grain waveform optimization
☹Fixed waveform, limited CLK freq. (High voltage CMOS)

(b) Conventional digital gate driver



☺Fine Grain Waveform Optimization
☺Adaptive waveform by LUT switching
☺Clock frequency reduction by Time Resolution Expansion

(c) Proposed Load Adaptive Digital Gate Driver IC w/ Functional Safety Feature

Figure 4.1: Conventional driver and proposed digital feed forward active gate driver.

The digital gate drive shown in Figure 4.1(b) is an attractive solution [42] [44] [46] [43] [39] [47] [48], because arbitrary control of gate voltage can regulate various power device characteristics such as dv_d/dt, di_d/dt, and current-voltage ringing. However the on-chip implementation with a single waveform Look Up Table (LUT) [42] was insufficient for the motor drive applications in which the load current varies in the order of sub-1 ms [29]. Even another FPGA-based digital implementation has not demonstrated real-time load current tracking [44]. An example of load application is given in reference [46], However an external measuring instrument is used to detect the load and output digital data to the gate driver IC.

The second and third problems related to device degradation can be solved by an external controller in the case of IGBTs because of their relatively slow operation. However, SiC-MOSFETs are more sensitive to short circuits that cause thermal breakdown because the current density of the chip is higher than that of IGBTs, requiring a gate driver IC to complete fast detection and protection.

This paper proposes a load-adaptive gate driver IC that solves issues related to surge voltage-induced noise and device gradients [75]. In this paper, theoretical analysis, simulation, and measurements are comprehensively performed to generate optimal waveforms for turn-off voltage surge reduction. The theoretical analysis and simulation of turn-off considering capacitor nonlinearity, which has not been done before, is performed. The gate waveform that reduces surge voltage is derived from theoretical analysis and simulation. The optimal waveforms are generated by measurements using the results of simulation and theoretical analysis. The proposed chip is fabricated and the optimum waveform is supplied to the power device. The switching that breaks the tradeoff between surge voltage and losses is demonstrated experimentally using SiC-MOSFETs as the power device. The proposed load adaptive digital gate driver is shown in in Figure 4.1(c). The IC implements the 3-bit segmented current sources, each consisting of a transistor array, to pull-up and pull-down the gate, the 1.5 kb LUT to store multiple gate drive patterns, the assisting schemes to expand the time resolution of the gate current and reduce the LUT size, and the multipurpose 500 ksps Successive Approximation Register (SAR) ADC whose concept is shown in reference [17], an isolated power supply and automatic power supply (VDD) selector is also implemented. The load adaptive digital gate

driver was monolithically integrated for the first time ever, making it possible to break the trade-off between surge/ringing noise and switching loss of SiC-MOSFETs for a wide variety of load varying applications.

The remainder of this paper is organized as follows. In Section II, the optimal gate current pattern is derived by performing a turn-off voltage ringing analysis that takes into account the non-linearity of parasitic capacitance. Section III describes the driver circuit to output the derived optimal gate current pattern with less memory. Section IV presents the sampling front-end circuit for detecting surge voltage, on-voltage, and drain current. The isolated power supply circuit is also shown in Section IV. The measurement result is shown in Section V. Section VI concludes the paper.

4.2 Turn-off voltage ringing analysis

In this section, the optimal gate current pattern is derived by performing a turn-off voltage ringing analysis that takes into account the non-linearity of parasitic capacitance. First, it is explained what is different from the conventional switching waveforms [19] [76] when capacitor nonlinearities of the SiC-MOSFETs are taken into account. Next, an analysis of turn-off voltage ringing considering capacitor nonlinearity and gate current waveforms that reduce ringing are shown. Figure 4.2 shows the equivalent circuit of the power device and power stage. Figure 4.3 shows what is different from the conventional switching waveforms [19] [76] by considering the nonlinearity of the capacitor. Figure 4.3(a) shows simulation results of turn-off using the circuit in Figure 4.2. Figure 4.3(b) is an enlarged view of a portion of Figure 4.3(a). The simulator is Cadence Spectre and the device is TW070J120B [12]. For simplicity of discussion, the inductance L_d is set to 0. The dotted line in Figure 4.3(a) and Figure 4.3(b) shows the result when the nonlinearity of the capacitor is not considered, and the solid line shows the result when the nonlinearity of the capacitance is considered. As shown in Figure 4.3(a), when nonlinearities in capacitance are not considered, the gate voltage does not change because the capacitance C_{gd} increases due to the Miller effect from time t_1 to t_2, when the drain voltage increases [18,19]. On the other hand, considering the nonlinearity of capacitance, as shown in Figure 4.3(b), the period during which the gate voltage does not change due to the

Miller effect begins at time t_3 and ends at time t_4. From time t_4 to t_5, the drain voltage rises sharply and the gate voltage also decreases due to the capacitance nonlinearity.

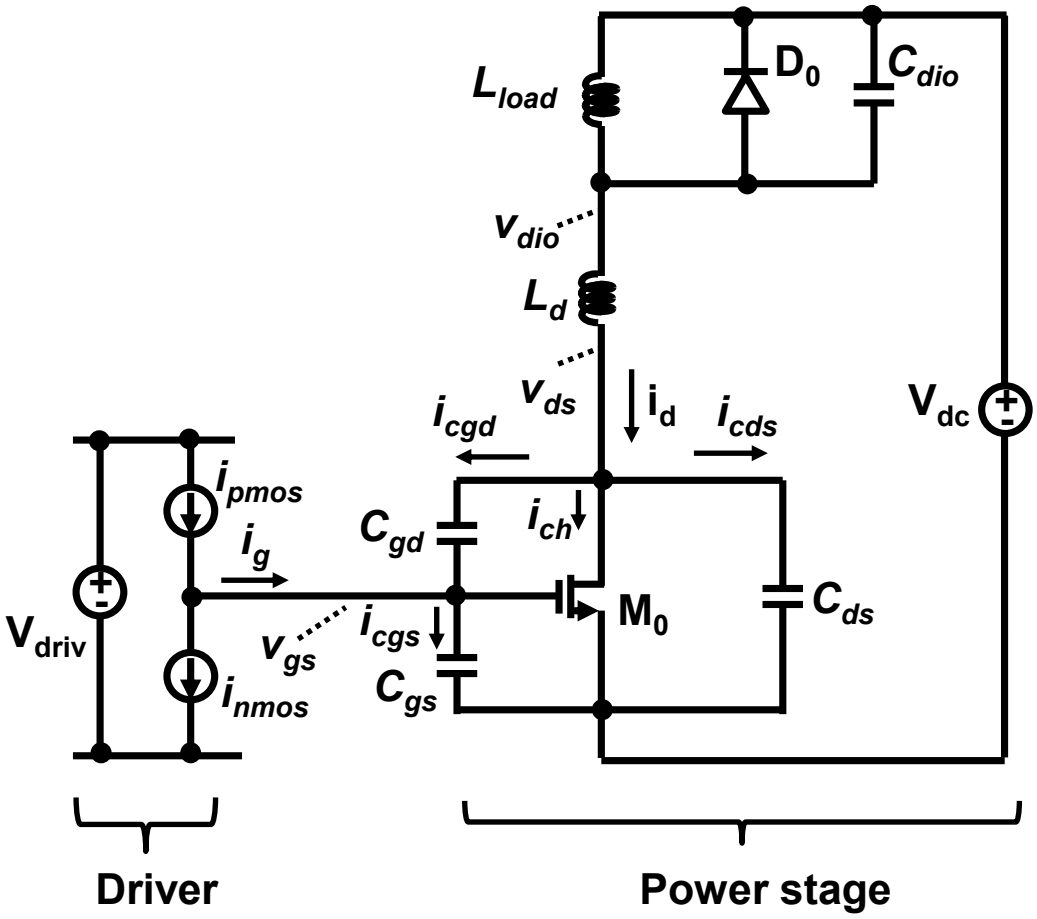


Figure 4.2: The equivalent circuit of the power device and power stage.

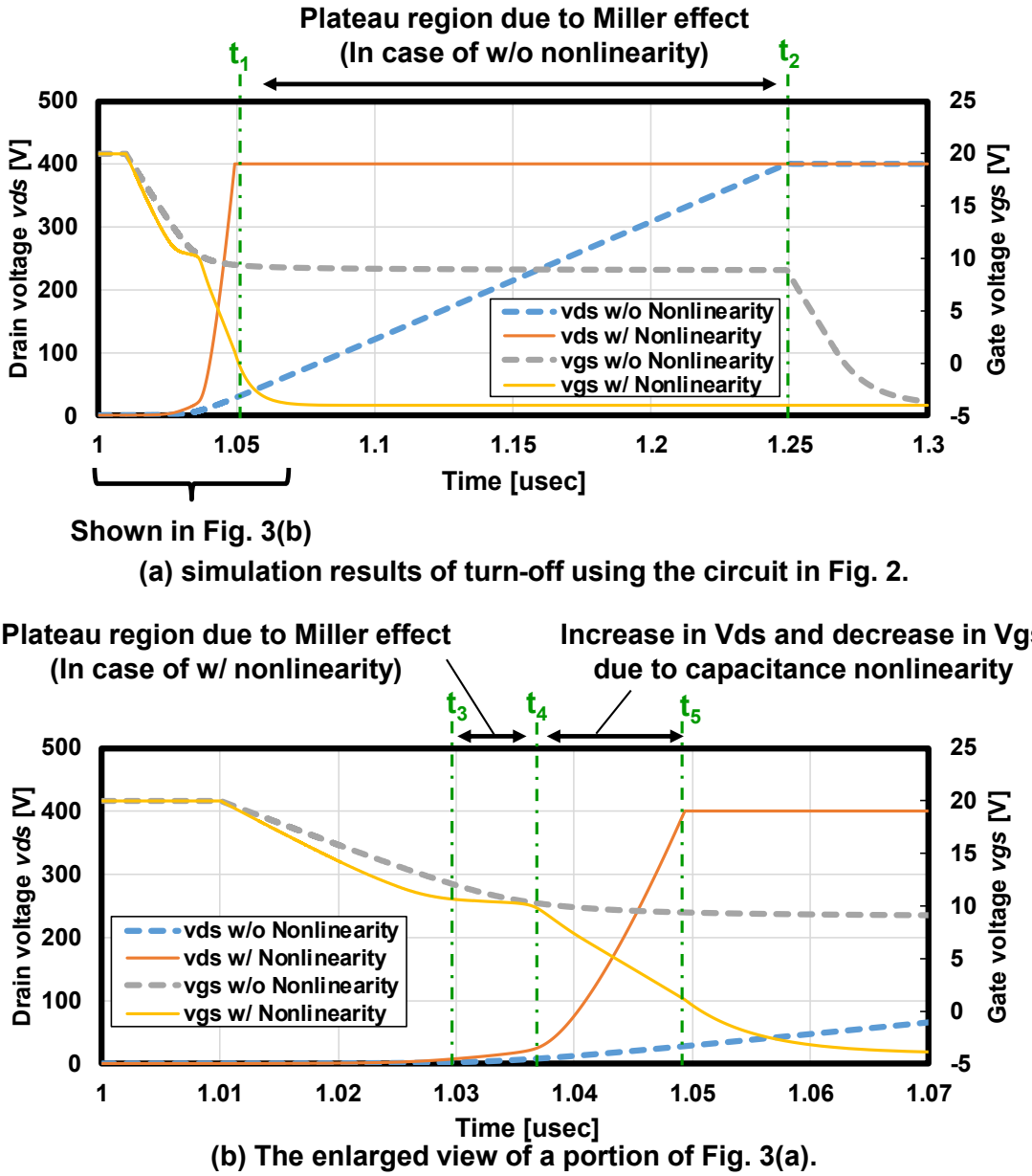


Figure 4.3: Simulation results of turn-off waveforms with and without consideration of capacitor nonlinearity.

The analysis of turn-off voltage ringing also needs to take into account the rapid increase in drain voltage and decrease in gate voltage due to capacitance nonlinearity.

The following is an analysis of turn-off voltage ringing and identification of gate waveforms that reduce ringing, taking into account the nonlinearities described above. Figure 4.4 shows the

simulation results using the circuit in Figure 4.2 when the inductance L_d is set to 10 nH. The currents i_g, i_d, i_{ch}, and i_{cds} are the gate current, drain current, channel current, and parasitic drain-source capacitance current, respectively. The voltages v_{ds}, v_{dio}, and v_{gs} are the drain and gate voltages of transistor M_0 and the anode voltage of diode D_0, respectively. The g(Abs) in Figure 4.4 is an absolute value of gain defined by dv_{ds}/dv_{gs}. In Figure 4.4, C_{ds}, C_{gd}, and C_{ds} show the time variation of capacitance, where $(1+g)C_{gd}$ is the gate-to-drain capacitance that takes into account the Miller effect.

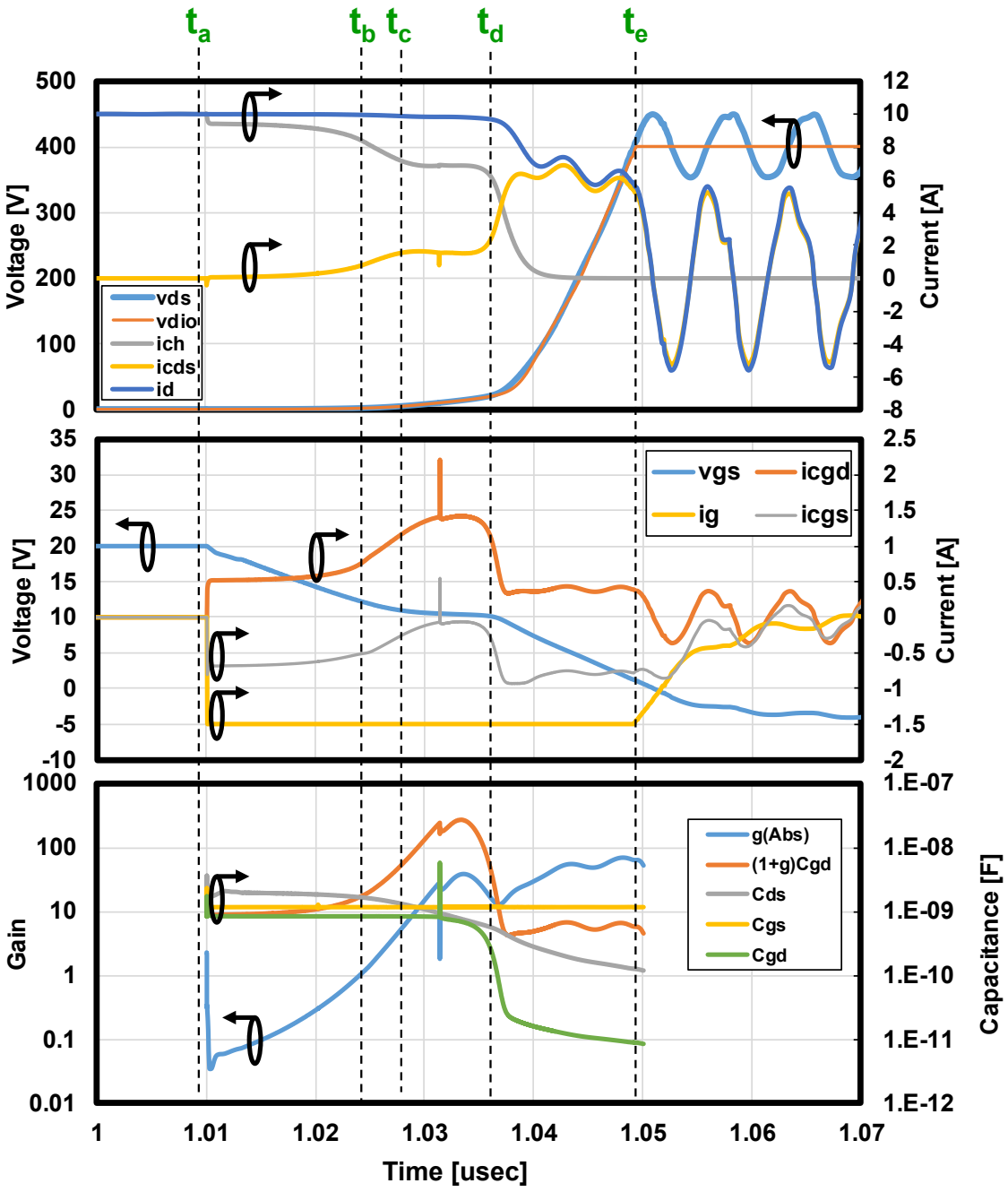


Figure 4.4: Simulation results with nonlinearity of capacitors are considered and parasitic inductance is included.

The turn-off operation is described below with reference to Figure 4.4. It is briefly described up to the beginning of the Miller plateau region, which is described in other literature [18,19], and then the subsequent characteristics are explained in detail. The gate current i_g begins to flow

from time t_a, at time t_b the power device M_0 transitions from the inter-tripolar region to the saturation region, and at time t_c the Miller plateau region begins [18,19]. In the Miller plateau region, the capacitance $(1+C_{gd})$, which takes into account the miller effect, becomes much larger than the capacitance C_{gs}, and most of the gate current i_g flows through the capacitance C_{ds}. From time t_c to t_d, the drain voltage v_{ds} slowly increases. The capacitance C_{gd} of SiC-MOSFET has a drain voltage dependence, and as the drain voltage increases, the capacitance C_{gd} rapidly decreases [73]. Then, at time t_d, the capacitance C_{gs} becomes larger than the capacitance $(1+g)C_{gd}$, even considering the Miller effect. The gate current i_g starts to flow into the capacitance C_{gs}, and the gate voltage v_{gs} decreases. Even if the drain voltage does not reach the power supply voltage V_{dc} of the power stage, the miller plateau region ends at time t_d. As the gate voltage v_{gs} decreases, the channel current i_{ch} decreases and the current flowing in the capacitance C_{ds} increases.

When the gate voltage v_{gs} reaches the threshold voltage, the channel current i_{ch} becomes almost zero, and most of the current i_d flows into the capacitance C_{ds}. Since the capacitance C_{ds} also decreases with increasing drain voltage v_{ds} [73], the drain voltage v_{ds} and the diode voltage v_{dio} increase rapidly. At time t_e, diode D_0 begins to conduct. Here, a resonant circuit is formed and ringing occurs in the drain voltage v_{ds}. Figure 4.5 shows simulation results magnified around time t_e and the equivalent circuit at time t_e. Since capacitance C_{gd} is an order of magnitude smaller than C_{ds} at time t_e as shown in Figure 4.4, the capacitance C_{gd} is ignored in Figure 4.5 to simplify the discussion. In the equivalent circuit shown in Figure 4.5, the drain voltage v_{ds} is $v_{ds}(t)$, and furthermore, the current source i_{ch} becomes almost zero at time t_e, so the following equation is obtained. Time t_e in Figure 4.5 corresponds to $t = 0$ in Eq. (4.1) to (4.3).

$$C_{ds}\frac{d^2v_{ds}(t)}{dt^2} - \frac{V_{dc} - v_{ds}(t)}{L_d} = 0 \tag{4.1}$$

$$v_{ds}(0) = V_0 \tag{4.2}$$

$$\frac{dv_{ds}(0)}{dt} = \frac{I_0}{C_{ds}} \tag{4.3}$$

The initial values of the drain voltage v_{ds} and the current in the capacitance C_{ds} are V_0 and I_0,

as shown in Figure 4.5. The drain voltage v_{ds} is expressed by the following equation.

$$v_{ds}(\mathrm{t}) = \sqrt{(\mathrm{V}_0 - V_{dc})^2 + \left(\frac{\mathrm{I}_0}{C_{ds}\omega}\right)^2}\sin(\omega t + \varphi) + \mathrm{V}_{\mathrm{dc}} \tag{4.4}$$

$$\omega = 1/2\pi\sqrt{L_d C_{ds}} \tag{4.5}$$

From Eq. (4.4), it can be seen that to reduce the amplitude of the resonance voltage, the initial current I_0 of the capacitance C_{ds} should be reduced.

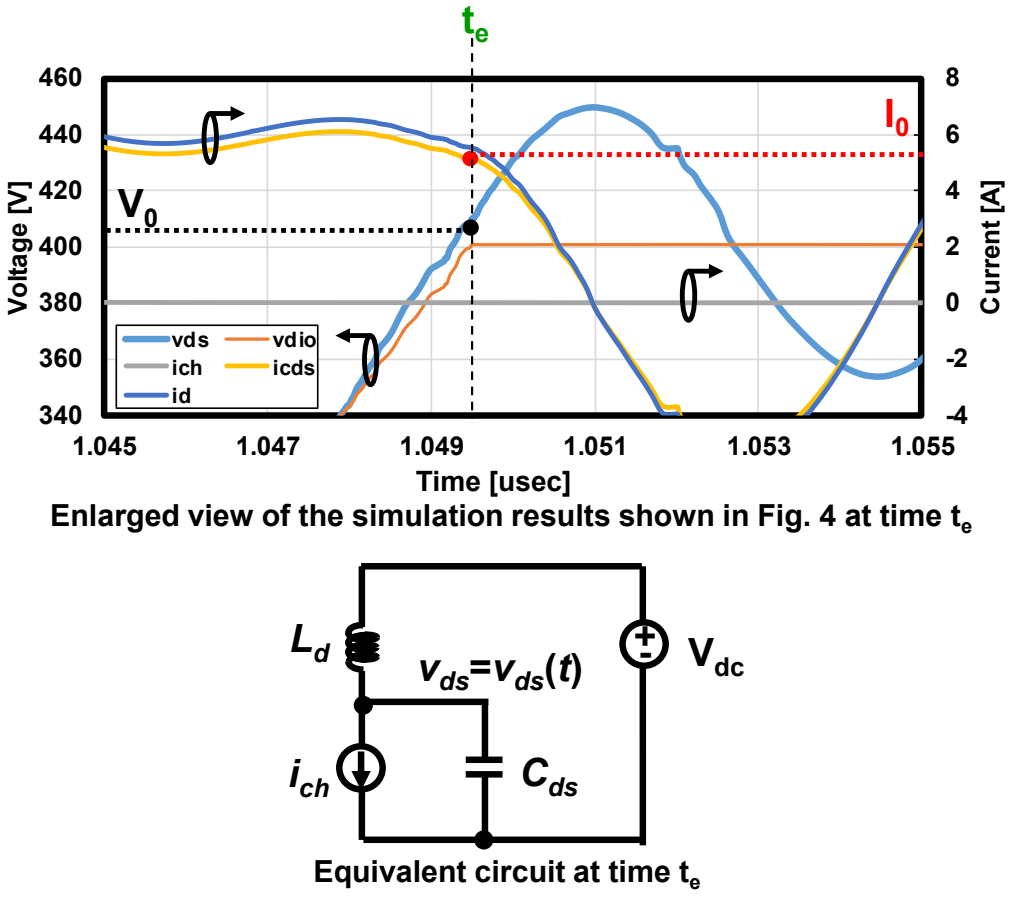


Figure 4.5: The outlines of the channel current i_{ch}, drain current i_d, and current flowing in the capacitance C_{ds}

Figure 4.6 shows the outlines of the channel current i_{ch}, drain current i_d, and current flowing in

the capacitance C_{ds}. The left figure in Figure 4.6 shows the waveform without current i_{ch} control, while the right figure shows an example with current i_{ch} control. To reduce the initial value current I_0, the channel current i_{ch} should be increased, as shown in Figure 4.6. This can be accomplished by temporarily flowing the gate current i_g in the opposite direction and increasing the gate voltage v_{gs} above the threshold voltage. The following describes how the gate current i_g is controlled to control the channel current i_{ch}. The requirement to control the gate current i_g prior to time t_e in order to control the channel current is illustrated in Figure 4.7. The simulation results showing an example of uncontrolled channel current i_{ch} are shown in Figure 4.7(a). Figure 4.7(b) shows an example where the channel current i_{ch} is controllable. Figure 4.7(b) also shows that the surge voltage has been successfully reduced. As shown in Figure 4.7(a), even if the gate current i_g flows in the opposite direction just before time t_e when resonance begins, the current i_{cds} flowing through the capacitance C_{ds} cannot be reduced. This is because the gate voltage v_{gs} is much lower than the threshold voltage just before resonance starts. Therefore, the gate current i_g shown in Figure 4.7(b) is desirable. By flowing the gate current i_g in the reverse direction around the point where the gate voltage v_{gs} falls below the threshold voltage, holding the gate voltage at a value slightly below the threshold voltage, the channel current i_{ch} can be changed and the initial value current in the capacitance can be reduced.

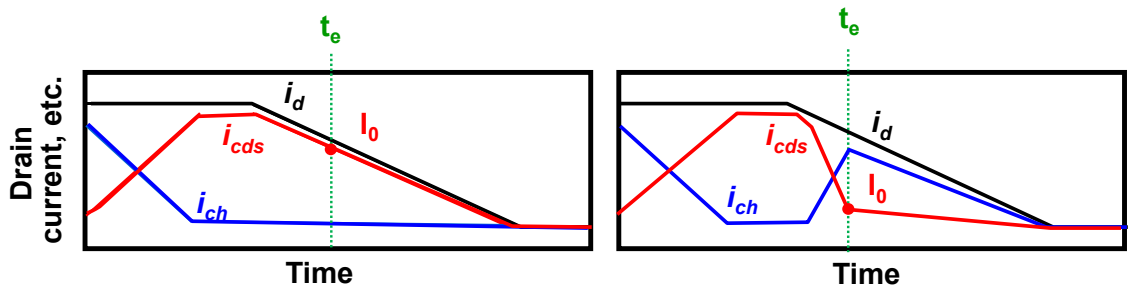
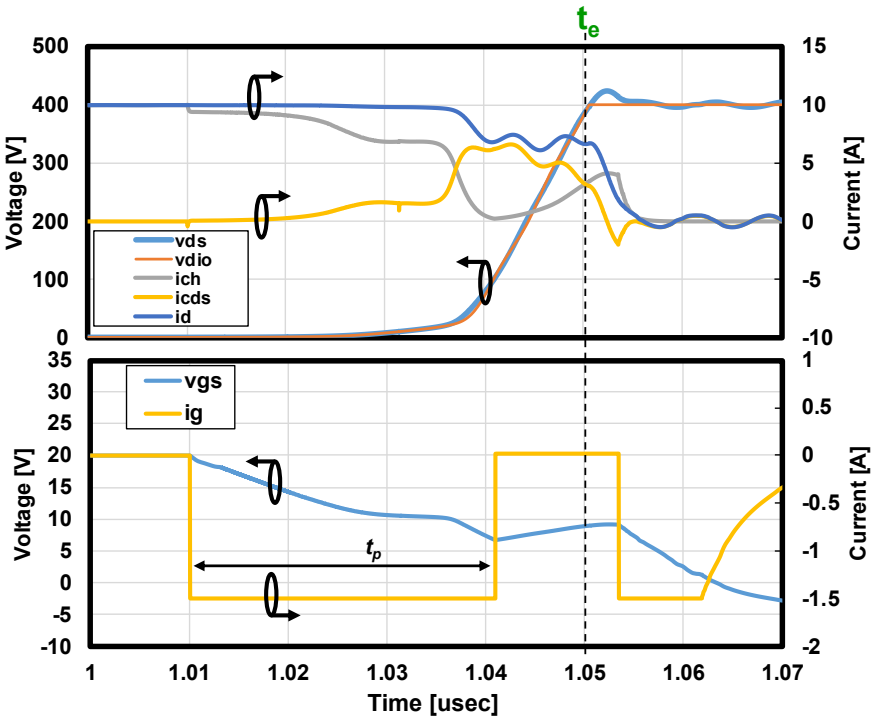
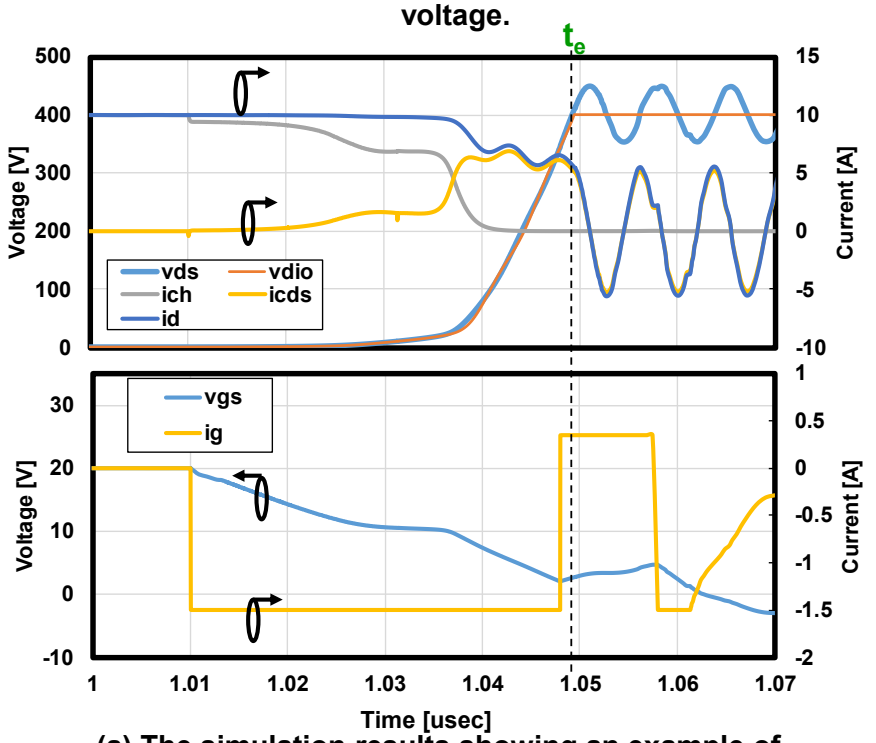


Figure 4.6: The outlines of the channel current i_{ch}, drain current i_d, and current flowing in the capacitance C_{ds}



(b) The simulation example of controllable channel currents, showing successful reduction of surge voltage.



(a) The simulation results showing an example of uncontrolled channel current

Figure 4.7: Simulation results with controlled channel current and reduced ringing, and simulation results with uncontrolled channel current.

4.3 Proposed gate driver design with time expansion technique

As described in Section II, a gate waveform signal is required to drive the gate current i_g in the opposite direction. The relationship between the time t_p in Figure 4.7 and the maximum surge voltage is shown in Figure 4.8. The t_p is the time when the gate current begins to flow in the reverse direction. The surge voltage shows the difference between the drain voltage and the main circuit dc voltage of 400V. The time t_p is set to 31 nsec in the simulation shown in Figure 4.7. As shown in Figure 4.8, when t_p changes by 1 nsec, the surge voltage changes significantly. Therefore, controlling t_p by 1 nsec is necessary.

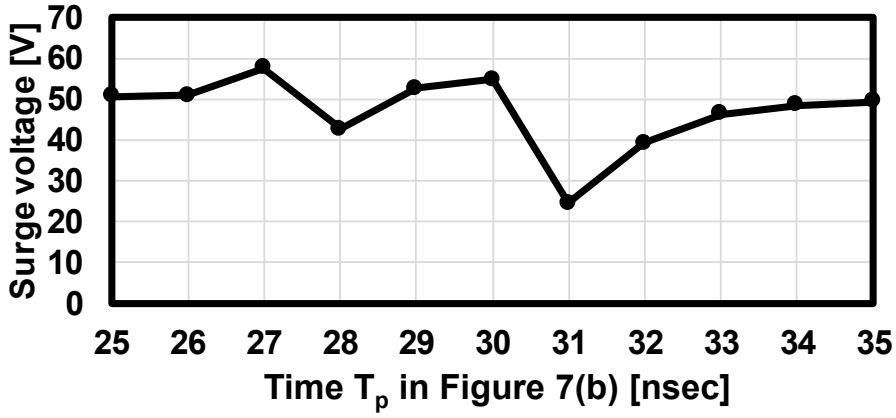


Figure 4.8: Simulation results of the relationship between the time T_p, when the gate current starts to flow in the reverse direction, and the surge voltage.

Figure 4.9 shows the proposed gate driver with Time Resolution Expansion (TRE). A 1 GHz clock is necessary to control 1 nsec in a digital circuit. Generating the 1 GHz clock in the low-cost High Voltage CMOS process for gate drivers is not feasible in terms of area, power consumption and skew. As shown in Figure 4.9, the time resolution expansion (TRE) scheme proposed here introduces fine tunable delay circuits between the level shifter (LS) and the output stage. The fine delay is adjusted in a circuit with a current source connected between the

PMOS or NMOS of the inverter and the power supply, as shown at upper left in Figure 4.9. The fine delay circuit is enabled after the first falling edge of the PWM signal. The time t_p can be controlled in 1 nsec increments by TRE. The output stage shown in Figure 4.9 can output current fast for a time resolution of 1 nsec, which has been confirmed by simulations that take parasitic resistance and parasitic capacitance into account. If the value of parasitic inductance between the power device and the gate driver becomes large, ringing may occur in the gate current and the intended active gate waveform may not be input to the power device. The inductance of the parasitic gate loop should be minimized by using TO247-4L with a Kelvin Source provided in the power device package.

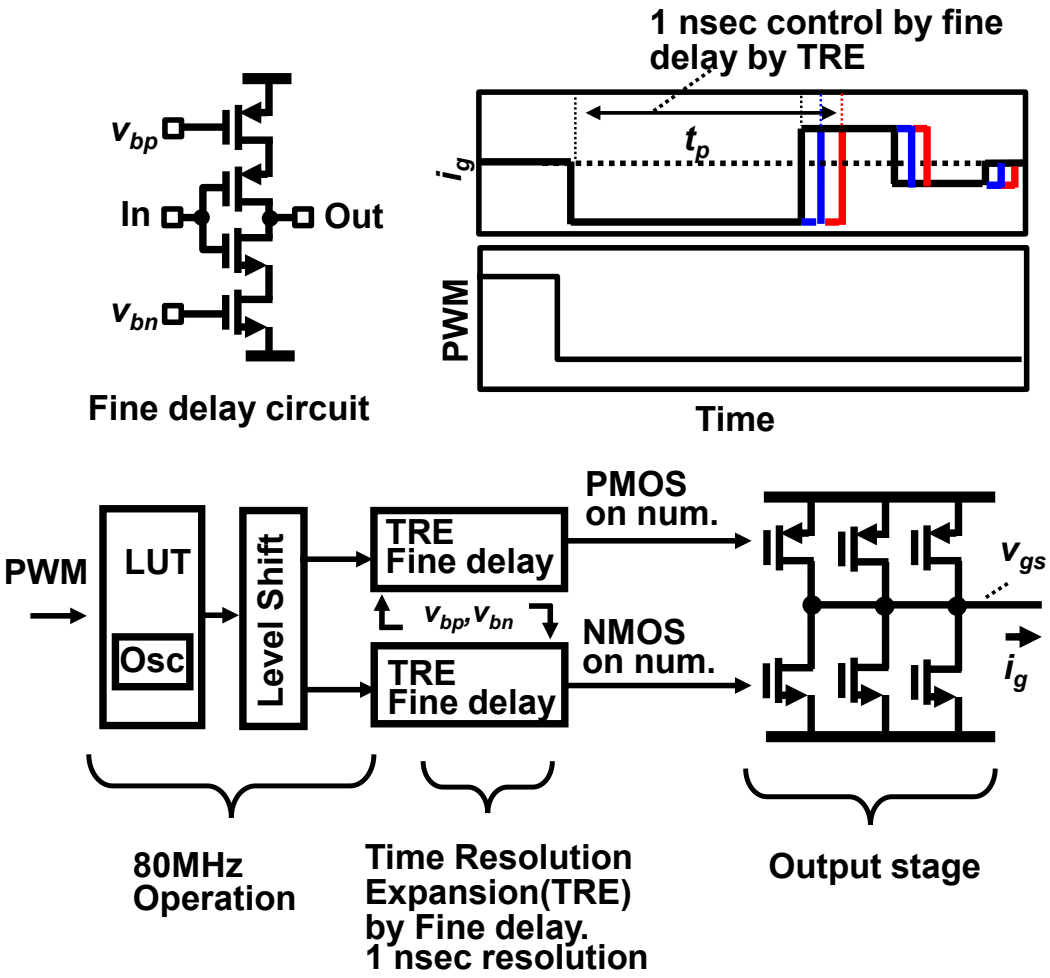


Figure 4.9: The proposed gate driver with Time Resolution Expansion (TRE).

The TRE scheme also keeps the clock frequency of the LUT at 80 MHz and LUT is significantly reduced in size by using TRE. The effect of the LUT on compactness is shown in Figure 4.10. The current profile specifications are shown at the top of Figure 4.10. The specification of the LUT includes the ability to store 6 bits (3 NMOS and 3 PMOS bits) of i_g amplitude information with a resolution of 1 nsec. The total control interval is 375 nsec. As shown at lower left in Figure 4.10, if a conventional DAC [44] is used without the proposed TRE technique, data in 1 nsec increments is required, resulting in a total LUT size of 18 kbit. On the other hand, when using TRE, 12.5 nsec segment data is sufficient. The time of one segment, 12.5 nsec, is controlled using fine delay at 1 nsec intervals. With 3 bits, 12.5 nsec can be adjusted in less than 1 nsec. Even considering the additional 3 bits needed for TRE, the total LUT size is reduced to 1.5 k. Figure 4.11 shows the time resolution and the required LUT size. When using a conventional 1 GS/s DAC, the smaller the required t_p resolution, the larger the LUT size. On the other hand, when TRE is used, the increase in the required LUT size can be suppressed. By using TRE, the required LUT size can be reduced to 1/12 of that using a conventional DAC. The LUT size of 3 kbits or less can be integrated into a CMOS process using digital circuits.

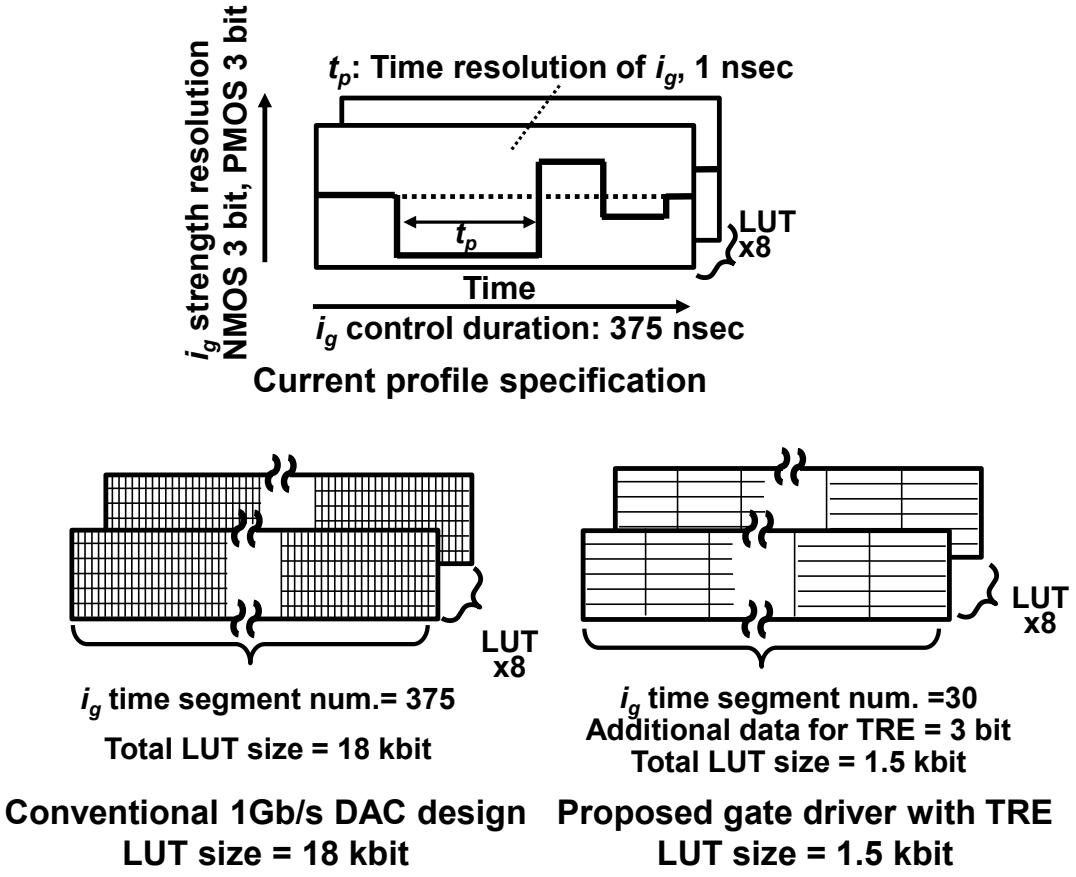


Figure 4.10: LUT size specifications and comparison of LUT size with and without TRE.

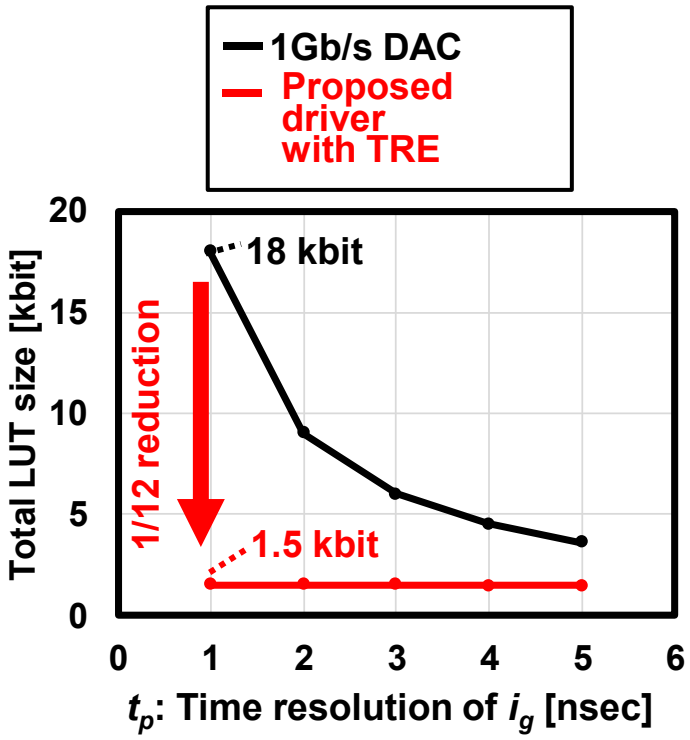


Figure 4.11: The relationship of the time resolution and the required LUT size.

In the gate driver IC used in this study, NMOS and PMOS may conduct simultaneously for a very short time, causing a large current to flow. To prevent the wiring in the IC from being disconnected due to the large current, the PMOS and NMOS in the IC are connected with thick wiring.

4.4 Design of proposed sampling front-end and isolated power supply

This section describes the circuit configuration of the sampling front-end and isolated power supply. By sensing the load current of the SiC-MOSFET, the LUT can be switched as a signal indicating the load status. The V_{ds}-on voltage can be used for short-circuit detection. By monitoring the surge voltage, information on the overvoltage applied to the SiC-MOSFET can be obtained and used to determine reliability. Isolated power transmission was also included to achieve functional safety, a concept presented in the literature [77]. The on-chip ADC, selector

and buffer circuits can be powered via isolated power transmission.

A. Load Current Sensing

Figure 4.12 shows the schematics of sampling front-end (FE) for the load current sensing, the surge monitoring, and the V_{ds}-on (short-circuit) monitoring with the integrated 500 ksps SAR ADC. The load current is detected by the resistor R_{sense} introduced in the source terminal of the low-side SiC-MOSFET, but both the positive and the negative voltages appear on v_{Rsense} because of the current commutation. To sense both of them, an inverting amplifier is integrated on the chip and the offset voltage v_{ref} is applied. The sample timing of the ADC is set to 4 us past the SiC voltage transient (steady sampling) so as to be unaffected by the switching noise of the 400 V power stage.

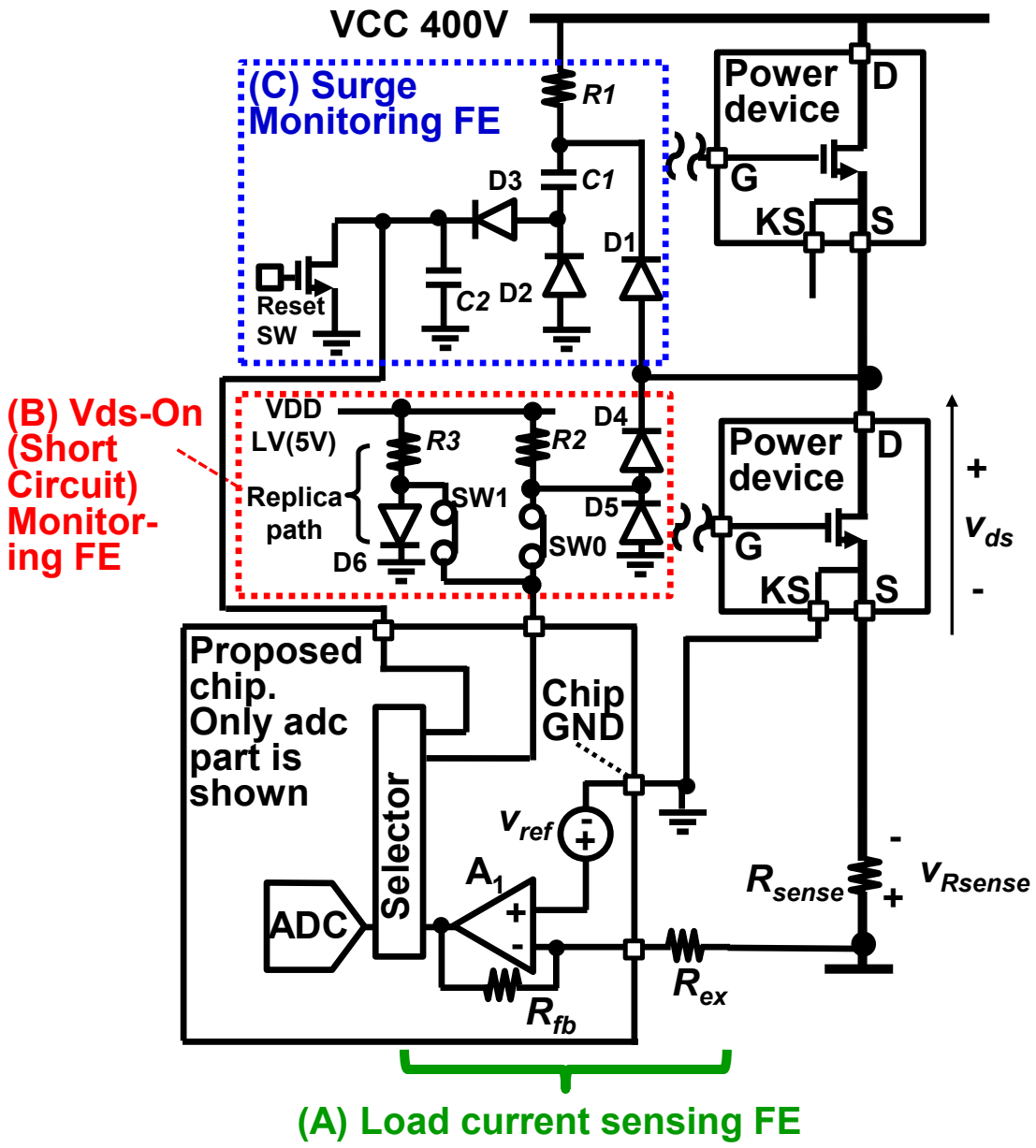


Figure 4.12: Surge monitoring circuit, Vds-on monitoring circuit, load current detection circuit.

B. Surge Monitoring

To detect the surge voltage, a peak hold surge sampling frontend composed of the off-chip high-voltage diode, dividing sample capacitors, and the reset switch was also implemented as a surge monitoring FE, as shown in Figure 4.12. In the initial state, resistor R_1 biases the voltage

on the cathode of D_1 to VCC of 400 V. When a surge occurs in the drain voltage of a low-side power device and the voltage becomes greater than 400 V, the cathode side of diode D_1 becomes equal to the surge voltage. The surge voltage larger than 400 V is divided by capacitors C_1 and C_2 to match the 5 V ADC input inside the chip. Diodes D_2 and D_3 are located to provide the current path when capacitors C_1 and C_2 are discharged by the reset switch. The detected surge voltage can be used to predict device performance degradation or failure due to repeated application of surge voltage.

C. Vds-On (short-circuit) Monitoring

On-state V_{ds} (V_{ds}-on) is also observed to detect the short-circuit fault. Figure 4.12 also shows the V_{ds}-on (short-circuit) monitoring front end. The Resistor R_2 biases the cathode of diode D_5 to 5 V. When the low-side power device turns on, the drain voltage v_{ds} of the power device is lower than 5 V. Then diode D_4 turns on and the anode of diode D_4 is the same as the drain voltage of the power device. Diode D_4 turns off when the low-side power device turns off and the ADC input voltage never exceeds 5V. With the proposed circuit, the on-voltage of diode D_4 is added to the V_{ds}-on voltage. Therefore, a replica circuit consisting of resistor R_3 and diode D_6 is prepared. By measuring the difference between the voltage at the anode of diode D_6 and the voltage at the anode of diode D_4, the effect of the on-voltage of the diode can be eliminated.

D. Isolated Power Supply

As shown in Figure 4.13, the receiver for the auxiliary isolated power transfer and the automatic VDD selector for the ADC and sensing frontend are integrated for functional safety. Power supply of the gate driver IC is typically provided from the VCC in the high-voltage domain through a step-down converter. But in terms of functional safety, the monitoring circuits should keep operating for diagnosis and safe system shutdown in case faults, including short circuit, occur in the high-voltage domain and the power supply is lost. Isolated power transfer is realized over a differential transformer implemented by a cost- and power-efficient Fan Out Wafer Level Package (FOWLP) process [77]. The automatic VDD selector consists of two diodes and outputs to the ADC whichever is the higher of the voltage generated from the high-voltage domain and the voltage transmitted wirelessly.

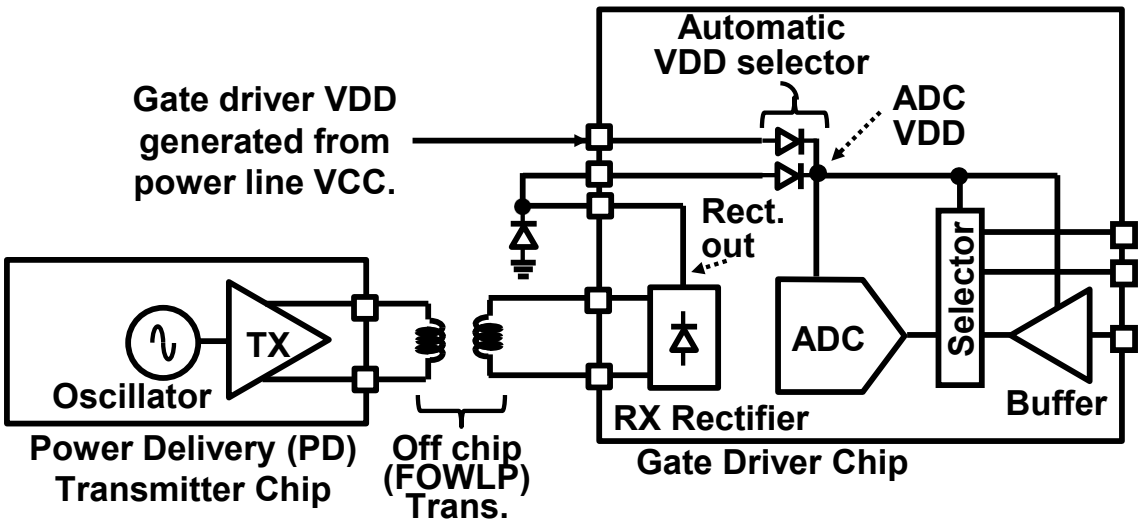


Figure 4.13: Isolated power supply circuits.

4.5 Timing of ADC operation to detect power device information

Power devices generate large noise during switching. If noise is generated at the timing of ADC operation, the ADC will not operate properly. The timing of ADC operation and the driver circuit for detecting the load state of a power device are shown in the Figure 4.14. Figure 4.14(a) shows the timing of ADC operation and Figure 4.14(b) shows the driver circuit for detecting the load state of a power device. In the figure, PWM is a signal that indicates the on/off state command of the power device, I_g is the gate current output by the driver, V_{Rsense} is the voltage generated across a resistor placed at the source of the power device to detect the drain current of the power device, and ADC conversion enable is a signal that indicates when to start AD conversion. As shown in the Figure 4.14, the rising or falling edge of the PWM signal generates large noise, so ADC operation at this timing should be avoided. After a short time has elapsed after the PWM signal rises and the noise disappears, the ADC starts conversion. The gate current I_g output at the next switching is determined based on the AD conversion result of the previous switching. This operation sequence allows AD conversion of the load current information avoiding the switching noise of the power device.

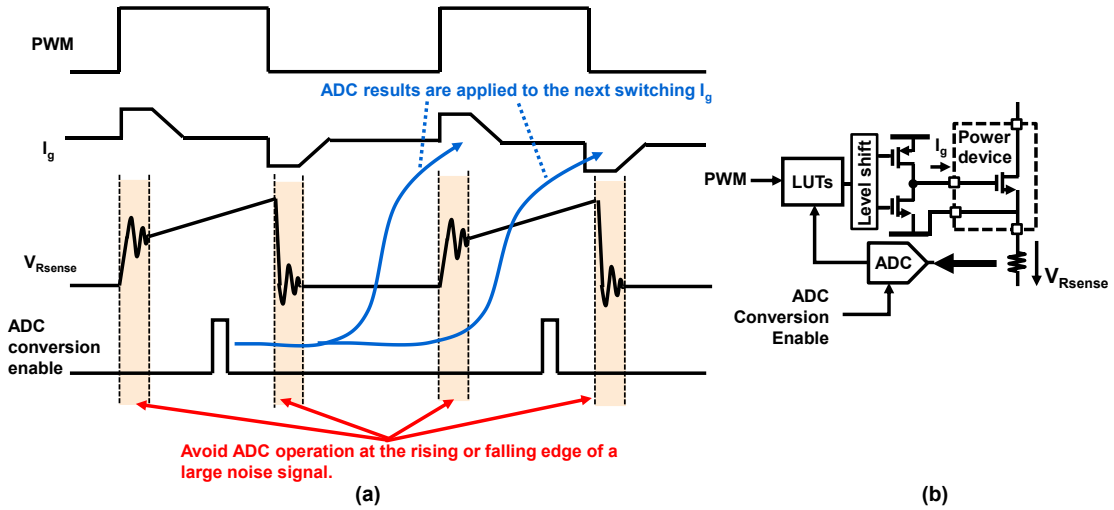


Figure 4.14: The timing of ADC operation and the driver circuit for detecting the load state of a power device

4.6 Measurement result

The gate driver test chip was fabricated in 0.5um CMOS with 40 V high-voltage transistors for the segmented current source. The performance is verified by using the device SCT3080KR [78], a 1.2 kV SiC-MOSFET. The device SCT3080KR has a TO-247-4L package and a Kelvin source. To avoid unwanted oscillations occurring in the gate voltage, a device with a package with less parasitic inductance was selected. The double pulse tests were performed under 400 V VCC. Figure 4.15 shows the measurement setup. The signal to write the LUT and the PWM signal are generated using Analog Discovery 2 from Digilent. The oscilloscope used to measure gate voltage, drain voltage, and drain current is a Tektronix MSO64. The oscilloscope and pattern generator are controlled by a PC.

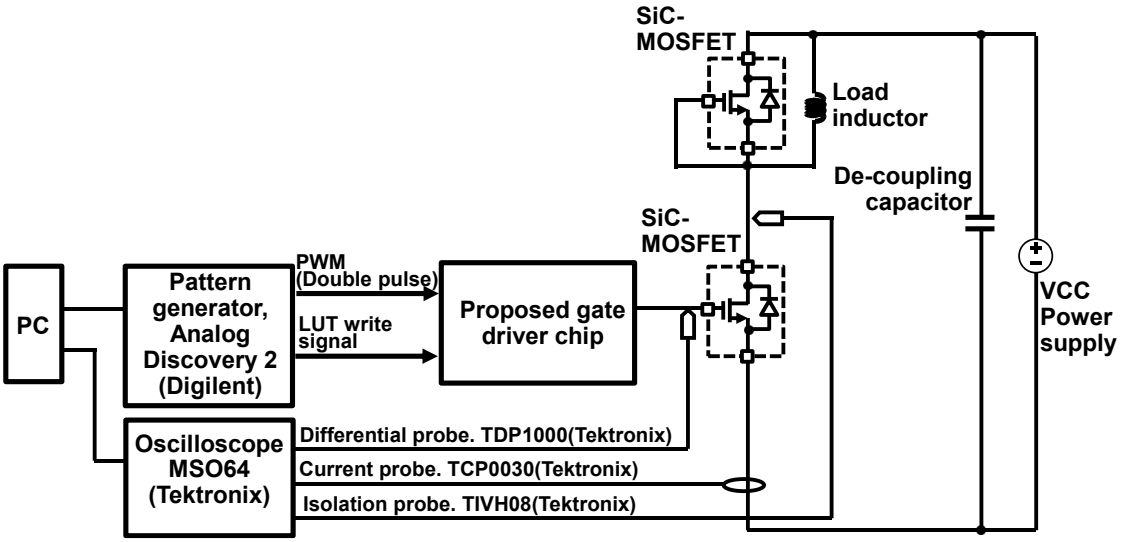


Figure 4.15: Measurement setup.

Figure 4.16 shows the drain voltage waveform of the optimized gate pattern with and without TRE. The TRE is adopted for the NMOS turn-on pattern. TRE enhances the optimization and compresses the surge by 31%(83V to 49V). Measured surge voltage and switching losses for drain currents of 3 A and 15 A are shown in Figure 4.17 and Figure 4.18. The constant current drive in Figure 4.17 and Figure 4.18 represents the case where the gate is driven without changing the current value in the time direction. Compared to the constant current drive, the proposed gate pattern achieves 51% and 27% surge reduction for the same level of switching loss at the load current of 15A and 3A, respectively.

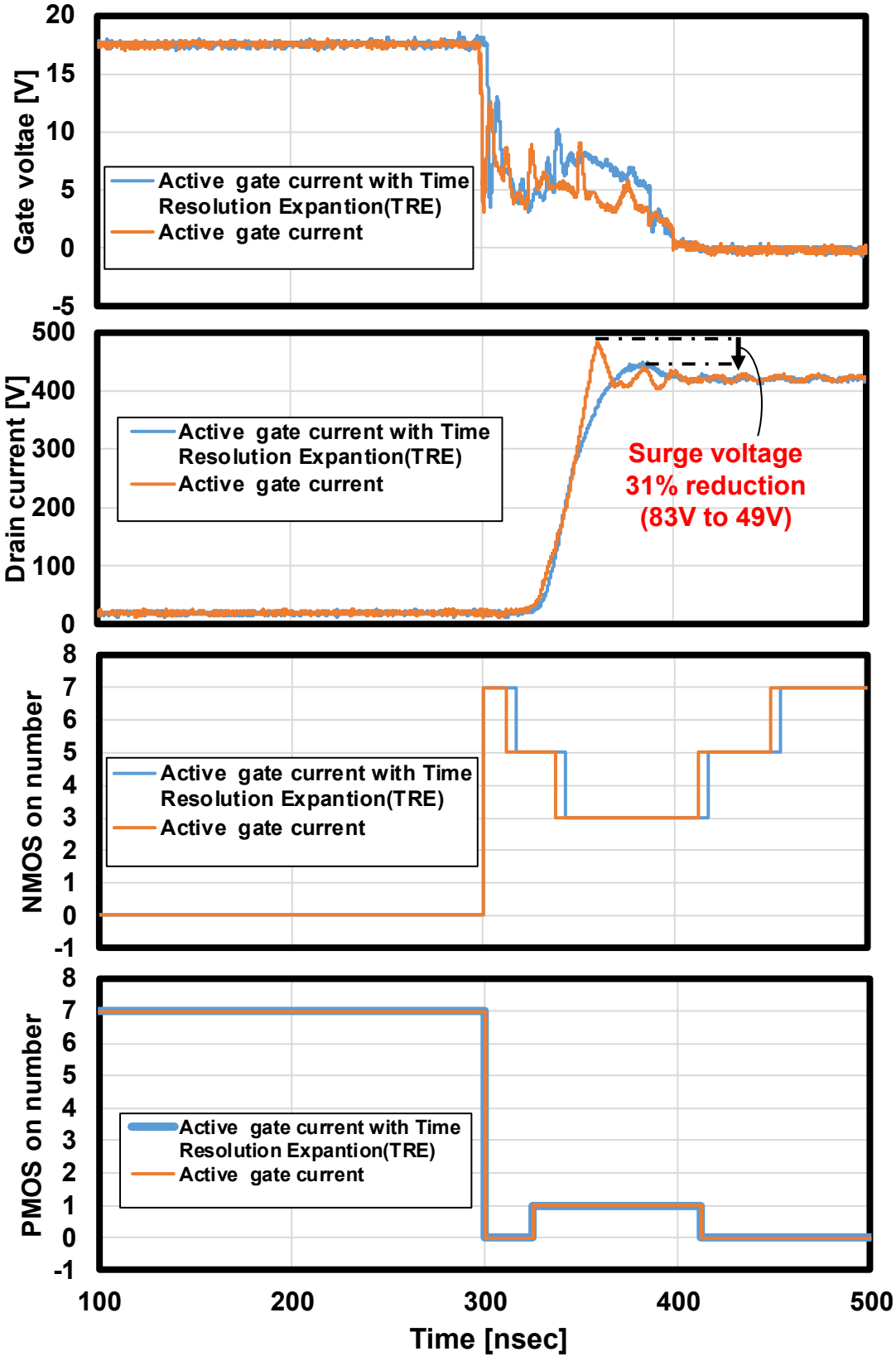


Figure 4.16: Measured turn-off waveforms with and without TRE.

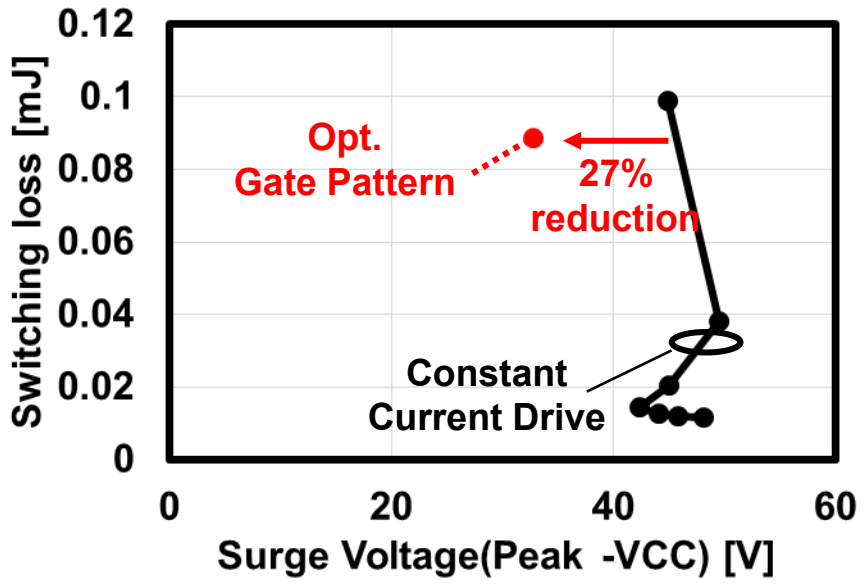


Figure 4.17: Measured surge voltage and switching losses at 3A drain current.

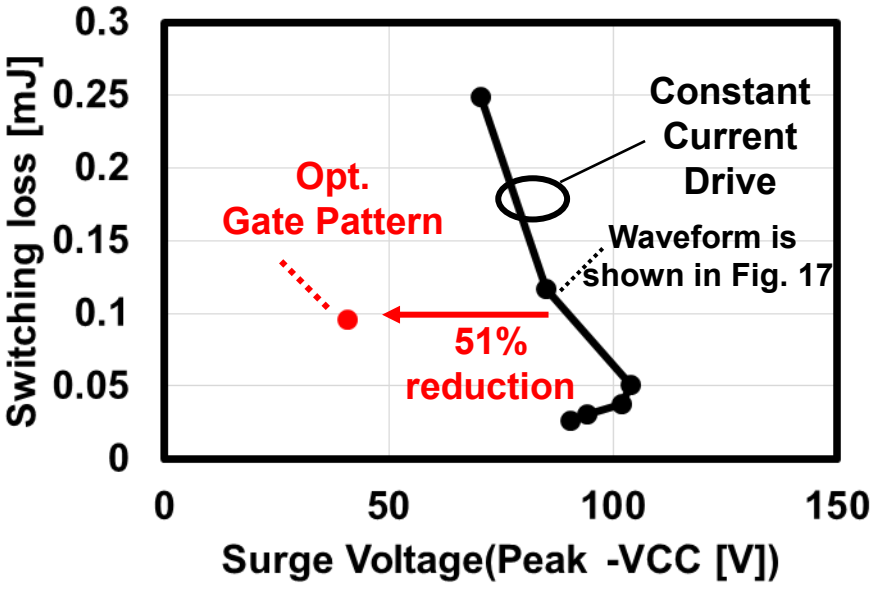


Figure 4.18: Measured surge voltage and switching losses at 15A drain current.

Figure 4.19 shows the switching waveforms using the proposed method and the conventional driving method at a drain current of 15 A. Using the proposed method, the surge voltage is

reduced by 51% from 85V to 40.1V. At time t_x in Figure 4.19, the PMOS is turned on. However, six NMOS are also turned on. In this study, the current value of 1 segment of PMOS and 1 segment of NMOS were designed as 522 mA and 153 mA, respectively. Therefore, at time t_x, the current flows from the gate of the power device to the driver direction. At time t_y in Figure 4.19, the number of NMOS on is reduced to 3. From time t_y, the current is flowing toward the gate of the power device. The gate current is flowing in the reverse direction before time t_z, when the resonant circuit is formed. The ringing of the drain voltage is successfully reduced. The dv_d/dt from 10% to 90% drain voltage increase with active gate control in Figure 4.19 is 16 V/ nsec.

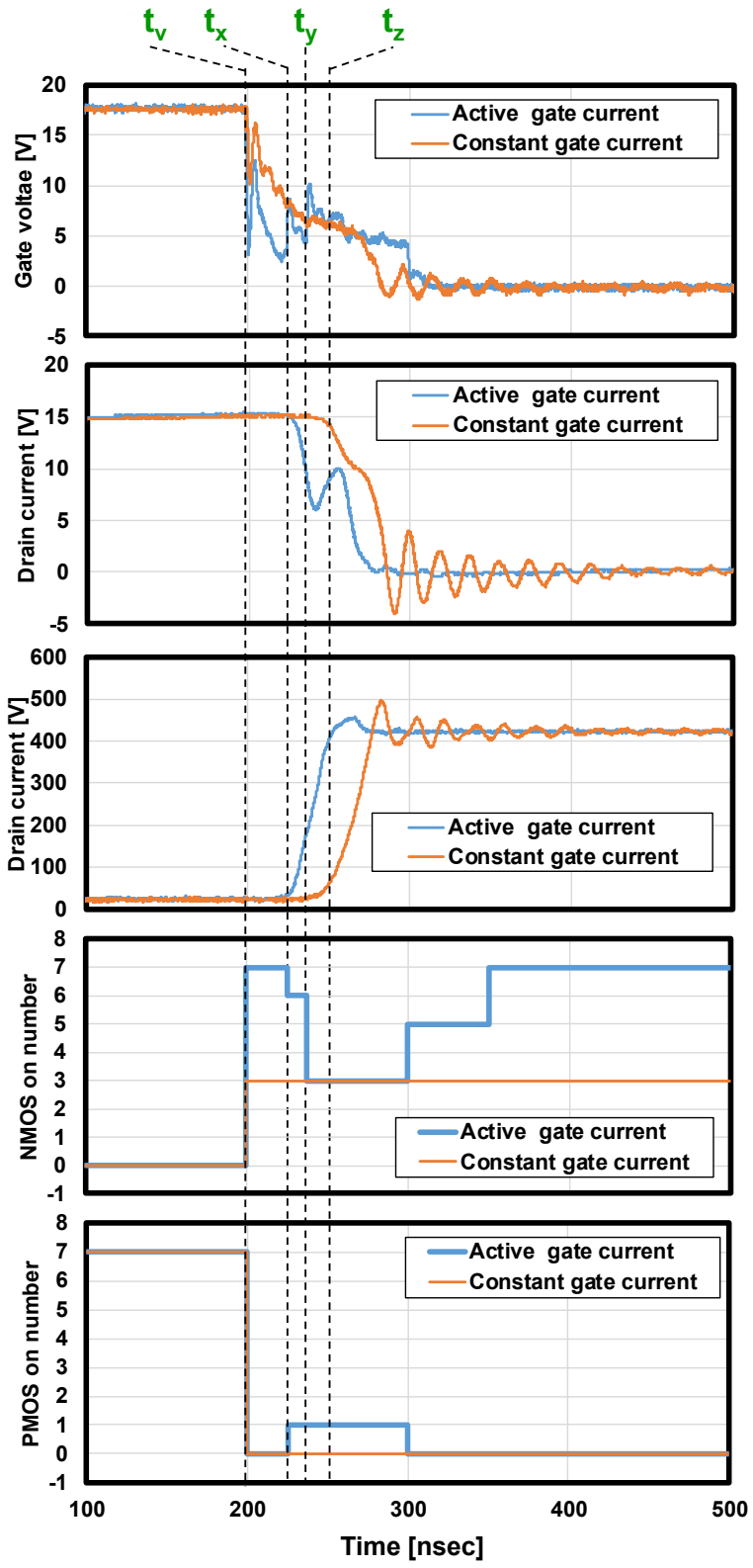


Figure 4.19: Measured switching waveforms using the proposed method and the conventional driving method at a drain current of 15 A.

The following shows the method of generating a gate current pattern that breaks the trade-off between surge voltage and losses in the measurement. The waveform generation was done manually with the measurement system shown in Figure 4.15, observing switching losses and surge voltages. As shown in the simulation and theoretical analysis in Section 2, there are two important aspects of the gate waveform that reduce the surge voltage. The first is to inject the gate current in the reverse direction shortly before the drain voltage reaches the power stage supply voltage, and the second is to keep the gate voltage value close to the threshold voltage value when injecting the gate current in the reverse direction. The method of how these two aspects are achieved with an active gate waveform is explained below.

First, the method to keep the gate voltage value close to the threshold voltage value when injecting the gate current in the reverse direction is described. Discharging the gate charge with a large gate current when turning off the power device is desirable in terms of turn-off delay reduction and switching loss reduction. Therefore, in the waveform shown in Figure 4.19, when the gate current draw starts at time t_v, the gate charge is discharged at the maximum current that the driver can provide. On the other hand, as shown in Section 2, the surge voltage cannot be reduced if the gate voltage is not close to the threshold voltage value when injecting the reverse current. If the gate charge continues to be discharged at a large gate current, the gate voltage falls far below the threshold voltage value at the time of injecting the reverse current. As a result, the surge voltage cannot be reduced even if the gate voltage is injected in the reverse direction, shown in Figure 4.7(a) in one example. The gate current should be varied to keep the gate voltage close to the value of the threshold voltage at the timing of injecting current in the reverse direction. At the time t_x when the gate voltage becomes close to the value of the threshold voltage, the driving force of NMOS is reduced and the driving force of PMOS is increased so that the gate voltage remains close to the value of the threshold voltage.

Next, the timing of injecting the gate current in the reverse direction is described. According to the simulation results shown in Figure 4.7 and the theoretical analysis in Section 2, injecting gate current in the reverse direction just before the drain voltage matches the power stage supply voltage does not reduce the surge voltage. Injecting gate current at an earlier timing enables the

surge voltage to be reduced. In the simulation shown in Figure 4.7(b), the surge voltage is successfully reduced when the gate current is injected in the reverse direction at the timing when the drain voltage reaches 100V instead of when the drain voltage reaches the power stage voltage of 400V. In the measurement, the gate current must be injected in the reverse direction at an earlier time as in the simulation, not just before the drain voltage matches the power stage voltage. In this measurement, the surge voltage was successfully reduced by injecting the gate current in the reverse direction at the time t_y shown in Figure 4.19, when the drain voltage reached 200V. With respect to the timing of injecting the gate current in the reverse direction, the difference between the simulation and the actual measurement is considered to be the difference in the non-linearity of the capacitance of the device used.

Figure 4.20 shows the relationship of the surge voltage and load current for each optimized gate pattern. As shown in Figure 4.20, the gate pattern optimized at a specific load current is not the best in other current ranges, and therefore the load adaptation is obviously effective.

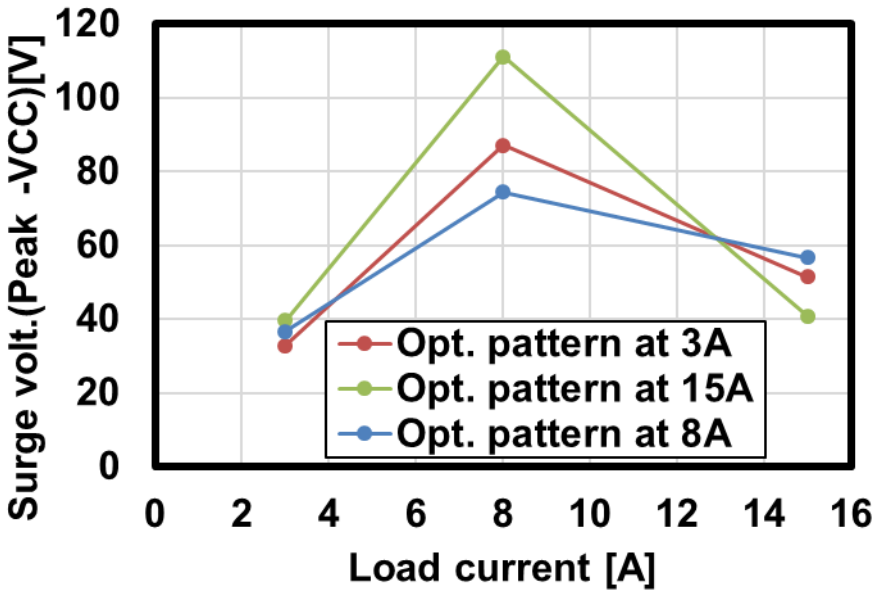


Figure 4.20: The relationship of the surge voltage and load current for each optimized gate pattern.

Figure 4.21 shows the dynamic load adaptation. The measurement circuit is shown in the lower left corner of Figure 4.20. The load current is detected by sensing the drain current i_d after

SiC-MOSFET turn-on. The ADC shown in Figure 4.20 detects the drain current i_d flowing in the SiC-MOSFET by sensing the voltage across the resistor R_{sense}. One of the LUTs is selected according to the output value of the ADC, and the gate current i_g defined by the selected LUT is output to the SiC-MOSFET. The time waveforms of drain voltage v_{ds}, drain current i_d, and gate voltage v_{gs} are shown at lower right in Figure 4.21. A double pulse signal is used as input. The drain current i_d is 3 A at the first switching shown by the red frame at lower right in Figure 4.21. In the second switching, shown by the blue frame at lower right in Figure 4.21, the drain current i_d is 6 A. A magnified view of the first switching waveform is shown at upper left in Figure 4.21, and a magnified view of the waveform during the second switching is shown at upper right in Figure 4.21. In the first switching with drain current i_d=3 A, the gate current i_g defined by LUT1 is supplied to the gate of the SiC-MOSFET. In the second switching, the output of the ADC changes because the drain current i_d has increased from 3 A to 6 A. The LUT2 is selected by the ADC changes because the drain current i_d has increased from 3 A to 6 A. The LUT2 is selected by the ADC output and the gate current i_g defined by LUT2 is supplied to the gate of the SiC-MOSFET.

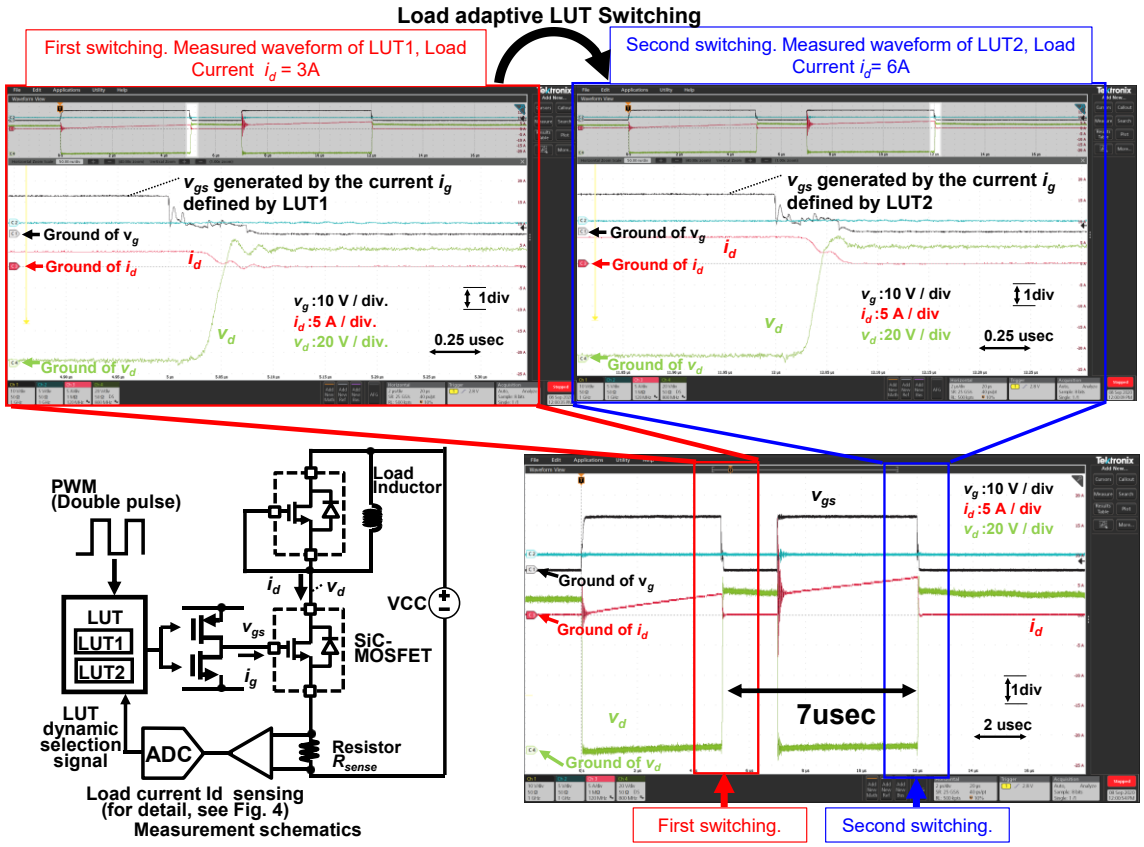


Figure 4.21: Measured result of dynamic load adaption.

The patterns of LUT1 and LUT2 are shown on the left in Figure 4.22. The waveforms of the gate voltage v_{gs} during the first and second switching are overlaid on the right in Figure 4.22. As shown on the right in Figure 4.22, the gate voltage v_{gs} is different between the first and second switching. Different LUTs are successfully selected and output according to the drain current i_d. As shown at lower right in Figure 4.21, the time between the first and second switching is 7 usec. During the time of 7 usec, the ADC detects the drain current, the LUT switches, and the gate waveform is successfully replaced. Since the pulse carrier frequency for motor drive is typically less than 20 kHz, the loop response of the chip is fast enough for load adaptation. In this scheme, the drain current i_d is sensed at a transient current one pulse ahead of the target transient current, and so the drain current variation must be slow enough relative to the PWM carrier frequency to achieve proper control. Since this relationship holds true for many motor applications, this scheme is acceptable.

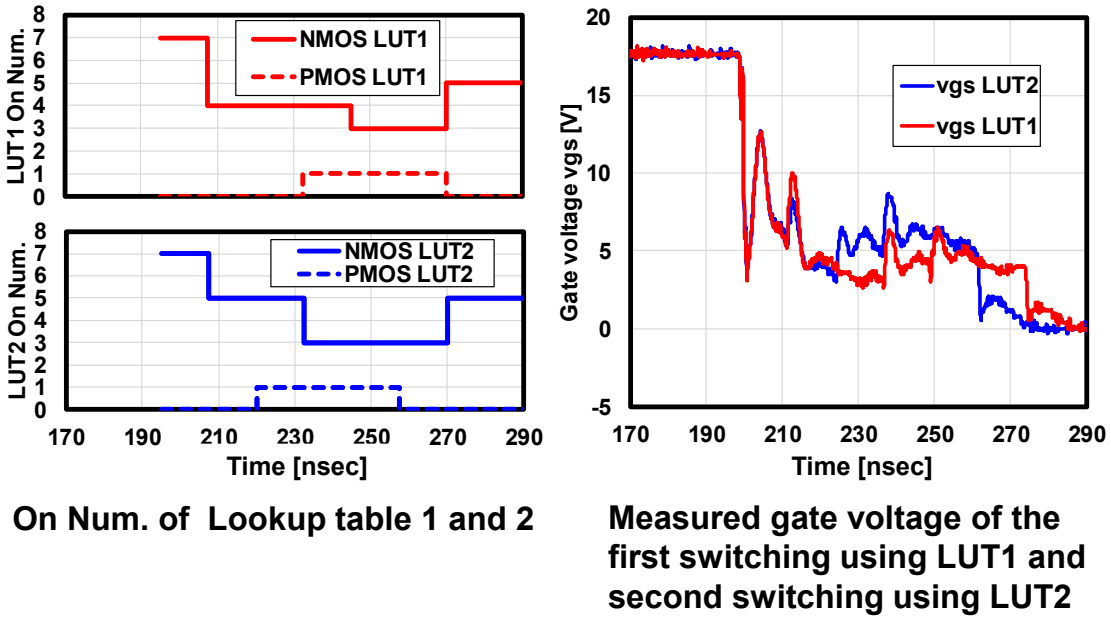


Figure 4.22: On number of MOS stored in LUT1 and LUT2 used to measure the dynamic load adoption shown in Fig 4.19. The measured waveforms of the gate voltages of the first and second switching overlaid.

The measurement results of the three sampling FEs are presented in Figure 4.23. The measured result of the load current sampling FE is shown at upper left in Figure 4.23. The blue line shows the analog drain current waveform. This current waveform is obtained from the calculation by measuring the differential voltage of the resistor R_{sense} by differential probe. The orange line shows the output code of the ADC. The ADC output code matches the measurement result of the drain current. The load current sensing FE is also used for the dynamic LUT adaptation as shown in Figure 4.21. The measurement result of the V_{ds}-on monitoring FE is shown at upper right in Figure 4.23. The blue line shows the analog voltage of the ADC input. This input voltage is the same as the anode voltage of diode D_4. The orange line is the ADC output code. The ADC output code matches the measurement result of the analog V_{ds}-on voltage. The measurement result of the surge monitoring FE is shown at the bottom of Figure 4.23. The blue line is the ADC input voltage, which is the same as the voltage of capacitor C_2. The orange line is the ADC output code. The surge voltage is successfully detected by the surge monitoring

FE circuit and the ADC output code matches the analog input voltage. By using the proposed sampling FE, the V_{ds}-on voltage and the surge voltage sensing during the SiC switching is acceptable, and very fast short-circuit protection in 2 us, which is limited by the ADC sampling rate, is achieved.

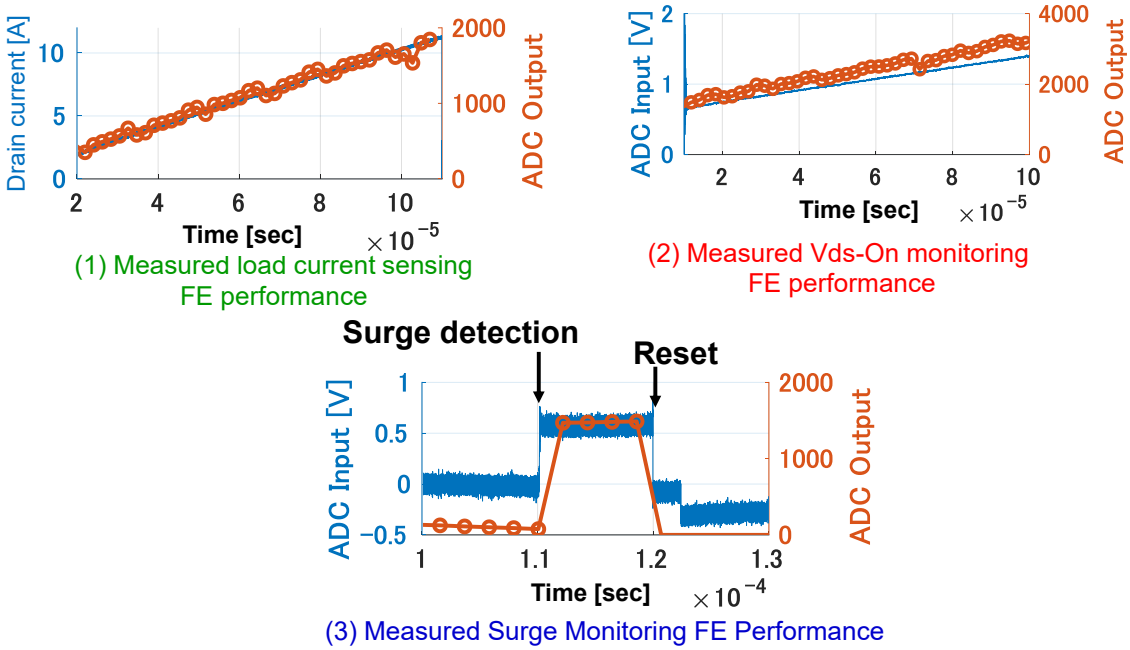
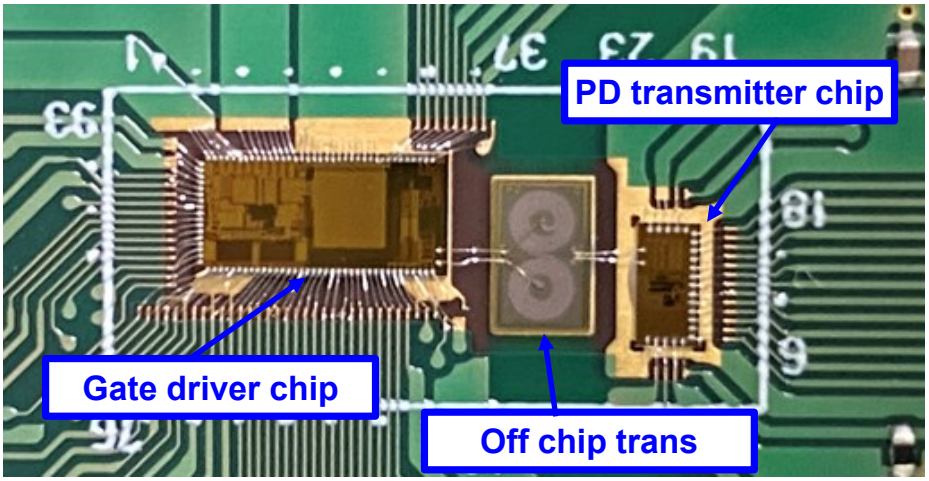


Figure 4.23: Measured result of sampling front-end.

The measured results of the receiver for the auxiliary isolated power transfer and the automatic VDD selector are shown in Figure 4.24. Shown on the left in Figure 4.24 are the off-chip transformer, the Power Delivery (PD) transmitter chip, and the gate driver chip. The PD transmitter chip was fabricated in 130 nm CMOS process. The chip provides over 10 mW power consumption with enough margin. The measured ADC VDD and rectifier output voltage are shown on the right in Figure 4.24. Without using the PD chip, the ADC VDD is decreased as shown by the blue line in Figure 4.24. When the PD chip is operating, the PD chip is constantly sending power. The ADC operates with the power acquired from the PD chip through wireless power transmission in the case that the power from VCC to the gate driver is interrupted. As shown by the red line in Figure 4.24, the ADC VDD keeps the minimum requirement of 4.0 V by using the power transfer circuit.



Photograph of PD chip, off chip trans, and gate driver chip

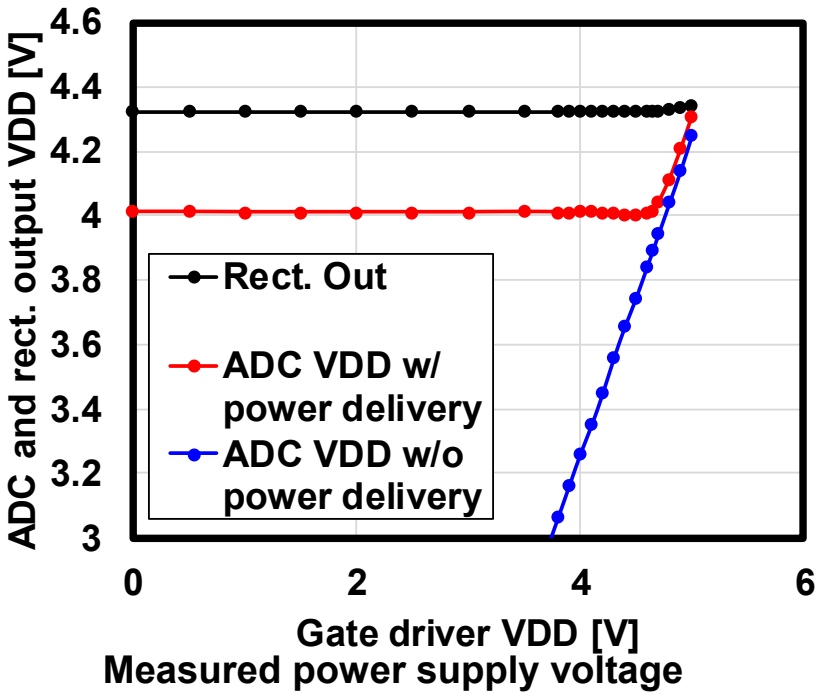


Figure 4.24: Photograph and measured results of isolated power transfer.

Figure 4.25 shows the photograph of the test chip fabricated in 0.5um CMOS with 40 V HV transistors. The chip size is 6mm x 3mm. Table 1 shows the Comparison table. In this study, eight LUTs were integrated on a chip to demonstrate surge voltage reduction for a 1200 V SiC application. As shown in Table 1, the slew rate or dv_d/dt of the power device with the active gate

technology in this study is 16 V/nsec, which is slower than the switching rate with GaN devices, however the same or faster than the other works SiC-MOSFET, IGBT and Si-MOSFET devices. The driver IC in this paper can output active gate waveforms and suppress surge voltage under switching conditions where the drain voltage slew rate is more than 10 V/nsec. The proposed driver IC successfully breaks the trade-off between surge voltage and power consumption. The function to switch the optimum waveform following the load current of the power device was realized in a single chip. The load adaptive gate waveform output was demonstrated using proposed digital gate driver with a high degree of freedom of waveform.

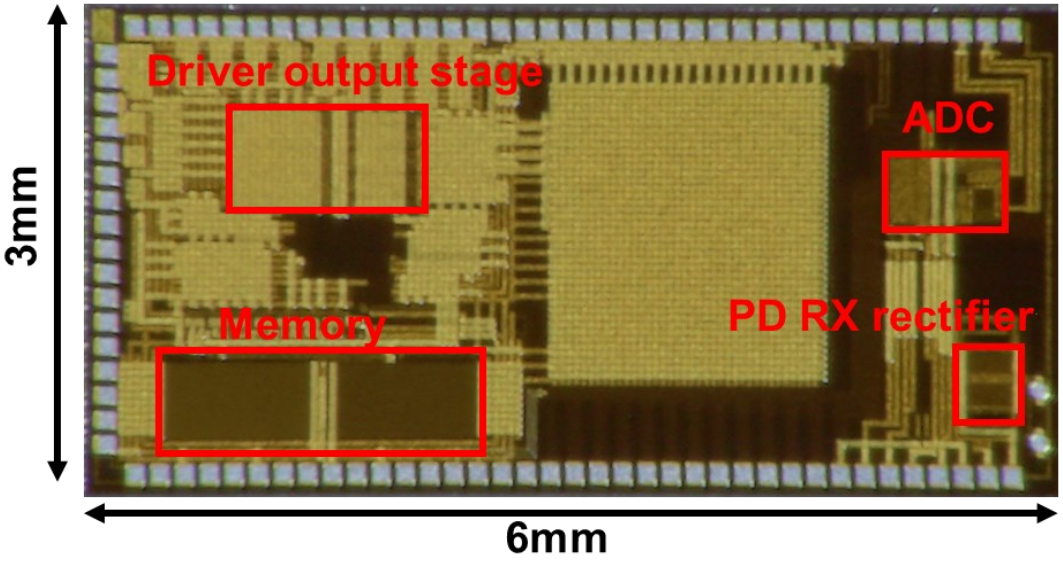


Figure 4.25: Chip micrograph.

Table 4.1: Comparison table of conventional driver and proposed digital gate driver.

	[42] TPE 2018	[39] TPE 2017	[66] ISSCC 2019	[44] TIE 2020	[24] TPE 2015	[43] TPE 2021	[47] TPE 2022	[65] TCAS 2022	This Work
Control strategy	Digital	Digital	Analog	Digital	Analog	Digital	Digital	Digital	Digital
#LUT	1 (on chip)	1 (off chip)	NA	8 (off chip)	NA	1 (on chip)	NA	NA	8 (on chip)
Load adaptive	No	No	Yes	No	Yes	No	Yes	No	Yes
Integrated ADC	No	No	NA	No	No	No	No	No	Yes
Time resolution expansion	Yes	No	NA	No	No	Yes	No	No	Yes
Time step	150 psec	40 nsec	Continuous	Unknown	Continuous	100 psec	250 psec	Continuous	1 nsec
Simultaneous PMOS NMOS Cont.	Yes	No	No	No	No	Yes	No	No	Yes
Power supply of driver	+5 V / 0 V	+15 V / 0 V	+10 V / 0 V	+20 V / -5 V	+14 V / -10 V	+5 V / 0 V	NA	+15V / -5V	+18 V / 0 V
Process(gate driver chip)	Unknown	40 V, 0.18 um BCD	18 V, 0.13 um CMOS	Discrete	Discrete	0.18um HV-CMOS	Discrete	0.18um BCD	40 V, 0.5 um CMOS
Target device	40 V GaN (EPC2015)	1200 V IGBT ,SiC(SCH2080KR)	600 V SJ-MOS*4 (TK8A60W5)	1200 V SiC (CAS120M12BM2)	1200 V IGBT (FF300R12MS4)	600V GaN (GS66508P)	75V N-ch (FDB031N08)	1200 V SiC (C3M0016120K)	1200 V SiC (SCT3080KR)
Driver output current	NA	756mA	NA	NA	NA	NA	NA	NA	3.6 A
Turn-off SR*3,4 when active gate is applied	2 V / nsec*1	6 V / nsec*1	-4.5 V / nsec*2	18 V / nsec*1	2 V / nsec*	100 V / nsec	-1.5 V / nsec*1,*2	12 V / nsec*1	16 V/ nsec
Target of active gate control	Turn-on I_d surge, Turn -off V_d surge.	Turn-on I_d surge, Turn off V_d surge.	Turn-on V_d slew rate	Turn-on I_d surge, Turn off V_d surge	Turn-on I_d/V_d SR*3,Turn-off I_d/V_d SR*3	Turn-on I_d surge,	Turn-on V_d surge.	Turn-off V_d surge.	Turn-off V_d surge.
Experimental results that breaks the trade-off between loss and surge	Yes	Yes	Yes	Yes	Yes	No	Yes	No	Yes

*1Estimated from figure.
*2Turn on slew rate.
*3Slew Rate (dv_d/dt). Speed when drain voltage changes from 10% to 90%.
*4Superjunction MOSFET

4.7 Generation nethod of optimal gate waveforms for products

This section describes how to generate the optimum gate waveform for an actual product.

The Figure 4.26 shows a flowchart of the optimal gate waveform generation method assuming an actual product. First, the optimal waveform is designed by simulation. To perform the simulation, the value of parasitic inductance of the equivalent circuit shown in Figure 4.2 is required. This value is extracted based on information from the boards of power converters and inverters in similar products in the past. For example, the layout of power stage circuits of inverters and converters in electric vehicle powertrains and server power supplies will not change significantly when the products are replaced by next-generation ones. Therefore, it is possible to extract parasitic inductance values with sufficient accuracy by referring to past products.

Next, the optimal gate waveform is designed by simulation. The gate waveform is designed based on the method described in section 4.2 of this paper. In this process, the variation in the characteristics of the power device is simulated, and the gate waveform is also designed for the variation in the characteristics of the power device.

Finally, the optimal waveforms are designed by measurement. The parasitic inductance in the power stage of the actually created inverter or converter may differ from the value used in the simulation. Based on the simulation waveforms created in No. 2 of the flowchart shown in Figure 4.26, the optimal gate waveforms are designed by measurement. The method of designing the waveforms by measurement with reference to the simulation is described in section 4.5 of this paper.

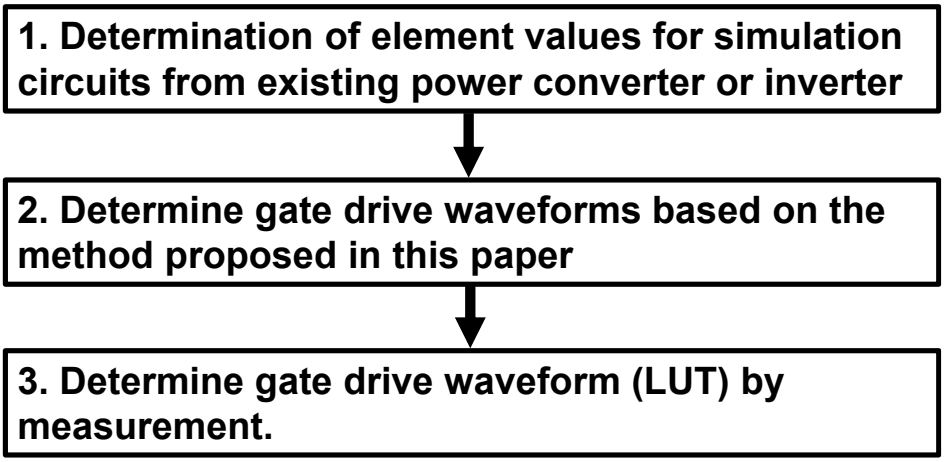


Figure 4.26: Flowchart of the optimal gate waveform generation method assuming an actual product

4.8 Optimum gate waveform application method for characteristic variation of power devices

This section describes how to apply optimal gate waveforms to the characteristic variations of power devices. Power devices have variations in temperature, supply voltage, capacitance, transconductance, and threshold voltage. The above variations can be classified into two types: those caused by environmental variations and those caused during manufacturing. Temperature and supply voltage depend on the environment surrounding the board on which the power device is mounted. On the other hand, capacitance is a variation caused by the manufacturing process of the power device and does not depend on the surrounding environment. Transconductance and threshold voltage vary with temperature and also exist as manufacturing-induced variations.

First, the following shows how the optimal waveform is applied with respect to the variation caused by environmental variations. Figure 4.27 shows the method of applying the optimum waveform to the variation caused by environmental variation. The driver IC proposed in Chapter 4 has an integrated ADC. The ADC detects variations in the power device and outputs the optimal waveform for each variation. By adopting the above method, the optimal waveform can be supplied according to the condition of the power device, even if environmental variations

of the power device occur.

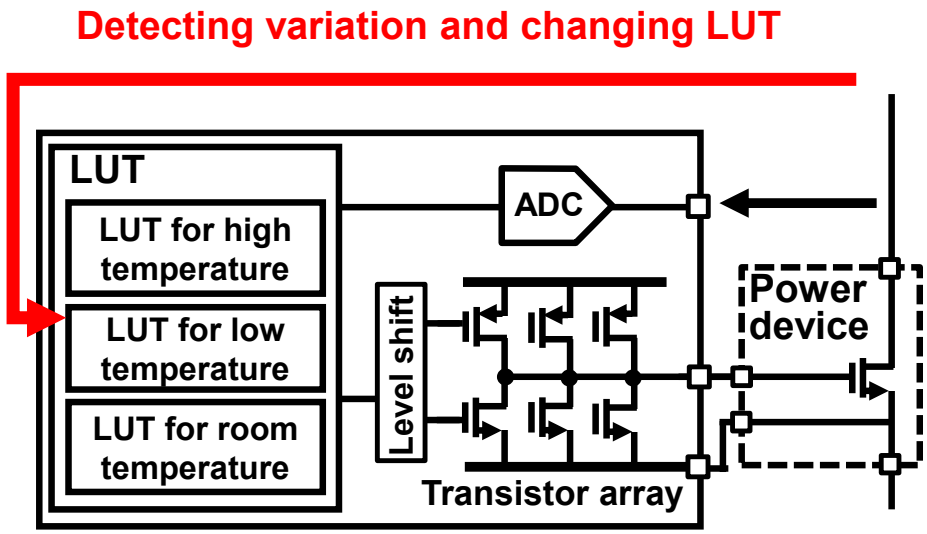


Figure 4.27: The method of applying the optimum waveform to the variation caused by environmental variation.

The method of detecting environmental fluctuations of power devices is described below. For power supply voltage fluctuations, the power supply voltage is divided by a resistor, and the divided voltage is detected by an ADC. There are several methods for detecting temperature. As shown in the Figure 4.28(a), the temperature of a power device can be detected by integrating a thermistor in the package of the power device and detecting the voltage of the thermistor. Depending on the position of the thermistor in the package, there is a difference between the junction temperature of the power device and the temperature of the thermistor. However, in the application of optimal gate waveform switching, it is not always necessary to accurately detect the junction temperature. Temperature information without high accuracy obtained from the voltage of the thermistor can also be used to switch the optimal gate waveform.

In addition, the internal gate resistance of a power device has temperature-dependent characteristics. By detecting the value of the internal gate resistance as shown in the Figure 4.28(b), the junction temperature Tj of the power device can be detected. Methods for detecting internal gate resistance have been studied in the literature [79] [80]. Compared to the method using a thermistor, it can detect the temperature more accurately.

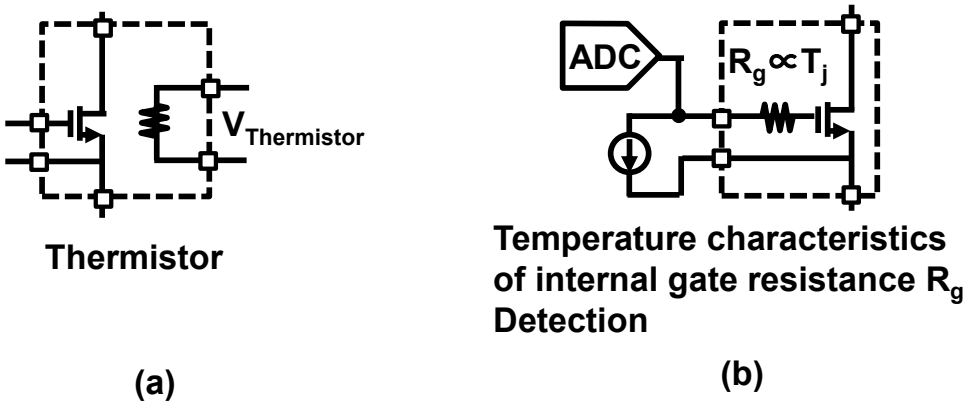


Figure 4.28: Temperature detection method of power device

Next, the method of applying the optimal gate waveform in the presence of manufacturing variation is discussed. Figure 4.29 shows the concept of writing the optimal gate waveform to the LUT at the shipment stage. The optimal gate waveforms corresponding to the threshold and capacitance variations of power devices are prepared, and the waveforms are written into the LUT when the driver IC is shipped. For example, for a device with a large threshold value, the optimal gate waveforms for a high threshold value are written to the driver IC in advance at the shipment.

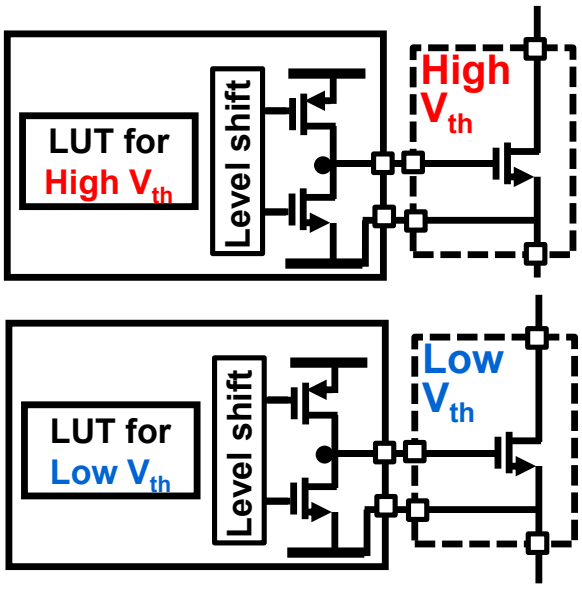


Figure 4.29: The concept of writing the optimal gate waveform to the LUT at the shipment stage.

Finally, the figure shows how to handle both environmental variations and manufacturing-induced variations. Even if the characteristics of the power device fluctuate, the characteristics of the power device can be improved by preparing an optimal gate waveform that covers all variation characteristics. For example, as shown in the figure, if an optimal gate waveform can be prepared that can be applied under all capacitance variations, the characteristics of the power device can be improved even if manufacturing-induced capacitance variations exist.

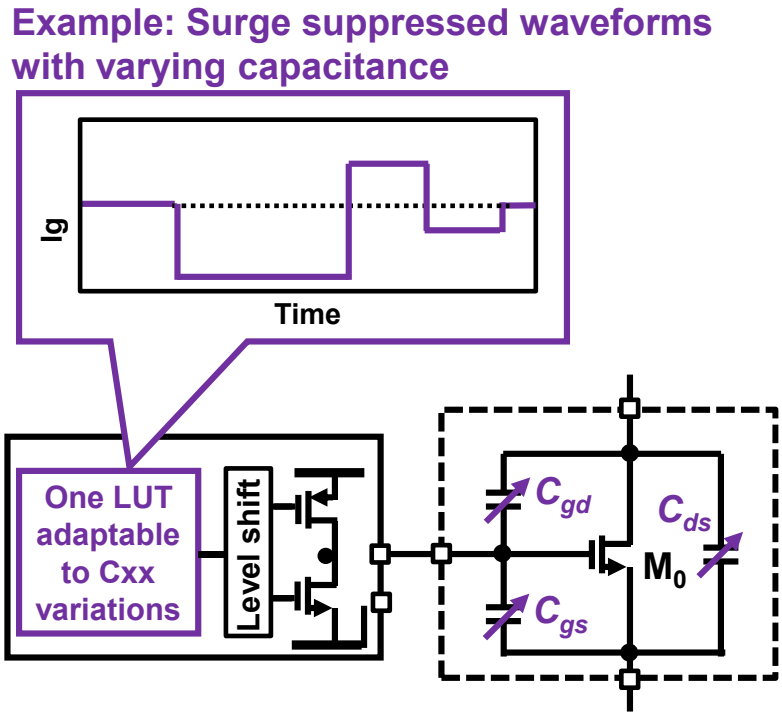


Figure 4.30: Uses waveforms that can improve performance even when variability in characteristics occurs

4.9 Applicability of the proposed digital FF driver IC proposed in chapter 4

This section describes the scope of application of the digital feed-forward driver IC proposed in chapter 4. As described in chapter 2, the driver IC proposed in Chapter 4 is designed for SiC-MOSFETs used at high switching frequency and at high converter power. However, the

optimal gate waveform using the backward current injection technique proposed in Chapter 4 can be applied to devices with large nonlinearities in capacitance C_{rss}.

The Figure 4.31 shows the drain voltage dependence of the capacitance in a Toshiba SiC-MOSFET and SJMOS. The model number of the SiC-MOSFET is TW070J120B. the model number of the SJMOS is TK8A60W5. As shown in Figure 4.31(a), the SiC-MOSFET capacitance C_{rss} depends on the drain voltage. The capacitance C_{rss} of the SJMOS also depends on the drain voltage as shown in Figure 4.31(b). The value of the capacitance C_{rss} changes by 2.5 orders of magnitude with increasing drain voltage. Therefore, the driver IC proposed in Chapter 4 can be applied to SJMOS as well.

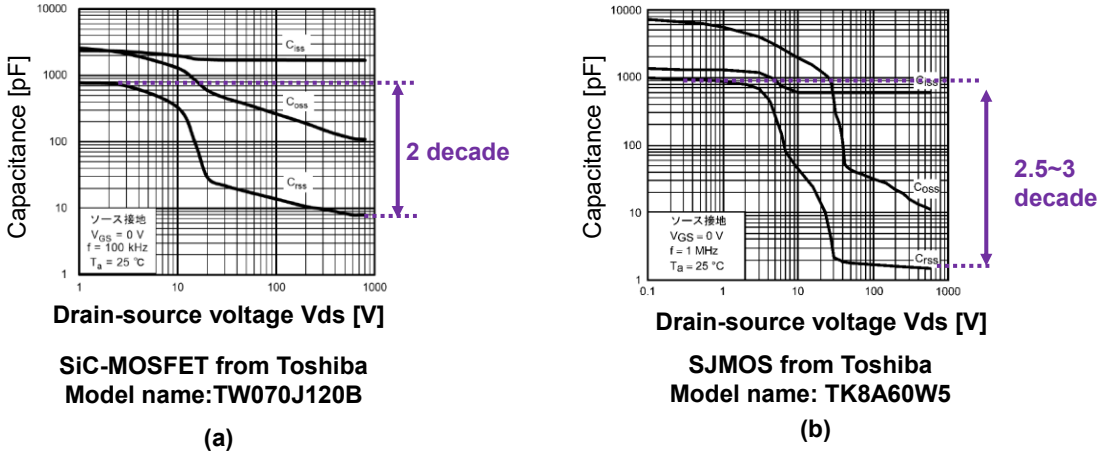


Figure 4.31: Drain voltage dependence of SiC-MOSFET and SJMOS capacitance.

The Figure 4.32 shows the voltage dependence of the capacitance of a Rohm GaNFET and an Infenion IGBT; the model number of the GaNFET is GNP1150TCA-Z. The model number of the IGBT is ILZ75N65EL5. As shown in Figure 4.32(a), the capacitance C_{rss} of the GaNFET changes its value by two orders of magnitude as the drain voltage increases. On the other hand, the capacitance C_{rss} of the IGBT, as shown in Figure 4.32(b), increases in value by only about one order of magnitude with increasing drain voltage. Although Figure 4.32(b) only shows the collector-emitter voltage up to 30V, the capacitance C_{rss} is expected to change by only 1.5 orders of magnitude even when the voltage reaches several hundred volts. From the above, the driver IC proposed in Chapter 4 can be applied to GaN. On the other hand, for IGBTs, the capacitance

nonlinearity is not so large that it is unclear whether the technology proposed in Chapter 4 can be applied.

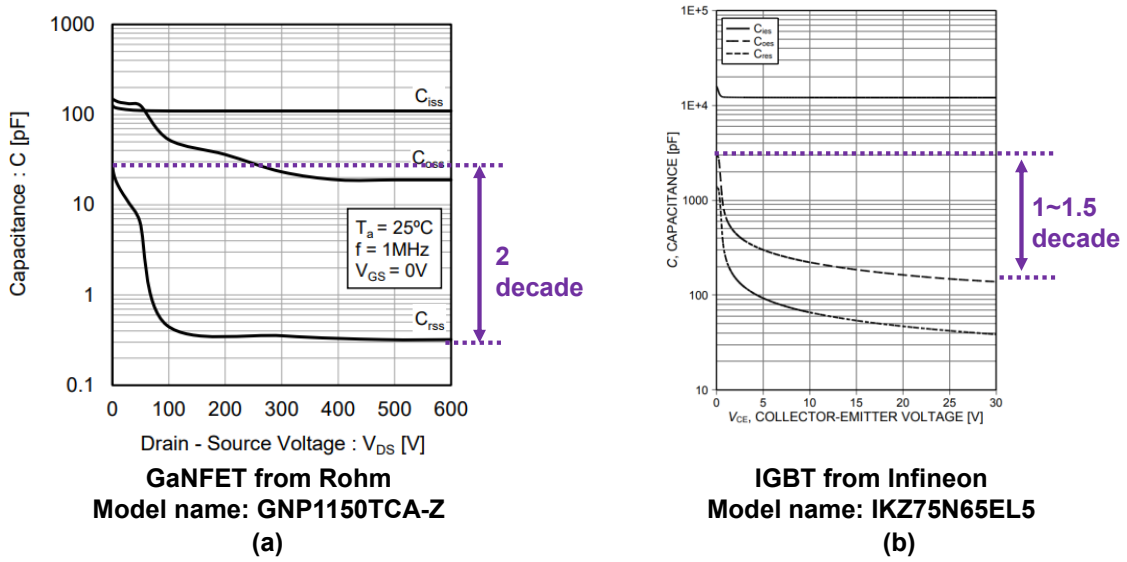


Figure 4.32: Drain voltage dependence of GaNFET and IGBT capacitance.

For IGBTs, it is also necessary to consider the tail current during turn-off. Figure 4.33(a) shows the equivalent circuits of SiC-MOSFETs and IGBTs. Figure 4.33(b) shows the waveforms of the drain current I_D and drain voltage V_D for the SiC-MOSFET and the collector current I_C and collector voltage V_C for the IGBT. IGBTs take more time to reach zero current at turn-off compared to SiC-MOSFETs. The turn-off phenomenon of IGBTs is different from that of SiC-MOSFETs. Therefore, the results of the SiC-MOSFET analysis presented in Chapter 4 cannot be used for IGBTs. For the above reasons, it is also unclear whether the driver IC proposed in Chapter 4 can be applied to IGBTs.

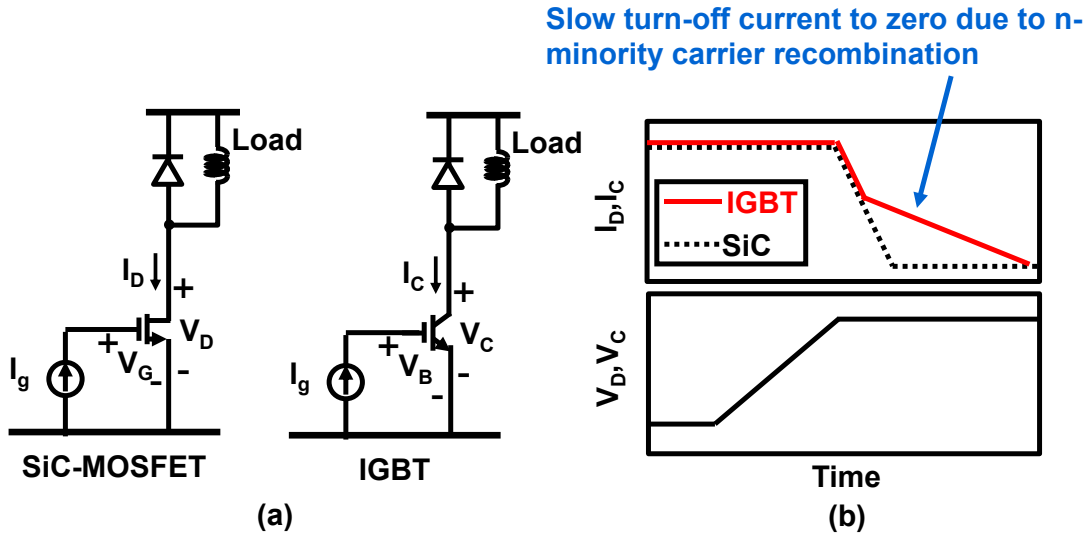


Figure 4.33: Equivalent circuit and turn-off time waveforms of SiC-MOSFET and IGBT.

Figure 4.34shows the range of possible applications of the driver IC proposed in Chapter 4, and it is unclear whether the driver IC proposed in Chapter 4 can be applied to IGBTs. However, the driver IC proposed in Chapter 4 can be applied to SJMOS and GaN.

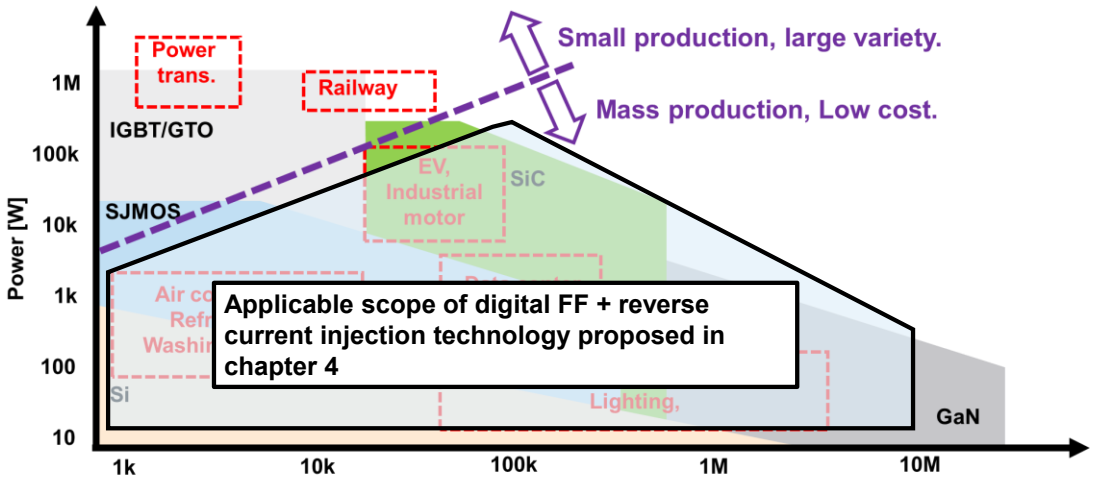


Figure 4.34: Applicable scope of digital FF + reverse current injection technology.

4.10 Summary of chapter 4

A fully integrated load adaptive digital gate driver with an on-chip ADC for functional safety is demonstrated for SiC-MOSFETs. The turn-off behavior of SiC-MOSFETs is analyzed by simulation, and it is shown that injecting the gate current in the reverse direction is effective in reducing the surge voltage. Measured surge voltage was reduced by 51% without increasing losses. The optimized current patterns stored in the on-chip LUT reduce surge voltage without increasing the switching loss. The sampling FE for functional safety successfully monitors the load current, surge voltage and V_{ds}-on voltage of the power device.

Chapter 5 Summary and future discussions

5.1 Summary

This chapter summarizes the findings of this thesis.

In Chapter 1, an overview of power electronics was presented and the importance of power converters was shown in terms of industrial aspects and power consumption. The history of the evolution of power electronics and the technologies that are expected to be responsible for the next generation of technological innovation are presented. It was also shown that the active gate technology presented in this paper is not only an important technology responsible for improving the performance of power converters, but also a fundamental technology that can be applied to other innovative technologies. Furthermore, the structure of this paper is presented.

In chapter 2, the characteristics, advantages, and disadvantages of power devices for each material are presented: SJMOS is used in high-voltage, low-power applications due to its low cost, although it has the disadvantage of increased loss due to recovery current, and SiC-MOSFETs with low ON-resistance and fast switching speed are used in high-voltage, high-power applications. SiC-MOSFETs, which have low ON-resistance and fast switching, have been used in recent years for high-voltage and high-power applications. The time waveform of a power device switching and the effect of the waveform on noise were described, and the trade-off between switching loss and noise was explained. Active gate technology was classified into analog and digital technologies, and the advantages and disadvantages of each were described. Issues in terms of the characteristics of active gate technology and power devices are summarized, and the corresponding relationship to the issues to be solved by the technology proposed in this paper is presented.

Chapter 3 describes an analog active gate driver IC using discrete-time feedback technique, where two resistors are controlled by the feedback technique to control the turn-on dVd/dt of the SJMOS. The proposed technique feeds back the feedback result to the next switching, thus

controlling the dVd/dt that depends on the reverse recovery current. It also does not require a wideband amplifier. The driver IC was prototyped in a 0.6um CMOS process, and the turn-on delay and switching losses were successfully reduced by 74% and 25%, respectively.

Chapter 4 describes an active gate driver IC using digital feed-forward technology. simulation analysis of turn-off considering the non-linearity of SiC-MOSFET capacitance was performed to identify the cause of voltage ringing during turn-on and the gate current that reduces ringing. The waveforms of the gate current that reduces ringing were clarified. An active gate waveform was proposed to temporarily reverse the gate current to reduce ringing. We also proposed a time resolution extension circuit to reduce the amount of memory and time resolution of the driver IC. Using an ADC integrated in the driver IC, the load of the SiCMOSFET was detected and the active gate waveform was successfully output according to the load. Turn-off voltage surges were reduced by 51% without increasing losses.

5.2 Future work

5.2.1 Parallel device drive.

To increase the current rating of a power device, multiple power devices are placed in parallel and driven (parallel drive). Figure 5.1 shows the schematic of parallel drive. In parallel driving, if there is an imbalance in the current of each power device, the current will be concentrated in one device and the device will be destroyed. Current imbalance can be classified into two types: transient imbalance, which is caused by the difference in the rise speed of current at turn-on due to the difference in parasitic capacitance, and unbalance in the conduction state due to the difference in threshold voltage. The transient unbalance has been studied for IGBTs and SiCMOSFETs using active gate technology [81] [82]. However, there is no research on how to resolve the unbalance in the conduction state. Furthermore, current-voltage ringing due to parasitic inductance and parasitic capacitance also occurs in parallel drive, causing noise. By placing an active gate driver for each element in parallel drive and driving with waveforms appropriate for each element, it may be possible to eliminate current imbalance and drive without current-voltage ringing and without increasing loss.

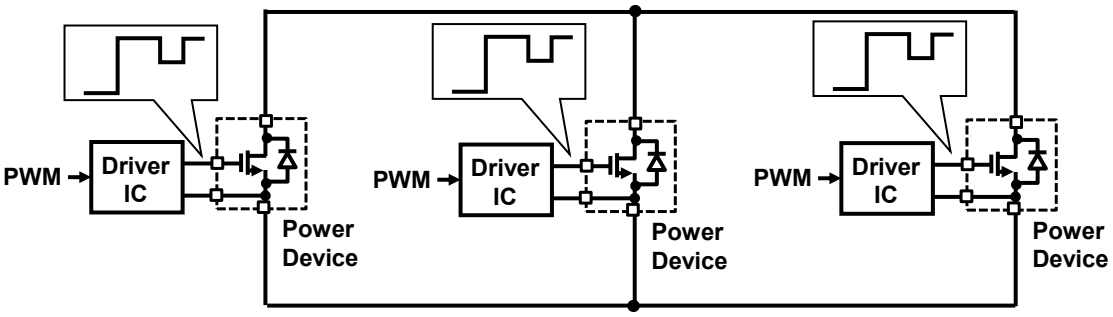


Figure 5.1: Schematic of parallel driving.

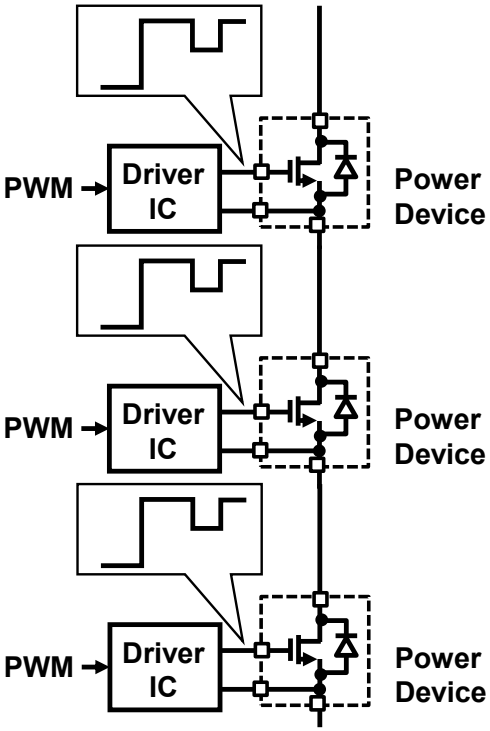


Figure 5.2: Schematic of series driving.

5.2.2 Series device drive

To increase the breakdown voltage of power devices, multiple power devices are placed in series and driven. Figure 5.2 shows schematic of series drive. If the transition rate of the voltage at turn-off of the power devices is not constant, the voltage will be concentrated in one device and the device may be destroyed. Furthermore, current-voltage ringing may occur due to parasitic capacitance and parasitic inductance present in devices placed in series. Two

Techniques have been proposed to eliminate voltage imbalance by placing devices in series [83] [84]. However, there is no example of eliminating voltage imbalance and voltage ringing at the same time. By applying active gate technology to each device, it may be possible to eliminate voltage imbalance and voltage ringing at the same time.

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