Power-efficient Body Bias Control for Ultra Low-power VLSI Systems

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Abstract

The power consumption of CMOS VLSI is still one of the main concerns for IoT demands. This is because available energy sources might be limited in some cases when the IoT nodes operate with quite tiny batteries (e.g. wearable computing, sensor systems, and health monitoring systems). On the other hand, recent transistors suffer from detrimental effects such as leakage current and process variations. Both of them increase the entire system power and degrade the battery lifetime; thus, they should be efficiently suppressed.

Body bias control is one of the most efficient means to address these issues. It can widely provide an efficient tradeoff between leakage power and gate delay by adjusting the transistor threshold voltages even after chip fabrication. In addition, the body bias effect is further endorsed with the unique transistor structure of Fully Depleted Silicon on Insulators (FD-SOIs). Moreover, this technology provides some good features such as low fabrication cost, high performance, and low-power consumption. Thus, leveraging FD-SOI and body bias control can be an efficient solution for a low power VLSI design.

Despite the advantages offered by body biasing, a crucial design challenge is introduced, namely, how to find the optimal voltage settings (i.e. power supply and body bias voltages). Improper voltage selection might cause excessive current consumption or timing violations. In this thesis, a power optimization methodology obtaining proper voltage settings is proposed and evaluated. Compared to the other conventional studies, the proposed method can improve the power/performance control granularity of body biasing. Since the proposed approach assumes conventional voltage sources, it allows utilizing given voltage regulators more efficiently compared to the conventional methods.

In addition, the overhead incurred by the body bias control has to be taken into account for low power applications. Conventionally, digital-analog converters are often adopted for body biasing because of their fine voltage controllability. However, such analog circuits require a high-power supply voltage and an additional power source, resulting in a considerable power overhead and an increased system cost. When a system needs to operate at a limited power budget such as an order of milliwatt, these factors cannot be ignored. Therefore, in order to achieve a lower power overhead, an on-chip digitally assisted automatic body bias tuning scheme (DABT) is proposed in this thesis. Thanks to the proposed architecture, it can operate even at 0.35V of power supply voltage. A power source for digital circuits can be shared with the proposed body bias controller even when its voltage

is set to a near-threshold region. As a result, the proposed architecture does not require any additional power sources.

These proposed methods are validated with real chips fabricated with the SOTB-65nm technology. The evaluation results show that, when compared to conventional methods, the proposed power optimization can achieve 9.62% of average power reduction reaching up to 22.77% in the case of the V850 microcontroller.

Also, the proposed DABT mechanism can operate with a power overhead which does not exceed a few μW. To the best of the author's knowledge, this is the lowest power overhead among the already fabricated controllers to date.

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1

Introduction

1.1 Low power VLSI system demands

Very Large Scale Integration systems have become primordial for the current human society. For example, when we are relaxing on a couch, we might check a smartphone which is equipped with VLSI chips. Also, when we cook a meal, we might use a rice cooker which is controlled with a microcontroller to regulate the temperature in the pot, depending on the type of rice. Definitely, nowadays human life cannot exist without the great assistance of VLSI systems. In addition, the recent technology trends try to connect physical objects (e.g. household appliances, temperature sensors, biomedical monitors, cars, etc) to the Internet also known as *Internet of Things* (IoT) [1]. Nearly 20 billion IoT devices are connected to the Internet in 2018 and their number will reach 30 billion in 2021 [2] as shown in Fig. 1.1. Needless to say, VLSI systems are indispensable for the IoT nodes to communicate to the Internet. Consequently, the importance of VLSI systems will be more increased in the future.

The IoT trends bring design challenges for low power VLSI systems. For example, regarding sensor network systems, some of the nodes cannot be connected to electrical outlets, thus, have to be driven by batteries. Nevertheless, such applications often require a few years of battery lifetime for each node [3]. In this context, the power consumption of VLSI systems has to be also minimized to satisfy these demands. However, the recent CMOS transistors suffer from their power consumption and fabrication cost as explained in the next section.

1.2 Technology trends of CMOS VLSI

CMOS technologies have been evolving for the last five decades following what is known as Moore's law [4]. The most famous method for the improvement is to shrink the transistor size and decrease the power supply voltage as Robert Dennard proposed in 1974 [5].

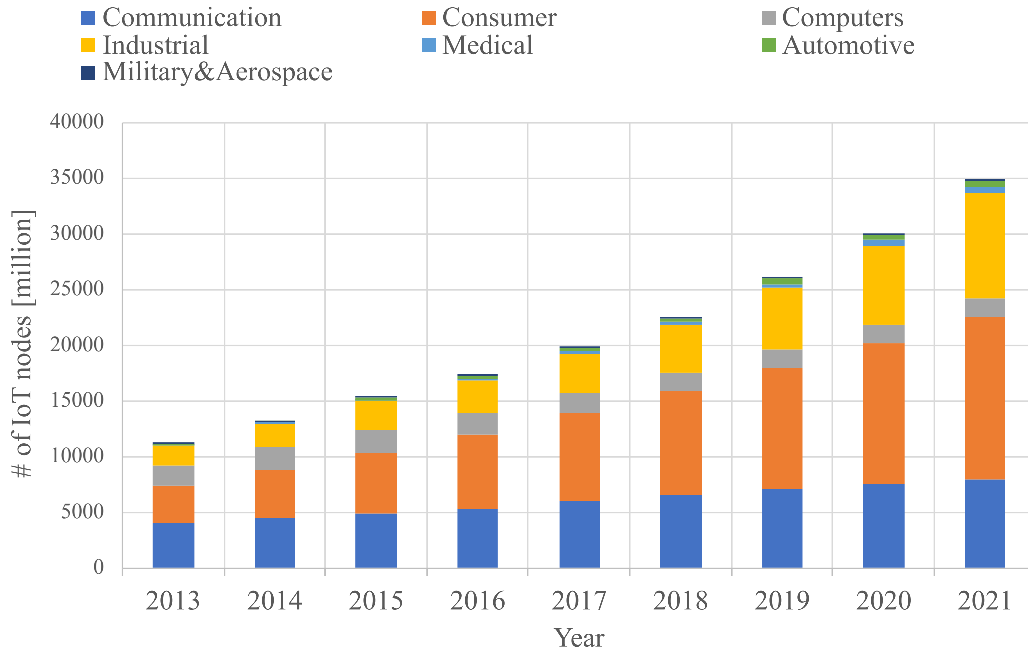


Figure 1.1: The number of IoT nodes

Shrinking the size allows more transistors to be integrated in a chip and reduce the cost per transistor. Also, the used supply voltage can be lowered; thus, the scaling results in lower power consumption. Although the Dennard scaling was over around 2005, the device feature size has kept scaling by employing new device structures. Indeed, the most advanced technologies for recent commercial high-end chips reach around 10-nm to the best of author's knowledge. For example, a 10-nm is adopted in the products shown in [6, 7]. Also, a 12-nm and 14-nm process are adopted in [8] and [9], respectively. These trends will continue to a few nm process generation [10] (Fig. 1.2).

On the other hand, the wafer cost has been also increased as the feature size is scaled. In the case of TSMC processes, the cost of the 16-nm node is about three times higher than that of 130-nm node as shown in [11]. Although the cost per transistor is not increased, the expensive fabrication cost restricts available applications. That is, the recent technologies can only be used for applications which can promise profits overwhelming the initial fabrication cost. Accordingly, they are not suitable for low-end chips (e.g. embedded systems) which require reasonable performance and fabrication cost.

From the above reasons, it has been also discussed how to utilize mature process technology and create new applications. This is because such technologies can be available at a reasonable cost when compared to the case of leading-edge technologies. Nowadays, sub 100-nm process technologies (e.g. 65-nm, 40-nm, 28-nm and so forth) can be used as mature ones, which are dense enough to realize a certain VLSI system in a chip. This trend is called *More than Moore* [12]. Clearly, *More than Moore* is indispensable to realize efficient

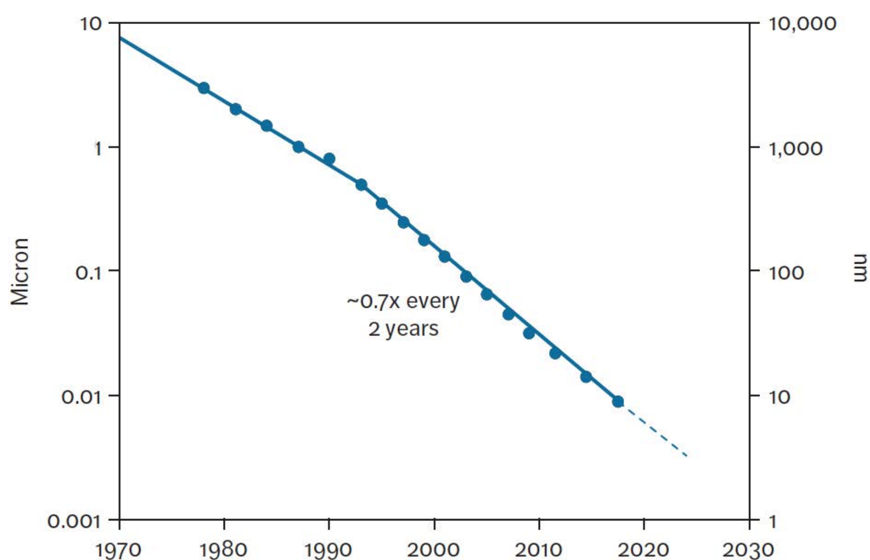


Figure 1.2: Minimum feature size scaling trend for Intel logic technologies [10]

Table 1.1: Leakage current of each process feature size [13]

Feature size [nm]	250	180	130	90	65	45	32
Leakage current [nA/μm]	1	3	100	400	100	100	100

IoT systems from the viewpoint of cost efficiency. However, even if such technologies are used, some detrimental effects should be considered.

1.3 Obstacles for IoT demands

Generally speaking, scaled process technologies suffer from detrimental effects. Leakage current has been one of the burdens for low power VLSI design from the device generation of 180-nm [13]. It consumes unnecessary power even without any computations, thus, degrades the energy efficiency. This effect is amplified when the process technology is scaled. Table 1.1 shows this behavior with the leakage current of each Intel's process node [13]. As can be seen in this table, the 180-nm process node consumes 3 times higher leakage current than the 250-nm node. Moreover, this phenomenon gets drastically worse at the 130nm and more scaled process nodes. In the case of the 45-nm node, 100 times leakage current is consumed when compared to the 250-nm. Consequently, in order to obtain a longer battery life of embedded systems, leakage current has to be reduced efficiently even though mature technologies are used.

Furthermore, characteristics variation of transistors is a thorny problem on the current VLSI designs [13]. This effect is mainly occurred by fabrication mismatches at scaled

process technologies. Therefore, even if each chip is designed with a typical transistor parameter, an actual one might have different delay and power behaviors. This problem is known as the process variation. For example, some chips might violate delay constraints, while the other might consume too much power. That is why, in order to avoid such situations, VLSI design should be conducted by considering the worst case. However, the worst case condition rarely appears, and a design optimized for such case is too conservative in most cases. As a result, process variation degrades the energy efficiency of almost all of the fabricated chips.

1.4 Design challenges

How can we suppress the leakage current and process variation? Body bias control (BBC) can be an efficient solution to suppress these issues. As explained later, the BBC has an exponential dependency on the leakage current. Hence, the leakage current can be efficiently reduced [14–16]. Also, since the BBC can adjust the threshold voltage of a transistor after chip fabrication, the transistor characteristics variations can be well managed [17–19]. Moreover, the body bias effect is further endorsed by a unique transistor structure of Fully Depleted Silicon On Insulator (FD-SOI), which provides low fabrication cost, high performance, and low power consumption compared to the conventional bulk technologies [20, 21]. Thus, leveraging the FD-SOI and BBC is an efficient solution for low-power VLSI designs.

Despite the advantages of the BBC, their voltages should be carefully controlled. This is because the BBC has a trade-off between the leakage current and gate delay. Regarding a real application, sometimes a system needs to perform computations (active state), sometimes it is in a standby as depicted in Fig. 1.3. At the standby mode, the lowest leakage (but slow) states can be used because the target system is not operating. Thus, body bias voltages for the standby state can be realized with a simple mechanism [16]. On the other hand, when a system needs to operate at a given performance requirement, appropriate body bias voltages have to be supplied. Otherwise, improper body bias selection might cause excessive leakage current or timing violations. Moreover, required performances can be different according to application demands, which obligates to enable various voltage levels. The voltage control for the active states becomes more complex than that for a standby state. Consequently, it is challenging to realize power efficient BBC, especially for active states.

For the sake of an efficient BBC, we have to consider how to find and generate appropriate body bias voltages. Conventionally, such voltages are decided by optimizing a target system power consumption [15]. Nevertheless, these power optimization methods cannot fully utilize the BBC efficiency. This is because they restrict available voltage patterns as explained later. Less voltage choice causes less performance/power control granularity; thus, the power efficiency of the BBC can be degraded. Power and system-cost overheads of body bias generators are also an important concern for low power VLSI design. Traditionally, digital analog converter (DAC) based designs are used for body bias controllers because of their fine voltage controllability. They can enable sophisticated BBC algorithm as shown in [15, 22]. However, considering the IoT usage, overheads derived from DACs cannot be ignored. In addition, recent low power digital systems often operate at near

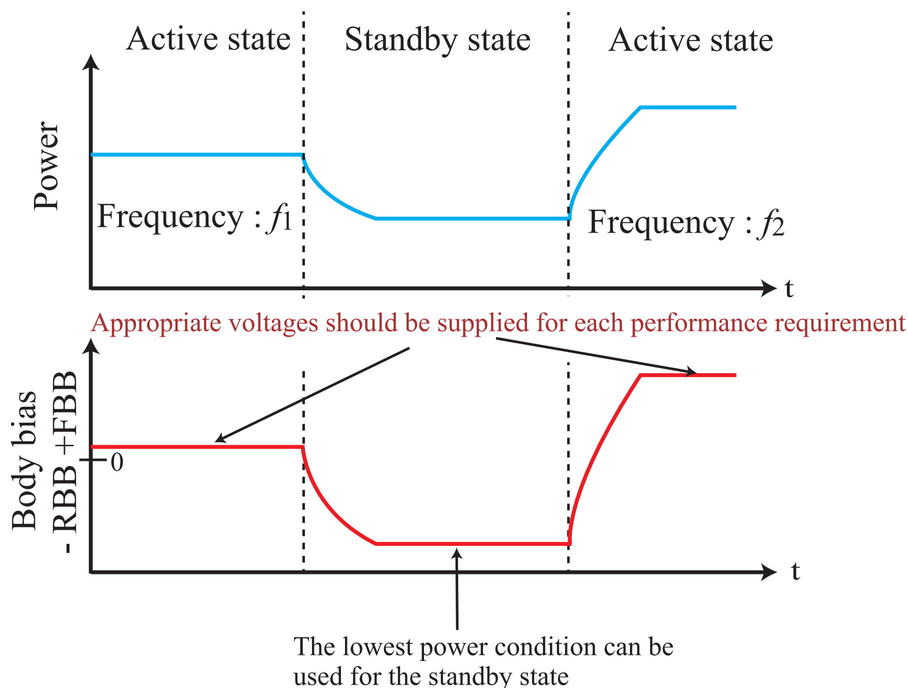


Figure 1.3: Conceptual waveform of the BBC

threshold voltages [23, 24]. This means that a voltage gap between analog and digital circuits becomes wider. Sharing the power supply for digital circuits is not a practical way for analog circuits in this situation. As a result, an additional power source is required for the body bias controller, which increases entire the system cost.

Regarding the above issues, in this thesis, an efficient power optimization methodology and body bias tuning scheme are proposed and evaluated. An overview of the proposed approaches is described in the next section.

1.5 Overview of the proposed approaches

1.5.1 Power optimization

The proposed power optimization is aiming for maximizing the power efficiency with a general body bias scheme. This is achieved by expanding the search area which the conventional methods have often ignored. Some conventional methods can only consider the "symmetric" body bias condition that the biases for both nMOS and pMOS are always set to the same degree for making the optimization easy. Although this simplicity allows realizing on-chip optimization algorithms as reported in [15,22], the search space for the conventional optimizations is intrinsically limited. Similarly to the aforementioned works, [25] cannot distinguish the body bias voltage of nMOS and pMOS. Also, considering practical BBC schemes, VLSI chips have a certain limitation derived from the available voltage sources. Besides the "symmetric" constraints, such limitation significantly degrades the number of

available voltage combinations; hence, it leads to less efficient performance/power control granularity. Regardless whether the used body bias voltage between nMOS and pMOS is the same degree ("symmetric") or not ("asymmetric"), the voltage combination that can achieve the lowest power consumption at a required frequency should be used. Therefore, the proposed approach can take the "asymmetric" body bias conditions into account.

However, when considering to use the asymmetric body bias combinations, the optimization becomes more complex due to the increasing number of voltage candidates. Moreover, the power optimization should also consider the power supply voltage [26]. Regarding this search space, brute force search [27] with real chip testing is not a practical way. Therefore, an effective power optimization methodology that can treat these problems simultaneously is required. Although there are studies treating "Asymmetric" voltage combinations [18], it does not consider both the power supply and body bias voltages, simultaneously.

The contributions of this thesis about the power optimization are listed below:

- Power and delay models are proposed for the power optimization. The proposed models can consider the power supply voltage and asymmetric body bias combinations simultaneously. Since the proposed models are based on real chip characteristics, the error is minimized to a few percents.

- Based on the proposed model, a power optimization methodology is introduced and evaluated. Unlike conventional brute force search techniques, the proposed model can reduce the number of testing points.

- Since the delay from the models and real chips might slightly differ from each other, the proposed optimization also includes an error compensation technique which makes sure that a target system can operate with the obtained body bias voltages. It is also demonstrated that this error compensation technique can be implemented as a lightweight on-chip body bias controller to further suppress the testing cost.

- In order to observe its efficiency, the proposed optimization is evaluated with two different types of real microprocessor chips. These chips are implemented with a 65-nm FD-SOI technology. The evaluation results show that the proposed method can actually reduce the power consumption by up to 22.77% when compared to conventional symmetric body bias conditions.

1.5.2 Body bias controller

The proposed body bias controller adopts DAC-less design strategy to pursue a small system overhead. This is inspired by a *Digitally Assisted Analog Circuits*, which is promising for low power VLSI design [28–30]. The main idea here is to achieve analog functionalities by using digital circuit components. Such a fashion enables a lower power supply voltage even for an analog functionality because digital circuits can operate at a lower voltage than analog ones. By exploiting these benefits, the power supply voltage for a body bias controller can also be lowered to the near-threshold region; hence, the power overhead can be drastically reduced. In addition, the proposed controller can share the same supply voltage with digital

circuits, thus, does not require any additional power source. This feature contributes to reduce the entire system cost.

The contributions regarding the body bias controller are as follows:

- An on-chip "Digitally-assisted Automatic Body-bias Tuning" (DABT) scheme is proposed and implemented. DABT can control the body bias voltages without the need for analog DAC components. This can be achieved by checking the delay information of a target system and directly controlling the body bias accordingly. In other words, DABT can automatically control the body bias voltage according to the system performance demands.

- In order to prove the DABT concept, a test chip prototype is fabricated with 65-nm FD-SOI technology. Real chip experiments showed that DABT can even operate at 0.35V of supply voltage and 70°C of chip temperature. To the best of the author's knowledge, DABT achieves the lowest power overhead when compared to the already proposed schemes.

- The leakage reduction efficiency is simulated with a MIPS R-3000 subset processor. The simulation results show that, even when the processor suffers from large leakage current due to the process variation, DABT can efficiently suppress the leakage current.

1.6 Outline of this thesis

The rest of this thesis is organized as depicted in Fig.1.4. In chapter 2, technical backgrounds for low power VLSI design are firstly introduced. For example, What is the body bias control? How to control it? Is there any research about it? These preliminaries are summarized in this chapter. Then, in order to explore more efficient BBC and obtain research queries, previous studies are deeply reviewed in chapter 3. According to the arguments in chapter 3, a power optimization methodology is proposed and evaluated in chapter 4. Also, an ultra-low overhead body bias controller is introduced in chapter 5. Lastly, obtained observations from this thesis are briefly summarized and possible future work is shared in chapter 6.

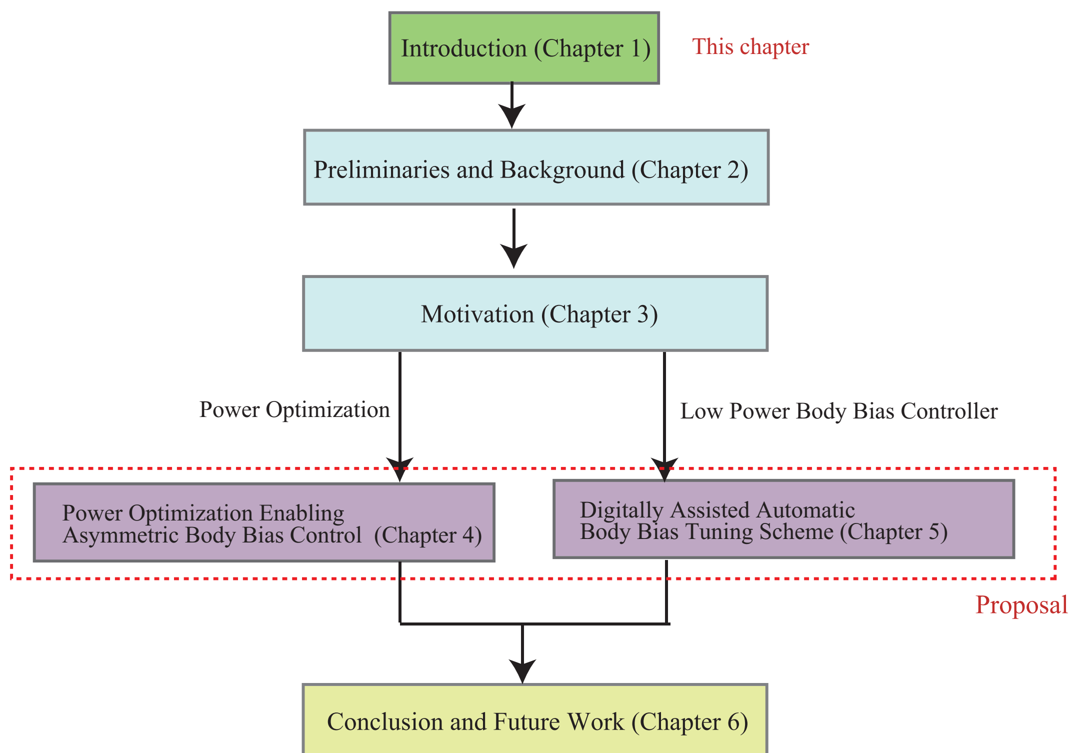


Figure 1.4: Thesis structure

2

Preliminaries and Background

2.1 System on Chip

Thanks to the CMOS scaling, various kinds of circuitries can be integrated on a chip. Such systems are referred to as System on Chip (SoC). In [31], *Tummala et al.* define SoC as: *"We define an SoC as the realization of an entire system's functionality in a single, large IC (with process compromises to accommodate various macros and technologies). This IC integrates digital, RF, analog, and other functions."* As shown in some works [24, 32–37], recent SoCs still have similar configurations with this definition. In order to clarify the target of this thesis, recent low-power SoCs are firstly reviewed.

In [24], *Pu et al.* report the *Black ghost* SoC, one of the Qualcomm products, for IoT usage. This system is implemented with the TSMC 28-nm CMOS technology. Fig. 2.1 depicts a simplified block diagram of it. It includes a sensor control processor (ARM Cortex™-M0), energy efficient accelerators for specific applications (e.g. face recognition, voice word detection, etc), an analog front end (AFE) for sensing, a power management unit (PMU), a clock generation unit, and peripherals. The AFE is implemented as a sensor peripheral. It is composed of a low-noise sense amplifier buffer and 12-bit Analog Digital Converter (ADC). The M0 processor can process the input data from the AFE according to the timing defined by a software. Also, since recent complex applications (e.g image processing) require both high speed and low power computation, the data from AFE can be offloaded to the accelerators according to application requirements. The power consumption of these digital components can be tuned by the on-chip PMU. Moreover, all the power domain, except the always-on (AON) part, can be cut-off with on-chip switches. As a result, this SoC can be driven by a tiny Li-Ion battery.

From Intel, *Karnik et al.* disclosed a self-powered IoT edge SoC in 14-nm Tri-Gate CMOS technology [33]. Fig. 2.2 describes a conceptual block diagram of this SoC. It integrates an x86 host application processor, a convolutional neural network (CNN) accelerator for visual recognition and classification, a crypto engine for secure boot and data transmis-

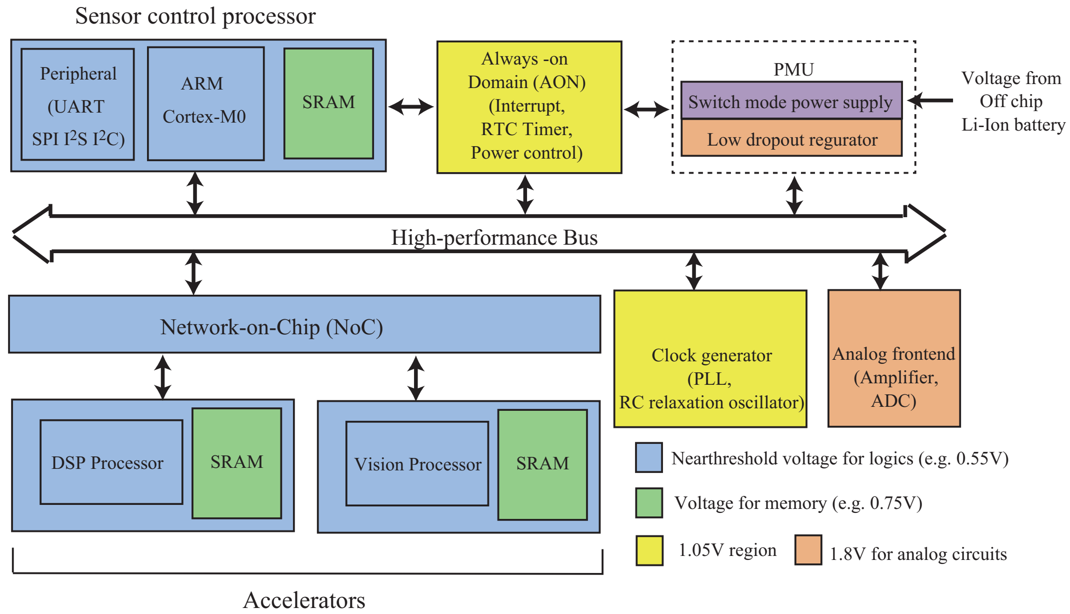


Figure 2.1: Simplified block diagram of *Black ghost* architecture

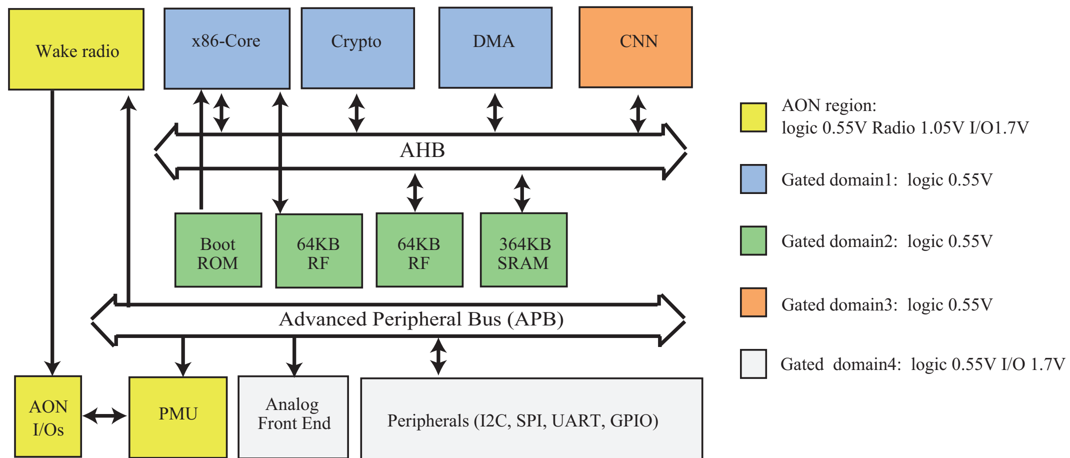


Figure 2.2: Simplified block diagram of the self-powered IoT edge from Intel

sion among IoT nodes and gateways, a sub-mW radio receiver for the control signals from IoT gateways, an analog front end, 512KB shared memory, and on-chip power management unit. Similarly to the *Black ghost* SoC, the x86 processor and accelerators can treat the data from the AFE. Also, since CNN is one of the promising techniques for energy efficient and high-performance image processing, it is implemented as the accelerator. Moreover, the equipped crypto engine can protect each IoT edge from malicious network attacks. At the active state of the SoC, the sensor, image data capture, image recognition/classification, or BLE transmission can be conducted. On the other hand, at the standby mode, all of the

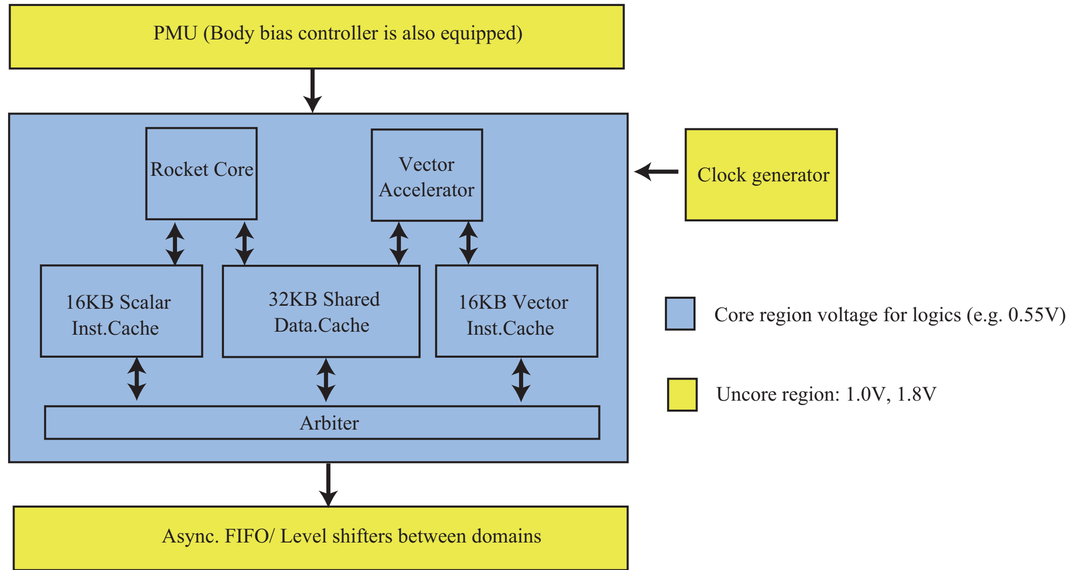


Figure 2.3: Simplified block diagram of the RISC-V SoC

subsystems, except the AON part, can be power-gated with the PMU. As a result, this platform can perform an image capture application with 24mW of the power consumption at maximum, which can be driven by a tiny battery.

Keller et al. reported a RISC-V processor SoC in 28-nm FD-SOI CMOS technology [35]. Fig. 2.3 shows a block diagram of the RISC-V SoC. *Rocket*, which is a 64-bit in-order single-issue processor supporting open RISC-V instruction set, is adopted. Also, a vector accelerator is implemented for compute-intensive workloads. Although this SoC does not include an AFE which can connect to off-chip sensors, an on-chip power management, and clock generator unit are integrated. The power management unit of this SoC can tune the processor's body biases and power supply voltage.

In [36], a fully integrated battery-powered system-on-chip in 40-nm CMOS, named *Brain SoC*, is reported. This SoC is used for controlling an insect-scale pico-aerial vehicle (Fig. 2.4). For such applications, low-power VLSI systems are important because available power budget is quite restricted. Indeed, a take-off mass of a tiny aerial vehicle is poor, thus, a tiny battery can be available. The *Brain SoC* is composed of general-purpose cores (Cortex M0 and Siskiyou Peak), accelerators (for Convolution filter and image interpolation optical flow(IIOF)), a digital signal processing (DSP) unit, memory components, on-chip voltage regulators, I/Os, ADCs, and an actuator controller for pico-aerial vehicle's wing. To perform efficient computations, a heterogeneous architecture is adopted like the other SoCs. The accelerators and DSP can be accessed by the general-purpose cores via the memory mapped registers. According to the computation results from these components, the actuator controller outputs control signals. The on-chip voltage regulator down-converts the battery output voltage because it is much higher than the maximum available voltage for the on-chip transistors. The core and accelerators can operate with 7.5mW of power consumption at 0.63V of power supply voltage. Nevertheless, the leakage current occupies

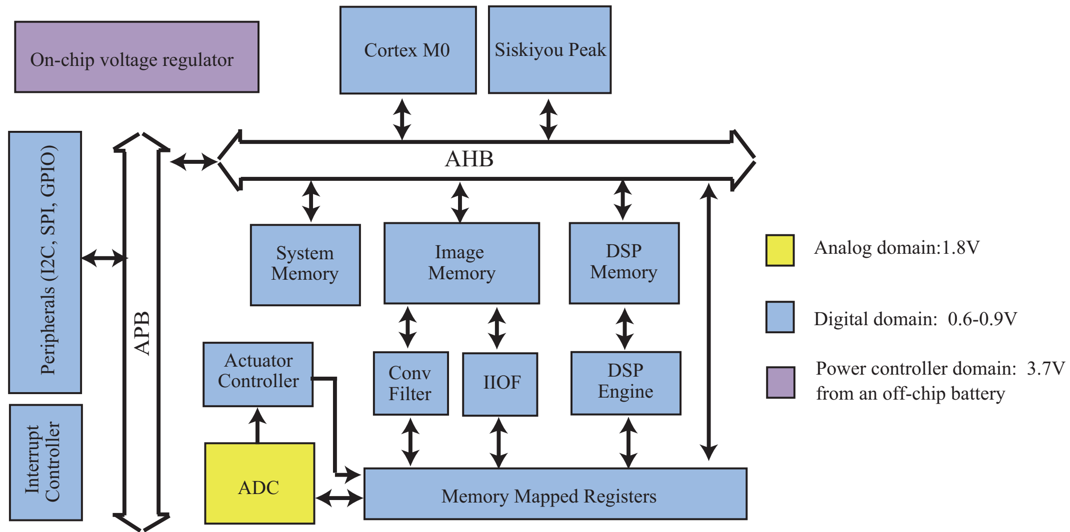


Figure 2.4: Simplified block diagram of the BrainSoC

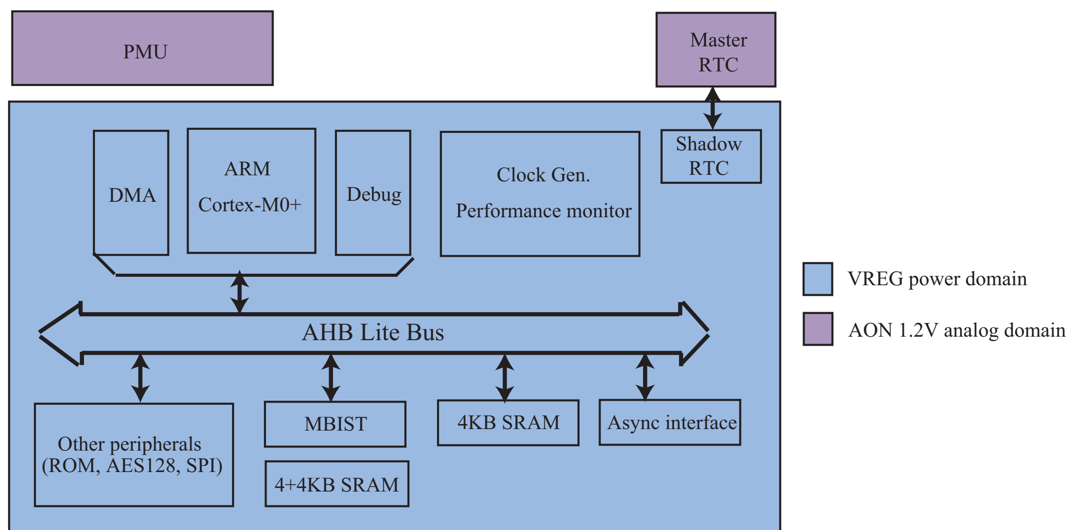


Figure 2.5: Simplified block diagram of the near threshold SoC in [37]

the large portion of the total current (3.3mW at this condition).

The work presented in [37] reports a tiny microcontroller in 65-nm CMOS for IoT applications (Fig. 2.5). This SoC consists of a CPU (Cortex-M0+ including DMA controller), 12KB RAM, a clock generator, a performance monitor, a PMU, and peripherals. As can be expected by the implemented computation budget, target applications of this SoC are smaller than those of the other SoCs reviewed so far. Nevertheless, the on-chip configuration is adopted for the PUM. The PMU can dynamically control the power supply voltage for the VREG power domain, shaded in blue shaded in Fig. 2.5. The VREG voltage domain

is divided into 16 power sub-domains for flexible voltage control. This SoC also enables a power gating technique similarly to [33]. By utilizing the dynamic voltage/frequency control and the power gating, the energy efficiency of this SoC is much improved. Indeed, the average power consumption with the low-power IoT workloads (EEMBC's ULPBench) is 1.01μW.

Firstly, we can notice that matured process technology is actually used for embedded VLSI systems as stated in the trend of *More than Moore*. In fact, the studies in [36] and [37] respectively adopt 40-nm and 65-nm technologies even though more scaled ones are available. Nevertheless, as briefly explained in the previous chapter, these mature technologies are scaled enough to cause some detrimental effects such as leakage current and process variation. Also, according to the transistor scaling trend, smaller feature size technologies than 28-nm can be considered as mature in the future. Indeed, a 14-nm process technology has actually matured; thus, the work [33] adopts it. From this context, the detrimental effects caused by the scaling will be a more fatal problem for low-power VLSI designs. Therefore, an efficient way to suppress these effects is required.

Also, some of the recent SoCs are often equipped with large computation systems (i.e. a processor + accelerators) even for embedded systems. Needless to say, integrating more transistors causes more leakage current. In addition, when VLSI systems operate, the dynamic power is consumed as explained later. Larger computation resource incurs larger dynamic power similarly to the leakage current. Therefore, the power management for recent VLSI systems needs to consider not only the leakage but dynamic power as well. Note that, regarding the reviewed SoCs, the power management should be integrated inside a chip.

2.2 Power consumption on CMOS VLSI

In order to discuss how to control the VLSI power efficiently, we need to know its basic characteristics. Generally speaking, the power consumption of CMOS VLSI is composed of the dynamic (P_{dy}) and static power (P_{st}) as follows:

$$P_{total} = P_{dy} + P_{st} \tag{2.1}$$

The dynamic power is consumed by charging and discharging parasitic capacitors for signal transition as depicted in Fig. 2.6 (a). On the other hand, the static power is consumed by the leakage current even when the transistor is cut-off. These two power phenomena have different characteristics; therefore, the characteristics of the dynamic power are firstly explained hereafter.

2.2.1 Dynamic power

As briefly explained, the dynamic power is caused when MOSFETs charge/discharge parasitic capacitors. The current consumption here is referred to as switching current. Therefore, similarly to the equations for charged energy at capacitors, the power consumption from switching current can be formulated as:

$$P_{sw} = (\alpha_{at} C) f V_{DD}^2. \tag{2.2}$$

Here, α_{at} is switching activity, C is capacitance, f is operational frequency, and V_{DD} is power supply voltage. Also, the dynamic current includes internal the short circuit current, which flows from the power supply terminal to ground when the input signal transits and weakly turns-on both nMOSFET and pMOSFET. The dynamic power is inevitable for computation. Also, higher switching activity incurs higher power consumption. Therefore, the large VLSI systems such as [24, 33, 35] suffer from large dynamic power.

The dynamic power consumption can be suppressed by lowering the power supply voltage as depicted in Fig. 2.7 (a). Nevertheless, as explained later, there is a trade-off between the gate delay and power consumption when controlling the voltage. This trade-off makes the voltage control complex.

In the next subsection, the characteristics of the leakage current are explained.

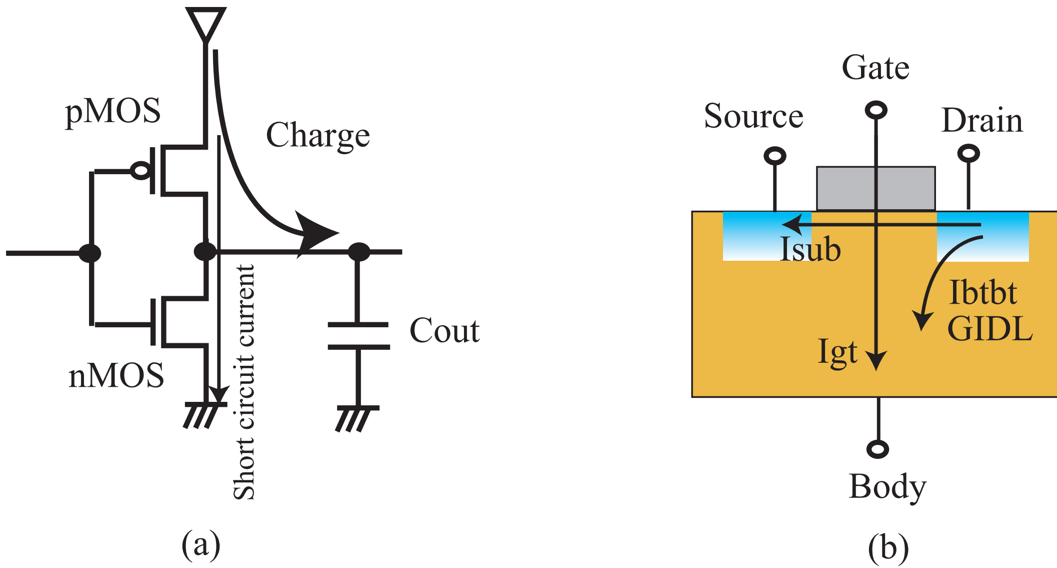


Figure 2.6: Power consumption on CMOS VLSI (a) Dynamic current (b) Leakage current

2.2.2 Static power

The so-called "static power" is caused by the sub-threshold leakage current, gate leakage current, gate induced drain leakage (GIDL) and p-n junction leakage current in MOSFETs [13] (Fig. 2.6 (b)). These can be ignored before the technology nodes of 250nm. However, from the node of 180nm, their effects are drastically strengthened and have to be taken into consideration.

Sub-threshold leakage (I_{sub}) is a drain-source current even when a transistor is at a cut-off state. Unlike the current at a super threshold region dominated by the drift effect, I_{sub} is caused by diffusion current [38]. (I_{sub}) can be formulated by the following equation:

$$I_{sub} = I_{off} 10^{\frac{V_{gs}+\eta(V_{ds}-V_{DD})+K\gamma V_{sb}}{S}} (1 - e^{\frac{-V_{ds}}{v_T}}) \tag{2.3}$$

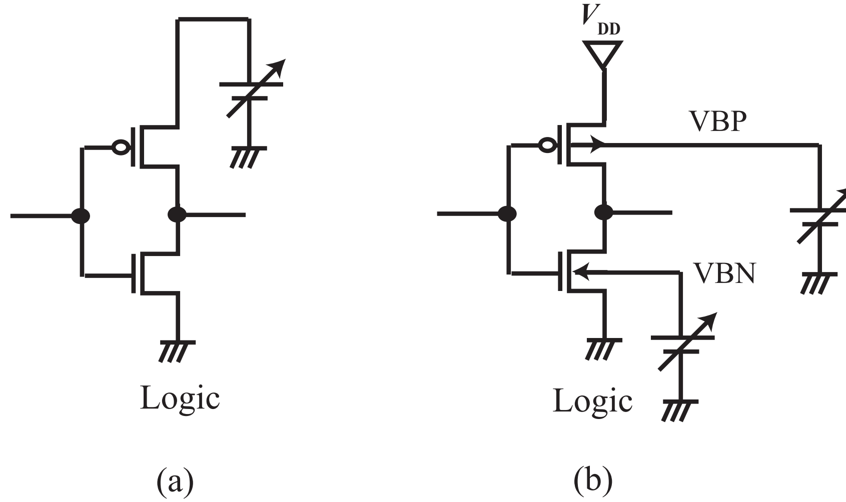


Figure 2.7: Voltage control technique: (a) Power supply control (b) Body bias control

Where I_{off} is the sub-threshold leakage current at V_{ds}=V_{DD}, V_{gs}=0V, and zero bias. v_T is the thermal voltage, η is the DIBL coefficient, K_γ is the coefficient of body bias controlling, and S is the sub-threshold slope [13].

The gate leakage current (I_{gt}) is caused by the tunnel effect. That is, the electron in the gate terminal is released to the channel if the gate oxide is very thin. (I_{gt}) can be represented as:

$$I_{gt} = WP_A(\frac{V_{DD}}{t_{ox}})^2 e^{-P_B \frac{t_{ox}}{V_{DD}}} \tag{2.4}$$

where t_{ox} is the thickness of the gate oxide, W is the gate width, and P_A and P_B are constants determined by the process technology [13].

The pn-junction leakage current is observed at the parasitic diodes in a MOSFET. Although this leakage current is not a serious problem in most cases, it cannot be ignored at the drain terminal because of its high impurity density. The high density causes a band to band tunnel current (I_{BTBT}). I_{BTBT} can be formulated as:

$$I_{BTBT} = WX_j P_1(\frac{E_j}{E_g})V_{DD} e^{-P_2 \frac{E_g^1.5}{E_j}} \tag{2.5}$$

where X_j is the junction depth of the diffusion, E_g is the bandgap voltage, E_j is the electric field along the junction, and P_1 and P_2 are technology constants [13].

GIDL occurs at a drain-gate overlap region when the gate is biased to form an accumulation layer at the silicon surface. This current is increased by the large potential difference between gate and drain because it enhances the electric field. As a result, a band-to-band current flows from the drain terminal.

In some cases, leakage current might occupy a large portion of the VLSI power consumption. For example, Fig. 2.8 show the breakdown of the power consumption of a real chip processor V850 fabricated with SOTB 65-nm CMOS technologies [39]. As can be seen from the graph, the leakage current consumes 64.6% of the power consumption in the

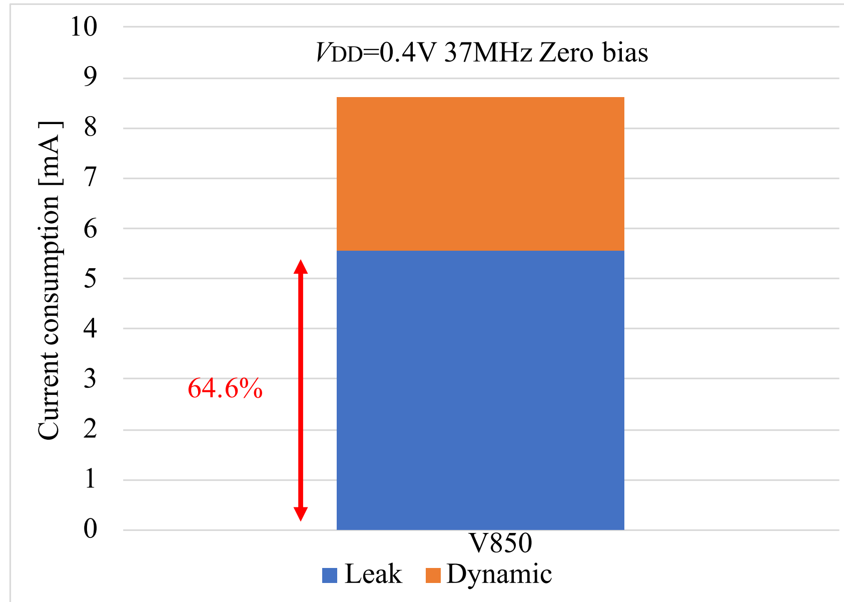


Figure 2.8: Break down of the power consumption

case of V850. In other words, the great portion of the power is wasted at V850; thus, an efficient solution to reduce the leakage current is required.

It is important to mention that using low-leakage devices (e.g. long-channel devices) is not the panacea for all low-power applications. This is because such transistors often require high V_{DD} voltages. This incurs larger dynamic power consumptions as depicted in equation (2.2). Also, the mandatory use of a high V_{DD} can limit the number of potential target applications. For example, bio-sensor platforms sometime need to operate under the power budget of biofuel cells, which can output around 0.4V as depicted in [40]. This voltage region is too low to adopt low-leakage devices. Therefore, it is still necessary to develop leakage reduction techniques for leaky process technologies.

It is also worth noting that power gating (PG) is one of the most well-known leakage reduction techniques. The essential idea of PG is to turn-off unused circuits with switch transistors as depicted in Fig. 2.9. Since the off resistance is much increased due to the switches, the leakage current can be drastically reduced when a target system is in a standby state. Nevertheless, this technique clearly cannot be used for active state circuits because the power supply is disconnected. Therefore, the PG cannot also be the solution for all low-power applications.

2.2.3 Power and delay trade-off

Contrary to PG, lowering the power supply voltage can reduce both of the leakage and switching current at an active state. That is why, recent SoCs often operate at a near threshold voltages [23,24,33,35]: At a conventional voltage region, around 1.0 V of power supply voltage is used, while it is decreased to roughly 0.5V in the near threshold voltage region.

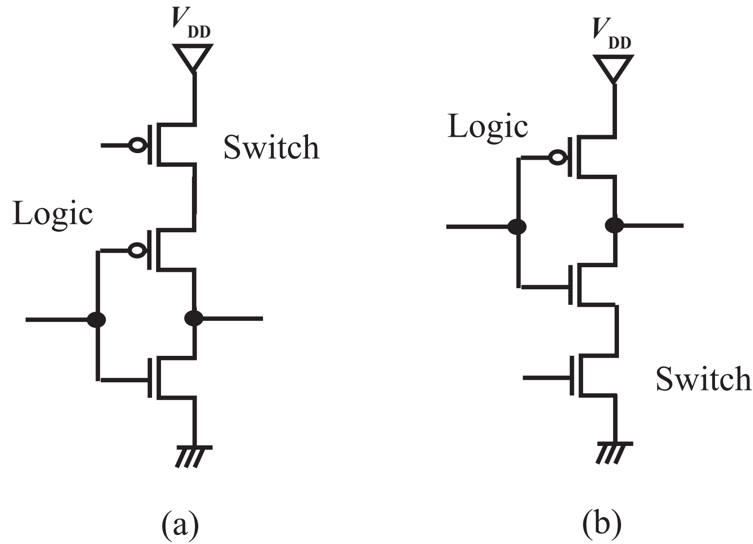


Figure 2.9: Power gating: (a) header switch (b) footer switch

Nevertheless, when the power supply is controlled, the gate delay should also be taken into consideration as can be seen in the alpha power law [41]. In this law, the delay is given by:

$$t_d = x \frac{V_{DD}}{(V_{DD} - V_{TH})^{\alpha}} \tag{2.6}$$

where x is a process parameter and α is a parameter for velocity saturation at high V_{DD}. Since α is from 1 to 2, we can notice that lower voltages cause large gate delays. The trade-off between the power and gate delay can be graphically understood with Fig. 2.10, which depicts the V_{DD} dependency to the power and delay of an inverter gate implemented with SOTB 65-nm technology.

For a standby state of VLSI systems which does not require any computations, a very low-power (and slow) state can be used. On the other hand, for an active state where a given VLSI system has to operate at a certain frequency, its voltage has to be carefully chosen. Otherwise, considering the trade-off, excessive power is consumed.

On the condition that the trade-off is utilized properly, the VLSI power consumption can be drastically reduced by adopting dynamic voltage and frequency (DVFS) scaling. That is, according to various performance demands, the supplied voltage and frequency are adaptively scaled. The power management units in [24, 35] enable DVFS. For example, in [35], the power supply voltage level can be selected from the four values. Also, the *Black ghost* SoC [24] enables the voltage control with 12.5mV of the voltage step.

In addition to the power supply voltage control, body bias control (BBC) can also realize a trade-off between the standby power and gate delay. Although the required power management becomes more complex, the energy efficiency of VLSI systems can be much improved by adopting both power supply and body bias control.

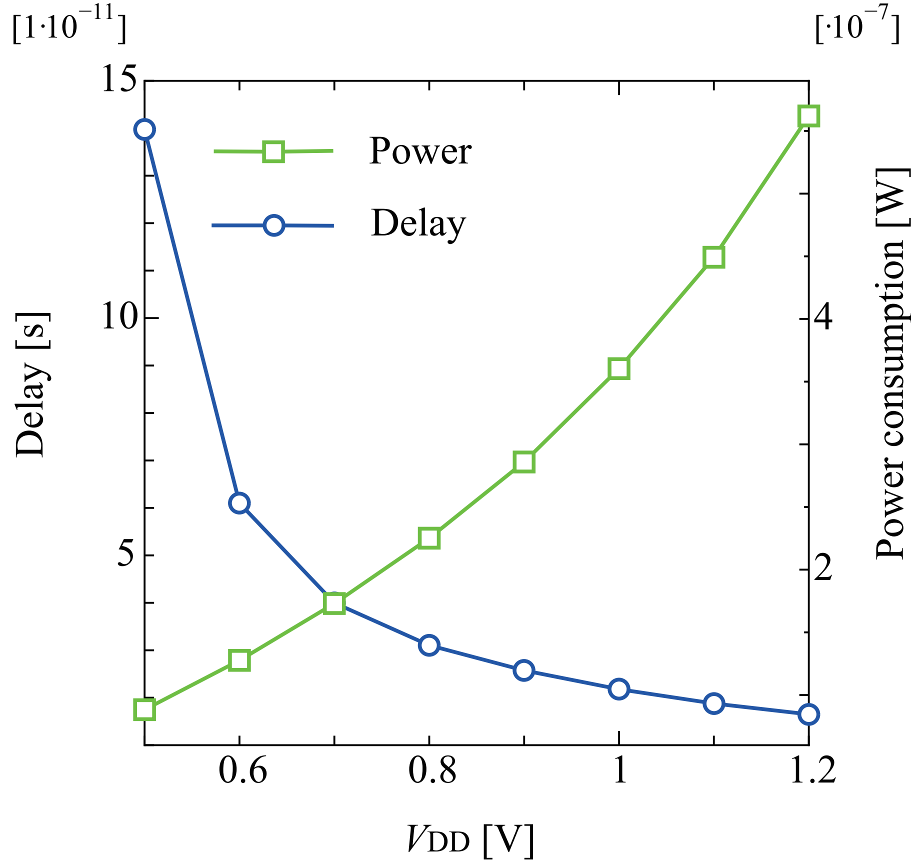


Figure 2.10: Trade-off between the power consumption and gate delay ($f = 200MHz$)

2.3 Body bias control

BBC consists of manipulating the body voltages (See Fig. 2.7 (b) and Fig. 2.6 (b)) of a MOS transistor to adjust its threshold voltage after chip fabrication. In order to control the body voltage, additional layers called "well" are added between the substrate and transistor.[1] Therefore, BBC controls the voltage of well layers.

V_{TH} is defined as the gate voltage which can achieve $2\Phi_B$ of the silicon surface potential. Here, Φ_B is the difference between Fermi potential and intrinsic potential [38]. Considering the MOSFET structure, when the well voltages of MOSFETs are controlled, the potential of the silicon surface is affected, hence, V_{TH} can also be changed. V_{TH} is formulated as:

$$V_{TH} = V_{t0} + \gamma(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}) \tag{2.7}$$

where V_{t0} is the threshold voltage when the source-body voltage (V_{sb}) is 0, and γ is a

[1]The well is conventionally used for optimizing impurity density. But, it can also be exploited for insulating the body of MOSFETs from p-substrate.

Table 2.1: Summary of body bias control

	pMOSFET	nMOSFET	Effect
Reverse bias	V_S <VBP	$V_S >$ VBN	Low leakage & Low speed
Forward bias	V_S >VBP	$V_S <$ VBN	High speed & High leakage
Zero bias	V_S=VBP	V_S = VBN	Normal threshold voltage

coefficient for the body bias effect. Here, ϕ_s is

$$\phi_s = v_T ln(\frac{N_A}{n_i}) \tag{2.8}$$

where N_A is the doping level in the channel, and n_i is the intrinsic carrier concentration in undoped silicon.

As depicted in equation (2.3), the body voltage affects the sub-threshold leakage current. This makes a trade-off between the leakage current and gate delay. From the viewpoint of this trade-off, the BBC can be categorized into three states. When the well voltage for nMOS (VBN) is lower than the source voltage and the well voltage for pMOS (VBP) is higher than the source voltage (V_{Sp}), V_{TH} is increased. This state is referred to as Reverse Body Bias (RBB). RBB can suppress the sub-threshold leakage current at the cost of the gate delay. On the other hand, when VBN (VBP) is higher (lower) than V_{Sn} (V_{Sp}), V_{TH} is decreased. This state is called Forward Body Bias (FBB). FBB can reduce the gate delay; but, the leakage current is exponentially increased. When the body bias is shorted to the source voltage, V_{TH} does not shift from a nominal voltage decided by the manufacturing process. This state is called zero bias. Fig. 2.11 shows the trade-off which is obtained by an inverter cell simulation with SOTB 65-nm technology. In this graph, we assume that the supplied body bias is set to the same magnitude between nMOS and pMOS. When 0.2V of FBB is supplied, the gate delay is reduced by 16.8% compared to the zero bias condition; but the leakage current is 2.68 times higher. While 0.5V of RBB can decrease the leakage current by 88.0%, the gate delay is stretched 1.61 times. Conventionally, BBC has been adopted to reduce the leakage power [14, 15] and improve system performances [42].

Similarly to the power supply voltage control, when a system is in a standby mode, a strong reverse bias can be applied to reduce the leakage current. On the other hand, when a system needs to operate at a certain performance, the body bias voltages have to be also carefully chosen for each performance requirement.

For low-power VLSI designs, utilizing BBC has become more important because novel Fully Depleted Silicon on Insulators (FD-SOI) can enhance the body bias effect as discussed in the next section.

2.4 Fully Depleted Silicon on Insulator

As the name suggests, FD-SOI is formed on an insulation layer and its transistor body is fully depleted. Recent FD-SOIs enable BBC as observed in UTBB [20, 43] and SOTB [21, 44] technologies because the nMOSFET and pMOSFET are formed on the ultra thin

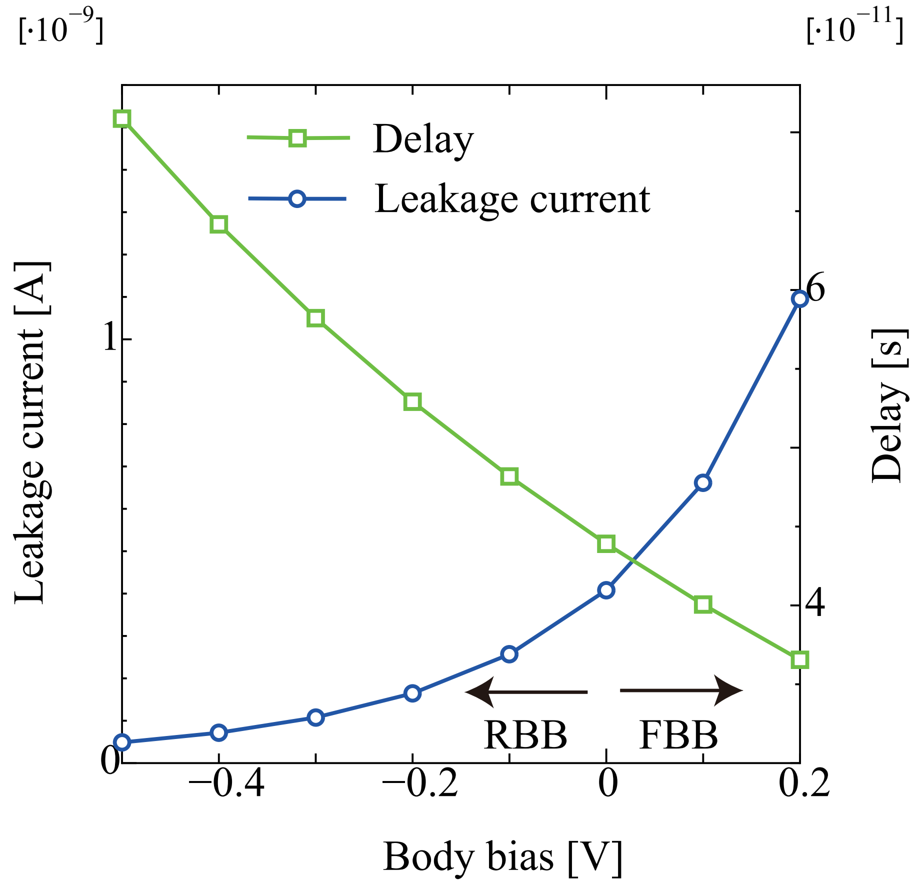


Figure 2.11: Body bias effect simulation.

BOX layer (Fig. 2.12 (a)). Although the conventional bulk technology suffers from the p-n leakage current between the drain and source to the body, the BOX layer can remove it. Consequently, it ensures higher leakage reduction and more efficient body bias control than other conventional MOSFETs.

Thanks to the advantage of body biasing on FD-SOI, a lot of research have been conducted to exploit its benefits. For example, the RISC-V SoC [35] explained in the early part of this chapter is equipped with a body bias controller. Thanks to the BBC, the maximum operational frequency of this SoC (0.9V of V_{DD}) is improved from roughly 500MHz (zero bias) to 600MHz (1.0V of FBB). Also, in [45], a DSP is implemented with 28-nm FD-SOI technology. It achieved 460MHz at 0.397V of V_{DD} and 2V of FBB. In other words, even with a near threshold voltage is used, roughly 500MHz of operational frequency can be performed with the body bias. FBB is also effective for a super threshold region such as 1.2V. In fact, an ARM Cortex™A9 processor fabricated with a 28-nm FD-SOI technology achieved 2.6GHz of operational frequency at 0.6V of FBB. Moreover, as observed in [16] which is based on 65-nm FD-SOI technology, strong reverse bias is utilized. The implemented microcontroller in [16] recorded 140nA of sleep current at 0.35V of V_{DD} and 2.5V

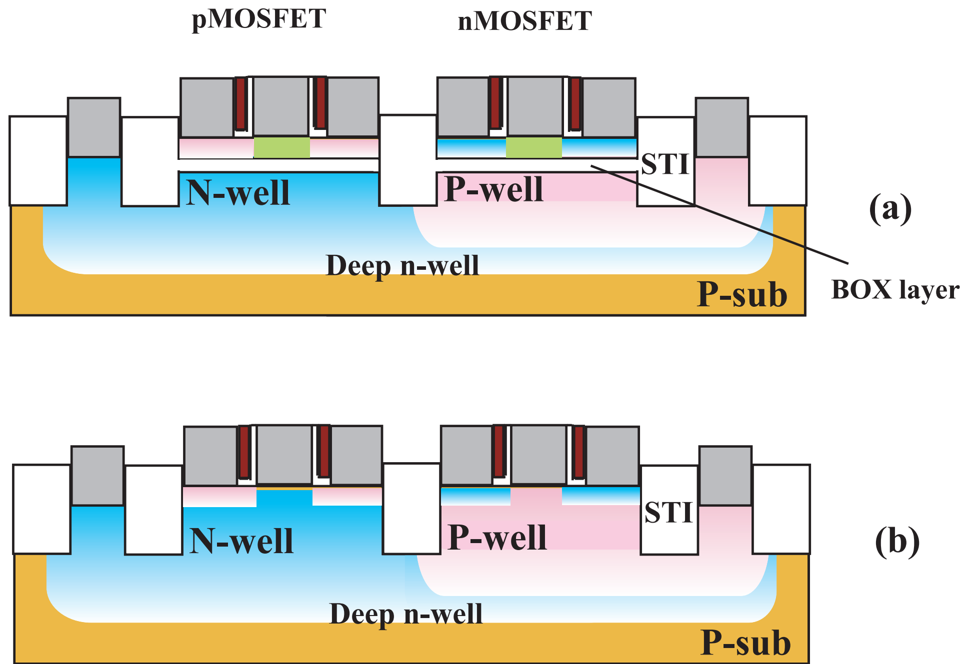


Figure 2.12: Cross-sectional view of MOSFET: (a) FD-SOI (b) Bulk.

of RBB. In addition, by appropriately considering the trade-off between the power and delay, the operating energy efficiency can be improved. In [46], an accelerator implemented with 65-nm FD-SOI technology achieved 192MOPS(Mega Operations Per Second)/mW.

In addition to the advantages obtained with BBC, the FD-SOI structure can adopt a dopantless technique for the channel because the device scaling of FD-SOIs is dominated by the thickness of the transistor body on the insulator [38]. This dopantless strategy can suppress the variation when compared to the conventional bulk technologies as explained later. However, the process variation problem still remains even when the FD-SOI technologies are used. The next section is dedicated to explore the characteristics of the process variation.

2.5 Process variation

Even if a chip is designed with certain parameters, fabricated one might have different characteristics. This fabrication uncertainty is also an obstacle to recent scaled process technologies because it degrades both chip yield and energy efficiency of VLSI systems. In order to understand why it degrades the energy efficiency, we consider, for example, that a huge number of chips are fabricated with a certain design and they should operate at a given performance requirement. If the chips are designed with optimistic parameters, some chips cannot perform the target frequency. Therefore, in general, the worst case parameters are used for VLSI system designs to improve the chip yield. However, since such case rarely occurs, the design is excessive in most cases. In other words, the supplied voltage for them

is excessive. This results in large power overheads.

The most dominant factors of the device level variation are deviations of transistor channel length and threshold voltage (V_{TH}) [13]. Gate length varies from designed patterns due to across chip linewidth variation (ACLV) and line edge roughness (LER). ACLV is caused by lithography limitations and etching deviation depending on each layout pattern. Since recent lithographies need to fabricate smaller feature size device than the used wavelength, it is difficult to completely realize a given layout design. Also, the etching rate depends on the polysilicon density. When the density is increased, the etch rate is decreased. Contrary to ACLV, the reason of LER is not elucidated, to the best of author's knowledge, and occurs randomly. However, at highly scaled technology, it is one of the dominant variation sources. Indeed, the average variation from LER reaches 4nm at a 35-nm process [47].

The threshold voltage is a function of the number of impurities on the channel as depicted in equation (2.7). That is why inaccuracies of impurity doping cause V_{TH} variations. This effect is called as random dopant fluctuation (RDF). The standard deviation of V_{TH} under RDF is formulated as:

$$\sigma_{V_t} = \frac{t_{ox}}{\epsilon_{ox}} \times \frac{\sqrt[4]{q^3 \epsilon_{si} \phi_b N_a}}{\sqrt{2LW}} \tag{2.9}$$

where N_a is the impurity density, ϵ_{si} is equal to $11.8\epsilon_0$, and ϕ_b is the surface potential. As can be seen from this equation, a smaller L and W result in larger threshold variation. In other words, smaller transistors (i.e. highly scaled transistors) cause large process variations.

Fabricated metal wires connecting each transistor also have variations. Similarly to the gate length variation, the fabrication accuracy relies on lithography limitations and the etching deviation depends on each layout pattern. Also, the thickness of the wires and the resistance of the contacts vary due to the fabrication inaccuracy. These phenomena also affect the delay and leakage characteristics of fabricated VLSI systems.

Considering its dopantless structure, FD-SOI is one of the low variation devices as explained before. This is because the impurity density is related to the threshold voltage variation but this doping step is skipped. As a result, the random variation can be mitigated. Indeed, although the random process variation raises the minimum operational voltage for SRAMs with conventional bulk technologies, FD-SOI allows them to operate around 0.4V of V_{DD} [48]. Hence, FD-SOI devices are suitable for the current near-threshold computing trend. In addition, due to the process simplicity, the fabrication cost is not so high compared to the bulk devices. This feature is also suitable for recent SoCs which requires low cost fabrication. Therefore, FD-SOI technology is a sensible choice for embedded systems. However, the process variation issues still remain even with the FD-SOI device.

In order to show the variation problem on the FD-SOI device, Fig. 2.13 depicts the simulation results of the leakage current and gate delay on the various process variations. For this simulation, an inverter cell implemented with the SOTB 65-nm technology is used. Here, "F", "T", and "S" represent the slow, typical and fast transistor characteristics, respectively. "F" and "S" variations are given by the transistor which is the point of $\pm 3\sigma$ in the normal distribution curve. As can be seen from the figures, FF condition incurs 3.67 times larger leakage current than that of TT. On the other hand, the gate delay is degraded

at the SS condition. Although FD-SOI is useful for low power VLSI systems, the process variation should be efficiently handled.

The BBC is an efficient mean not only for power management but suppressing the process variation as well [17–19]. Indeed, in [17], the standard deviation of the die frequency distribution is reduced by 7 times by applying the BBC. Therefore, when controlling the body bias, process variation effect should also be taken into consideration.

We have discussed that controlling the body biases and power supply voltage can efficiently suppress the power consumption. Also, we have argued that process variations can be mitigated by body biasing. However, how to control these voltages? As explained in the early part of this chapter, on-chip power management units are often adopted as voltage controllers on recent SoCs. In the next section, on-chip voltage generators are reviewed.

2.6 On chip voltage generators

2.6.1 DC-DC converter for power supply

For the power supply of digital VLSI circuits, raw voltages from batteries are rarely used because it is too high for normal core transistors. The output voltage from a battery is usually down-converted to the level of standard V_{DD}s by DC-DC converters. Three types of DC-DC converters are often used for this purpose: Buck converter, Low drop-out regulator (LDO), and Switched capacitor.

The simplest buck converter is composed of switches, an inductor, and an output capacitor as shown in Fig.2.14 (a). When *S1* is conducted and *S2* is cut-off, the power supplier charges the energy to the inductor. The diode is cut-off during this state, thus the charged energy can remain. When *S1* is cut-off and *S2* is on, the charged energy in the inductor is discharged to the load using *S2*. Modulating the period when the switches are on and off, the output voltage (V_{out}) can be controlled. As shown in [49], the recent buck converter allows the fine but discrete voltage control with 12.5mV of the step. Although this technique can provide the high conversion efficiency, it usually requires an off-chip inductor [49]. Otherwise, on-chip inductors suffer from a large foot-print for implementation and low conversion efficiency [50].

An LDO is basically constructed with the pMOS switch, a comparator, and an output capacitor as shown in Fig.2.14 (b). Compared with the reference voltage, the output voltage is regulated to the required level. LDOs can enable fine voltage controllability such as 10mV of the voltage step [51]. However, the down-conversion of the voltage is performed with the on-resistance of the pMOS switch. This means that the conversion efficiency is linearly degraded when the output voltage is lowered. Hence, this way is clearly not suitable for near-threshold computing which requires quite low power supply voltages.

A switched capacitor converter is constructed with flying capacitors (*Cfly*), switches and an output capacitor as depicted in Fig.2.14 (c). The switches are periodically conducted with the complimentary oscillation signals (ϕ and $\overline{\phi}$). By repeatedly charge and discharge the capacitor, the required voltage level can be obtained at V_{out}. The depicted configuration in this figure can down-convert the input voltage with the ratio of 2:1 under no output current. Indeed, when ϕ is "0", the charged energy in the capacitor is $CflyV_{out}$, while it is $Cfly(V_{in} - V_{out})$ when ϕ is "1". Because of the energy conservation on the condition of no

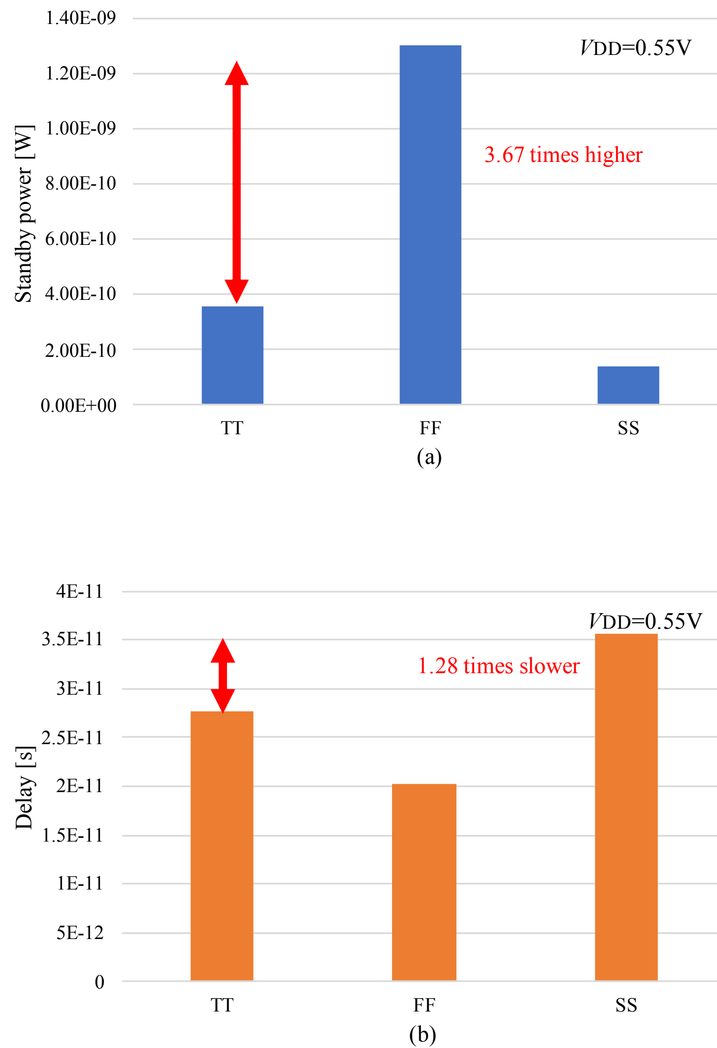


Figure 2.13: Process variation effects on a FD-SOI. The SOTB 65-nm technology is used. (nMOS/pMOS=FF,TT,SS): (a)Leakage power (b)Gate delay

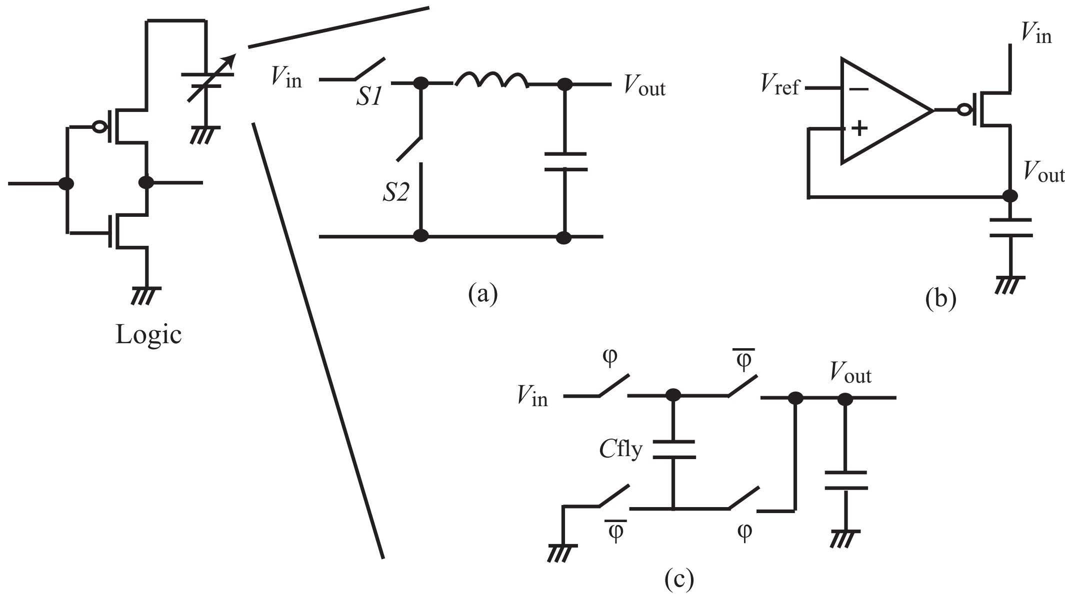


Figure 2.14: Various types of DCDC converters: (a) Buck converter (b) LDO (c) Switched capacitor.

output current, $CflyV_{out} = Cfly(V_{in} - V_{out})$ is obtained. As a result, $V_{out} = 1/2V_{in}$ can be obtained. The conversion ratio can be changed with the different number of switches and capacitors [52,53]. This converter can achieve both on-chip integration and high conversion efficiency at a low output voltage condition. Therefore, for a near-threshold voltage region, a switched capacitor type converter is often used and suitable for such demands. Nevertheless, the control granularity is not as high as the LDOs and buck converters. Indeed, in [35], only four voltage levels (1V, 0.9V, 0.67V and 0.5V) can be selected by users.

2.6.2 Voltage generators for BBC

Conventionally, on-chip body bias control schemes have been widely developed [14,54–58]. *Kuroda et al.* [14] proposed a system which can switch from strong reverse bias voltages, in the low leakage standby state, to a predefined body bias voltage in the operational state. This control is realized by monitoring the leakage current as shown in Fig. 2.15. The leakage current monitor can detect whether or not the leakage current reaches the predefined value. Based on the results, the charge pump is controlled and the body bias voltages are regulated. However, the system clock frequency needs to be decided and fixed before the chip implementation, so it cannot be changed afterward. Also, since the leakage current is sensitive to the process variation as previously discussed, this system also suffers from the variations. Therefore, it is not suitable as a body bias controller with recent process technologies.

In order to use various body bias voltages, *Digital Analog Converters* (DACs) are often used [54–57,59]. Fig. 2.16 shows a simplified diagram of a DAC-based body bias generator. The output voltage of the Charge Pump (CP) is compared with a reference voltage from

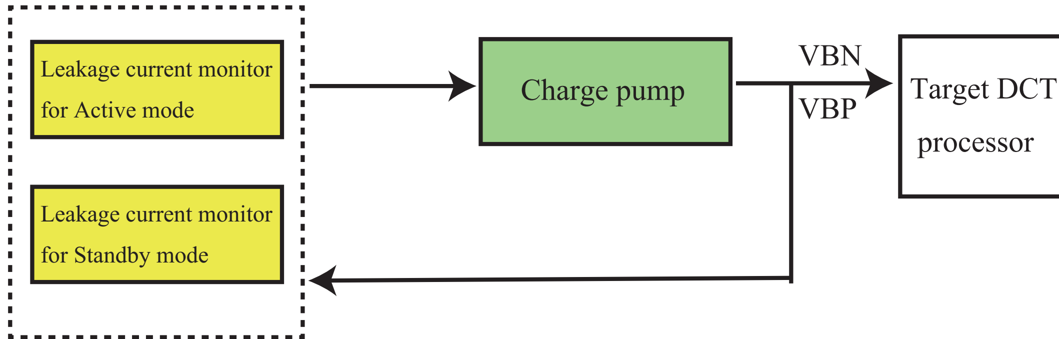


Figure 2.15: Simplified block diagram of VTCMOS.

the DAC. As a result, the body bias voltages are regulated to the same output voltages of the DAC. Note that, although a resistor ladder is depicted in this picture, another type such as a serial charge redistribution DAC can also be used [57]. Also, a resistor ladder can be inserted to the voltage feedback path, which is compared with the fixed reference voltage [59]. Recent body bias generators more or less utilize a DAC component.

It is obvious but important to mention that DAC-based body bias generators can output the voltage discretely. For example, in [55], n-well (p-well) voltage can be controlled with 58mV (72mV) of the step. Also, the body bias generator in [59] can enable 100mV of control granularity. Although the controller in [57] achieves 19mV of granularity, its power overhead is not suitable for low-power VLSI designs.

Thanks to the various level of output voltages, a DAC-based body bias generator can enable sophisticated body bias control. For example, a BBC system collaborating with a critical path monitor or/and variation monitor, which can detect a target system condition, is proposed in [54]. Fig. 2.17 depicts a simplified block diagram of it. The delay line is used as a variation monitor. The delay of the delay line is compared with the external clock signal. Then, the decoder sends the difference between these two signals. Based on this information, the body bias generator adjusts the output voltages on which a target system achieves a required performance.

The body bias control scheme in [60] also exploits a DAC-based configuration for complex voltage control. As previously mentioned, strong RBB conditions cause the increment of pn-junction leakage current and result in excessive power consumption. That is why the work presented in [60] adopts a current monitor circuit and can track the leakage optimal point.

From the above observations, used body bias voltages and power supply voltages should be properly decided. That is why a lot of research that tried optimizing them have been carried out in the past years. In the next section, previous works related to the optimization are reviewed.

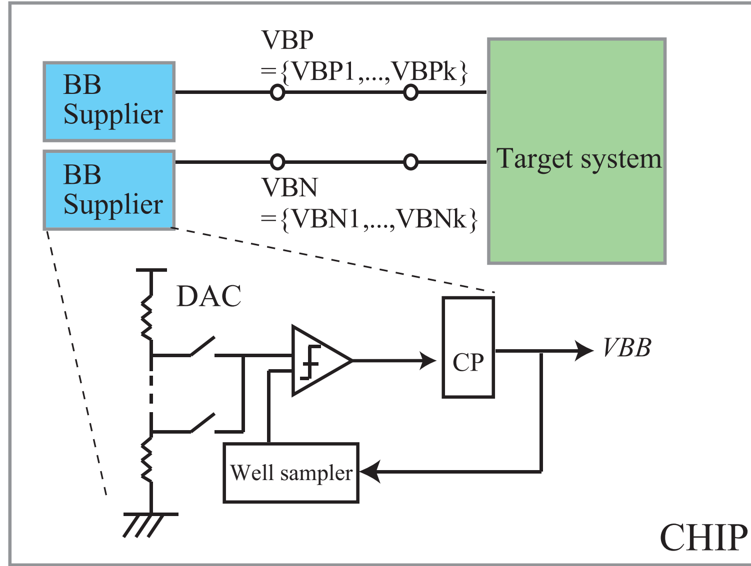


Figure 2.16: Simplified diagram of a DAC-based body bias generator.

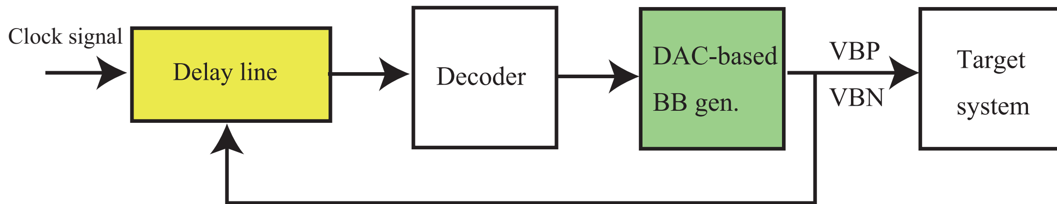


Figure 2.17: Body bias tuning system using a DAC-based controller.

2.7 Optimal voltage selection

2.7.1 Energy optimization

One of the well-known ways of the optimization is to minimize the VLSI energy consumption [61, 62].

VLSI energy consumption at one cycle can be obtained by following equations:

$$E_{total} = C_{eff} V_{DD}^2 + W_{eff} I_{sub} V_{DD} t_{d-cp} \tag{2.10}$$

where W_{eff}, C_{eff}, and t_{d-cp} represent a total effective gate width, a total effective parasitic capacitor, and a total delay at the critical path. Since the dominant leakage current is usually the sub-threshold leakage current, this equation only considers it. The energy minimization is performed by solving this equation by selecting the power supply and threshold voltages properly. *Calhoun et al.* solved the equation (2.10) and served the optimal power supply voltage in [63].

The energy minimum point is often achieved at a sub or near threshold region. Generally speaking, the maximum operational frequency is quite degraded in a sub threshold

region. Indeed, the FFT processor in [64] achieved the energy minimum point at 0.35V of V_{DD} when 16bit processing is performed. At this condition, the FFT processor can only operate at frequencies less than 10kHz. When the processor needs to operate at high frequencies such as tens of MHz, the obtained voltage is not optimal anymore. In conclusion, when VLSI systems have some certain frequency demands, only minimizing the energy consumption is not suitable.

2.7.2 Power optimization

In contrast to the energy optimization, there are some studies which optimize the power consumption for a required operational performance [15, 18, 22, 65–68]. In addition to the energy minimization, the work in [63] also can consider the performance requirement at a sub-threshold region. The essential idea of these techniques is to obtain the voltage condition which can achieve the minimum power consumption at a certain frequency demand.

In [15, 65], first of all, the power consumption is modeled as follows:

$$P_{total} = P_{SW} + P_{leak} = (\alpha_{at}C)fV_{DD}^2 + I_{off}10^{\frac{V_{gs}+\eta(V_{ds}-V_{DD})+K\gamma V_{sb}}{S}}(1 - e^{\frac{-V_{ds}}{v_T}})V_{DD} \quad (2.11)$$

Since the leakage currents are represented by the complex equations as shown in the previous section, they treat only the sub-threshold leakage current on their model. However, as shown in [25], a simpler leakage model can be constructed. Since I_{gate} is an exponential function to V_{DD}, the leakage model including both I_{gate} and I_{sub} can be represented with:

$$I_{sub+gate} = K_3 e^{K_4 V_{DD} + K_5 V_{bs}} \quad (2.12)$$

where $K_3 - K_5$ are constant fitting parameters. Also, the current from pn-junctions is considered as a constant value I_j. As a result, the leakage current is modeled as:

$$I_{leak} = K_3 e^{K_4 V_{DD} + K_5 V_{bs}} + I_j \quad (2.13)$$

Under the delay constraints from equation (2.6), the power consumption can be minimized by tuning the power supply voltage and body bias voltages based on the model values. These models can also be leveraged by a task scheduling algorithm incorporated with DVFS [66, 67].

Due to the configurations of actual on-chip voltage regulators previously shown, the available voltages for the power supply and body bias are discrete values at actual VLSI systems. Power optimization has to consider this limitation. Therefore, the work in [68] proposes such an optimization. The authors of [68] assume that the power supply driver can only output a few voltage steps. On the other hand, the body bias voltages are assumed as continuous values since relatively finer voltage granularity can be available for BBC. Although the assumption for BBC is not practical, we can notice the importance of considering hardware constraints from this problem definition. Upon this assumption, the power consumption behavior of VLSI systems can be depicted as shown in Fig. 2.18. The curves on the power-frequency plane can be obtained with each discrete V_{DD} voltage by sweeping body bias voltages. From this figure, we can notice that it is difficult to achieve

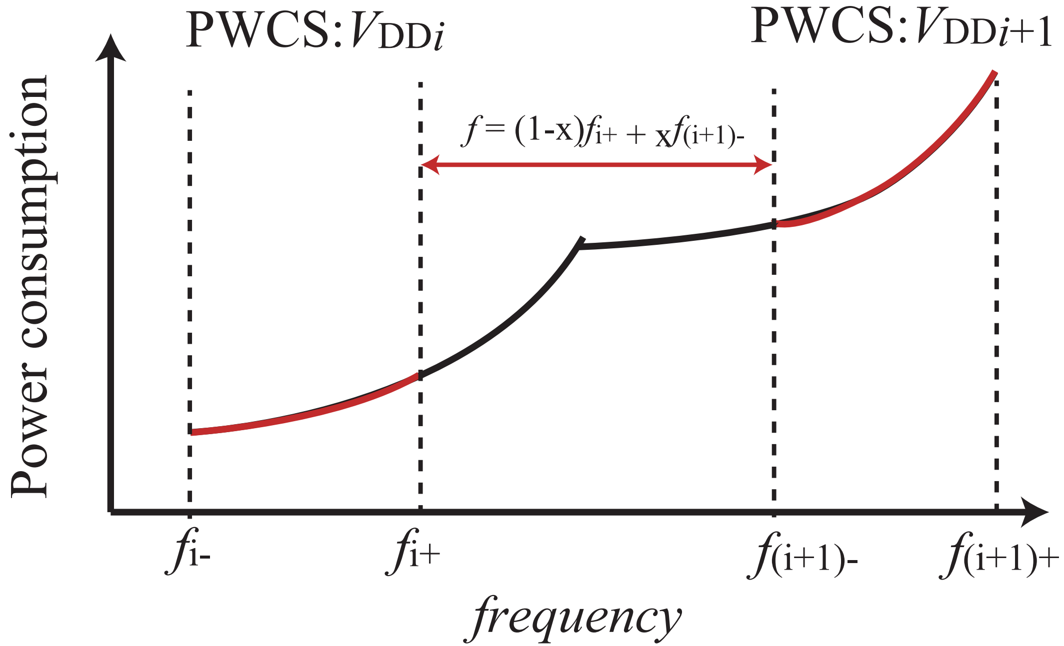


Figure 2.18: Power optimization considering the restrictions of an actual power supply source.

a convex curve for the entire frequency region. In other words, the power consumption is rapidly increased at some performance points, which cannot be convex. Therefore, in order to ascertain the convexity of the entire frequency region, Piece Wise Convex Set (PWCS) is introduced. PWCS is defined as [68]: *"A function is defined as piece-wise convex, if every point of the function $P_{total}(f)$ between two points from different pieces of curve are situated below the segment of line connecting these points."* If a required frequency (f_{req}) is in a PWCS, such conditions can be used. On the other hand, if f_{req} is out of a PWCS, it is achieved as

$$f_{req} = xf_{(i+1)-} + (1-x)f_{i+} \tag{2.14}$$

where $f_{(i+1)-}$ (f_{i+}) is the lowest (highest) frequency in V_{DDi+1}'s (V_{DDi}) PWCS. That is, the power between PWCSs is achieved by the timewise control of V_{DD}.

From these backgrounds, some research queries for low-power VLSI designs can be obtained and introduced in the next chapter. Before clarifying them, a summary of this chapter is depicted in the next section.

2.8 Summary

Firstly, in this chapter, recent SoCs for embedded systems are introduced in order to understand our target. Such systems adopt highly scaled process technologies and integrate

huge computation resources, which result in large power consumption. Therefore, lowering system power is still one of the main concerns for VLSI designs.

The power consumption is composed of the leakage and dynamic current. The dynamic current can be controlled by the power supply voltage scaling, while the leakage current can be tuned with both the power supply and body bias voltages. Nevertheless, these voltage scalings have a trade-off between power and system performance. For a standby state when a target system does not have to operate, ultra-low power voltage conditions can be used. Hence, a required voltage control can be simply realized such as just supplying very low V_{DD} or deep RBB. On the other hand, when a VLSI system is an active state, an appropriate voltage control methodology to satisfy performance demands and minimal power consumption is required. Therefore, power optimization methodologies which can obtain such voltages have been investigated so far.

Also, recent VLSI systems suffer from process variation effects because highly scaled process technologies are often used even for embedded VLSI systems. Although FD-SOI devices can relatively mitigate the variation effect compared to bulk technologies, they cannot completely resolve this problem. Nevertheless, the body bias effect is strengthened by the unique transistor structure of the FD-SOI. Therefore utilizing both of the BBC and FD-SOI is an efficient mean to manage both leakage current and process variation. As previously stated, an efficient voltage control for an active state of a target system is particularly necessary.

From these backgrounds, in this thesis, a more efficient body bias control is explored. As explained in the next chapter, considering practical hardware limitations, conventional power optimizations cannot fully utilize given power management units. Also, as reviewed in this chapter, recent SoCs are equipped with an on-chip power management unit. Nevertheless, especially for low-power VLSI designs, its overhead cannot be ignored and should be minimized.

3

Motivation

3.1 Restriction on conventional optimization methods

As shown in the previous chapter, the body bias voltage has to be supplied not only to nMOSFETs, but pMOSFETs as well. However, the conventional power optimizations shown in the previous chapter cannot distinguish these voltages. For example, the only one body bias variable (V_{bs}) is available for equation (2.12). In the original work [25] introducing this equation, the coefficient for V_{bs} is extracted from nMOS SPICE model. Therefore, the leakage dependency to the body bias for an entire VLSI system is represented by that for an nMOSFET. This means that the entire system leakage current is assumed as:

$$I_{entire-leak} = I_{leak-pMOS}(V_{sbp}) + I_{leak-nMOS}(V_{sbn}) = 2I_{leak-nMOS}(V_{sbn}). \quad (3.1)$$

Here, $I_{leak-pMOS}$ and $I_{leak-nMOS}$ are the leakage currents from pMOS and nMOS, respectively. In order to obtain the expected optimization result with a real chip, the body bias for pMOS has to be controlled so as to comply to $I_{leak-nMOS} = I_{leak-pMOS}$. From this context, an appropriate VBP condition is decided for each VBN voltage. Thus, VBN and VBP voltages cannot be distinguished. Also, in the system fabricated in [15], the VBP and VBN voltages are set to the same degree. For example, if VBN is set to 0.1V of RBB, VBP is also set to 0.1V of RBB. This manner can be expressed with the following equation:

$$VBP + VBN = V_{DD}. \quad (3.2)$$

Hence, the work in [15] cannot distinguish VBN and VBP. This "symmetric" voltage constraint is utilized for making the power optimization problem easy and enables on-chip solutions [15]. Nevertheless, this constraint can degrade the efficiency of BBC as discussed below.

First of all, do the "symmetric" constraints given by the equation (3.2) always bring power optimal conditions? If there are other optimal points outside the constraints, they

should be used even though the required power optimization becomes complex. For this query, HSPICE simulations with some standard cells are conducted and their results are shown in Fig. 3.1. 2NAND, 2NOR, and INV implemented with SOTB 65-nm technology are used. For each of the gates, the magnified graphs are also shown. Here, we assume in the case of "symmetric" BBC that VBP and VBN comply with equation (3.2) similarly to the work in [16]. The horizontal and vertical axes of Fig. 3.1 represent the gate delay and leakage current, respectively. The used voltages here are $\mathbf{VBP} = \{0.2, 0.4, ..., 1.6\}$V, $\mathbf{VBN} = \{0.4, 0.2, ..., -1.0\}$V, and 0.6V of V_{DD}. Each curve corresponds to each VBP voltage value and is depicted by sweeping the VBN voltage with 0.2V of the voltage step. Therefore, each plot in these curves corresponds to each VBN voltage. For example, the plot at the left end of each VBP curve represents $VBN = 0.4V$ (0.4V of FBB). From right to left, VBN voltage is incremented at every plot with 0.2V of the voltage step. As can be seen from the graphs, the symmetric condition curve is optimal in the case of INV. Nevertheless, some voltage points which are not "symmetric" can be optimal in the case of 2NAND. For example, on the condition that $VBP = 0.4$V of RBB and $VBN = 0.2$V of RBB are supplied to the 2NAND, the corresponding plot is located below the line of "symmetric" BBC (Fig.3.1 (b)). 2NOR simulations also demonstrate the presence of such points; but they are less than the case of 2NAND. Regarding the case where $VBP = 0.2$V of RBB and $VBN = 0.4$V of RBB are supplied to the 2NOR, the corresponding point is below the line of "symmetric" BBC (Fig.3.1 (c)).

The behavior difference among these graphs comes from the difference of the gate structures. For example, VBN is supplied to the stacked nMOS in the case of 2NAND. Thus, the body bias effect at the nMOSFETs is strengthened when compared to the case of INV. As a result, the optimal voltages for 2NAND and 2NOR can be shifted from the "symmetric" conditions which are optimal for the INV.

It is important to mention that the number of optimal "asymmetric" body bias conditions for 2NOR is less than that of 2NAND. This is from the difference of the body bias effect between nMOS and pMOS. As can be seen from Fig. 3.2 which depicts the body bias dependency to V_{TH} of nMOS and pMOS, pMOS has a smoother slope than nMOS. That is why, although the body bias effect for the pMOS at 2NOR is stronger than the case of INV, the optimal body bias balance does not shift a lot from the case of INV, unlike the NAND gate. In conclusion, the optimal body bias balance might be different according to used standard cells.

Also, if we could not distinguish VBN and VBP control, power inefficient situations can be caused when considering a restriction from actual body bias genelators. Here, we assume that the "symmetric" constraint is given by equation (3.2). As discussed in the previous chapter, actual body bias generators can output discrete voltages because DAC-based body bias generators are often used. Combining this restriction and the "symmetric" constraints, the number of available voltage conditions are quite limited. For more clarification, Fig. 3.3 (a) shows the concept of conventional symmetric body bias voltage combinations. Note that the number of the boxes in this figure corresponds to the degree of the body bias. In the symmetric condition, the direction of the body bias (i.e., FBB, zero bias and RBB) and the degree have to be completely matched between VBP and VBN (*Comb.1* and *Comb.2*). In other words, if a body bias generator has k of voltage steps for both VBP and VBN, the number of available symmetric voltage pairs is also k at maximum, as shown in

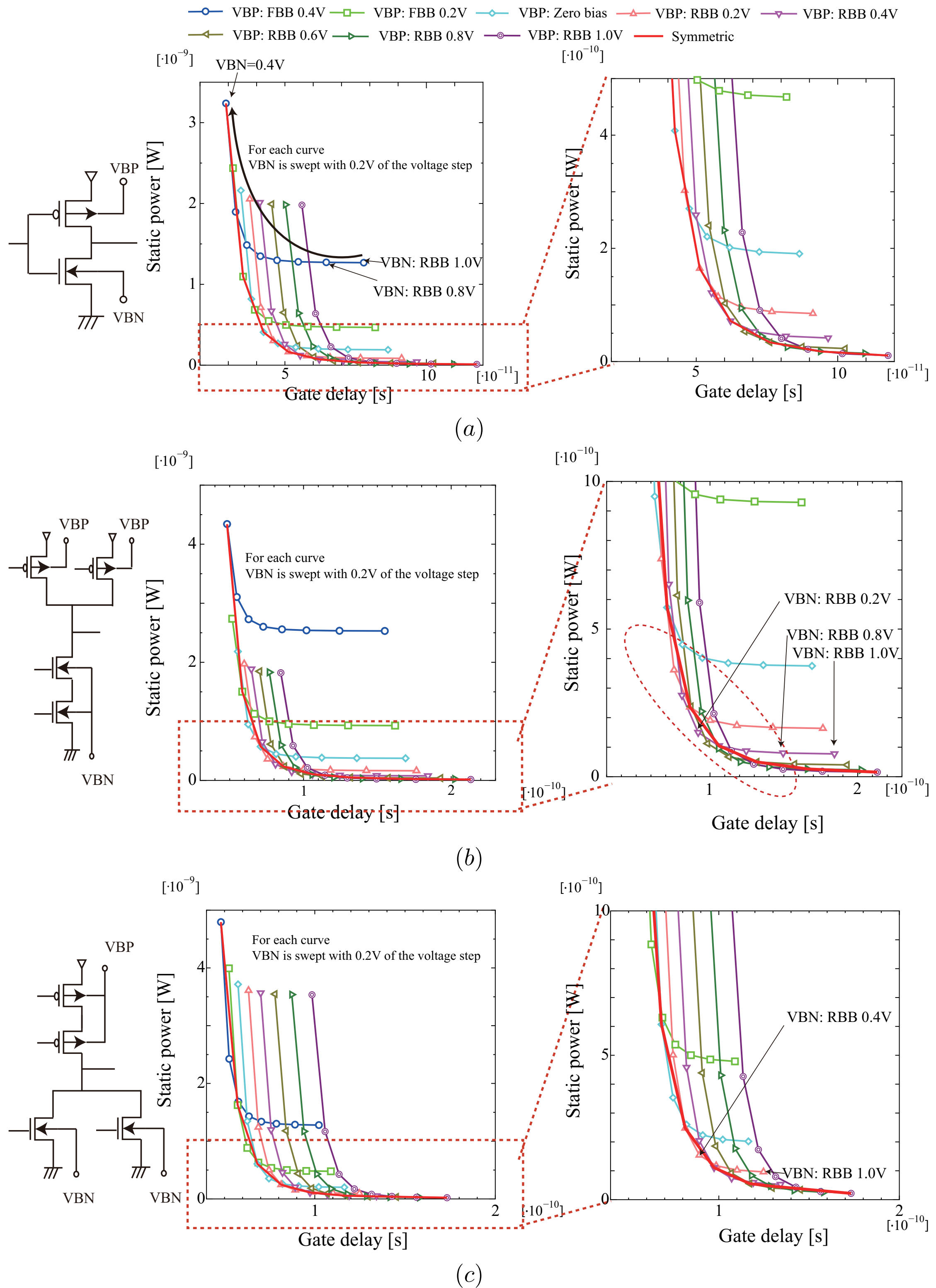


Figure 3.1: Relationship between the gate delay and static power under the various body bias voltages ($V_{DD} = 0.6V$):(a) INV (b)2NAND (c)2NOR

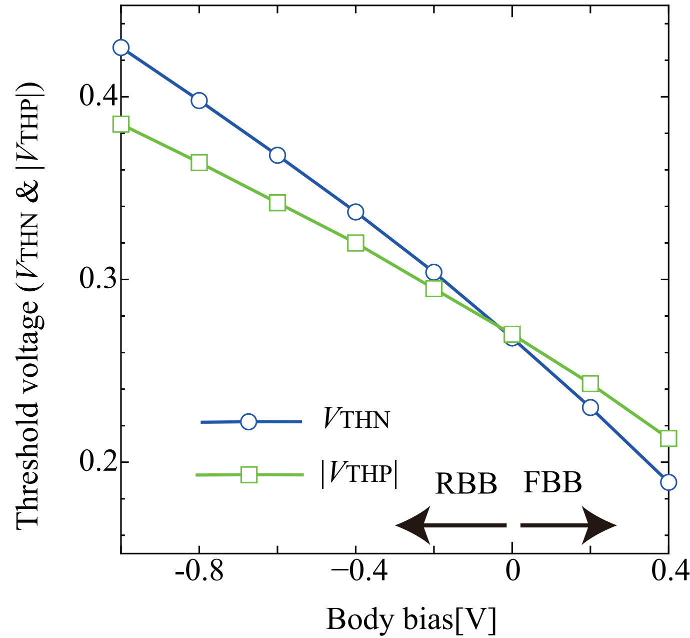


Figure 3.2: Simulated body bias dependency to the threshold voltage (+:FBB -:RBB)

Fig. 3.3 (a).

Contrary to the “symmetric” BBC, if the degree and direction of body bias can be different between VBP and VBN, as depicted by *Comb.3* and *Comb.4* in Fig. 3.3 (b), any VBP voltage can pair with any VBN voltage. If a body bias generator has k voltage steps, the number of possible voltage patterns is increased to k^2.

Table 3.1: Implementation conditions of the tested chips.

	V850E-Star	MuCCRA4BB
process	65-nm FD-SOI (Renesas SOTB)	
Logic Synthesis	Design Compiler	
Routing of Layout	IC Compiler	
Package	208PIN QFP	
Threshold voltage	V_{t0n}=0.19	V_{t0n}=0.269
	$\|V_{t0p}\|$=0.20	$\|V_{t0p}\|$=0.270

To show the efficiency of asymmetric BBC, the real test-chips of two different types of architectures are evaluated: (1) a dynamically reconfigurable processor, named "MuCCRA4-BB" (MuCCRA4) [69], and (2) an embedded microcontroller "V850-Estar" (V850) [39]. Both systems are implemented with SOTB 65-nm FD-SOI technology. Note that, although both processors employ SOTB technology, V_{TH} and typical V_{DD} voltages for V850 are lower than those of MuCCRA4. Thus, V850 is a leakage current dominant system, while MuCCRA4 is a switching current dominant one. The summary of the tested chips and their

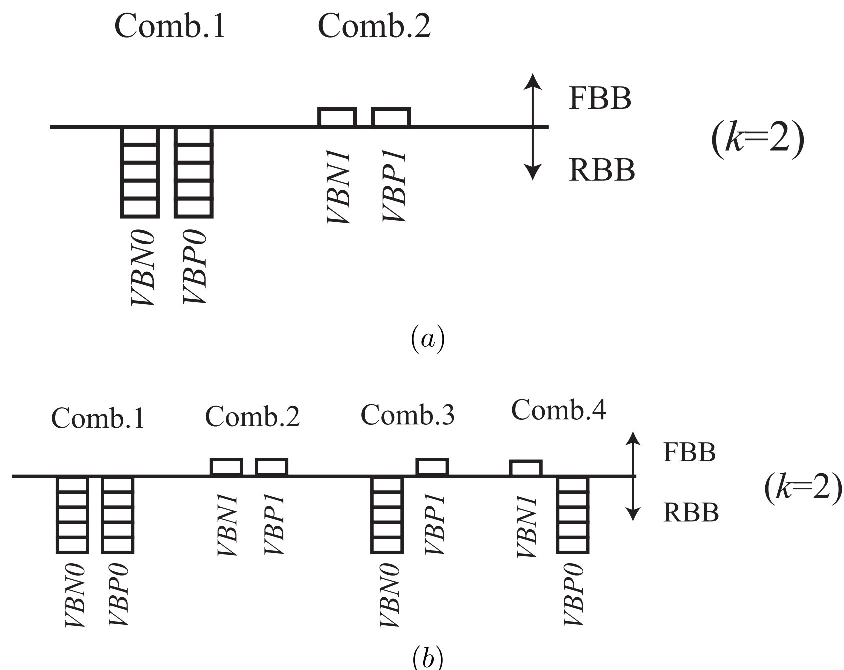


Figure 3.3: Concept of the body bias control at the condition where the number of voltage pattern k is equal to 2. We have $\{VBN0, VBN1\}$ for nMOS body bias and $\{VBP0, VBP1\}$ for pMOS: (a) Symmetric (b) Asymmetric.

chip photographs are shown in Table 3.1 and Fig. 3.4, respectively. For a body bias generator, an ideal voltage regulator for BBC is assumed. It can output voltages ranging from 0.2V of FBB to 0.5V of RBB with a voltage step of 0.1V. These voltages are supplied to the entire chips with an off-chip voltage regulator. Therefore, the number of asymmetric body bias combinations of VBP and VBN for both systems in this experiment is 64 (only eight in the case of symmetric BBC). The V_{DD} of V850 and MuCCRA4 are set to 0.4V and 0.6V, respectively. With these voltages, the maximum operational frequency and leakage current are measured.

Fig. 3.5 shows the relationship between the measured maximum operational frequency and leakage current. The maximum operational frequency is obtained with 1MHz of frequency step. Since there is a noise margin at the near-threshold region, unlike the subthreshold region, both systems were able to correctly work at asymmetric body bias conditions. From these plots, it can be observed that careless choices of body bias voltages clearly cause unnecessary leakage overhead. For example, at 36MHz of operational frequency in Fig. 3.5 (a), there are three measured points. From these three candidates, the leakage minimum point has to be selected. The same applies for other operational frequencies.

Fig. 3.6 shows the comparison results between the symmetric BBC and the extracted minimum leakage points, from Fig. 3.5, of the "asymmetric" BBC for each of the operational frequencies. It is an important reminder that the asymmetric BBC also includes the symmetric body bias pairs as shown in Fig. 3.3. Due to the discrete voltage and performance

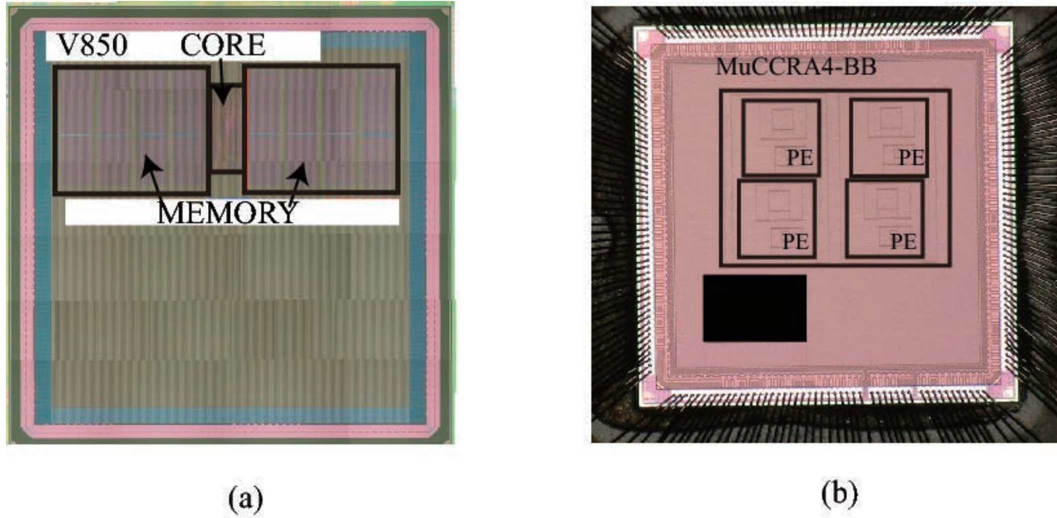


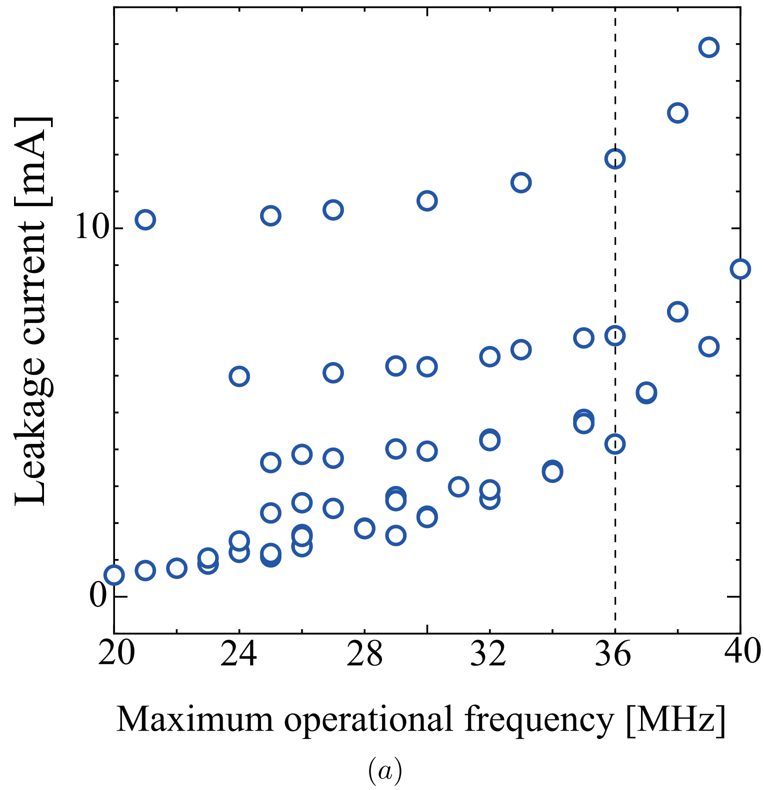
Figure 3.4: Photos of the tested chips: (a) V850-Estar (b) MuCCRA4-BB.

control, the step-wise curves can be obtained at both lines of “asymmetric” and “symmetric” BBC. For example, on the condition that ($VBN1$, $VBP1$) and ($VBN0$, $VBP0$) can respectively achieve 40MHz and 37MHz, 39MHz and 38MHz are both achieved by ($VBN1$, $VBP1$) at the symmetric BBC. The leakage currents at these frequencies are the same at 40MHz. From 37MHz, the leakage current can be lowered by using ($VBN0$, $VBP0$). In this manner, the step-wise curve of the symmetric BBC can be depicted. Although the curve of the asymmetric BBC is step-wise as well, the step is finer than the symmetric BBC thanks to the finer voltage control. This contributes to lower the leakage consumption at some frequencies. Considering the case of V850 at 38MHz, 23.68% of leakage reduction is achieved. Also, comparing Fig. 3.6 (a) to (b), we can observe that the benefits of the asymmetric BBC depend on the target architecture. The asymmetric body bias pairs provide less optimal voltage combinations in the case of MuCCRA4. Nevertheless, the asymmetric BBC still achieves lower leakage condition at some frequencies. Observing the case of MuCCRA4, 22.78% of leakage reduction is obtained at 36MHz of operational frequency.

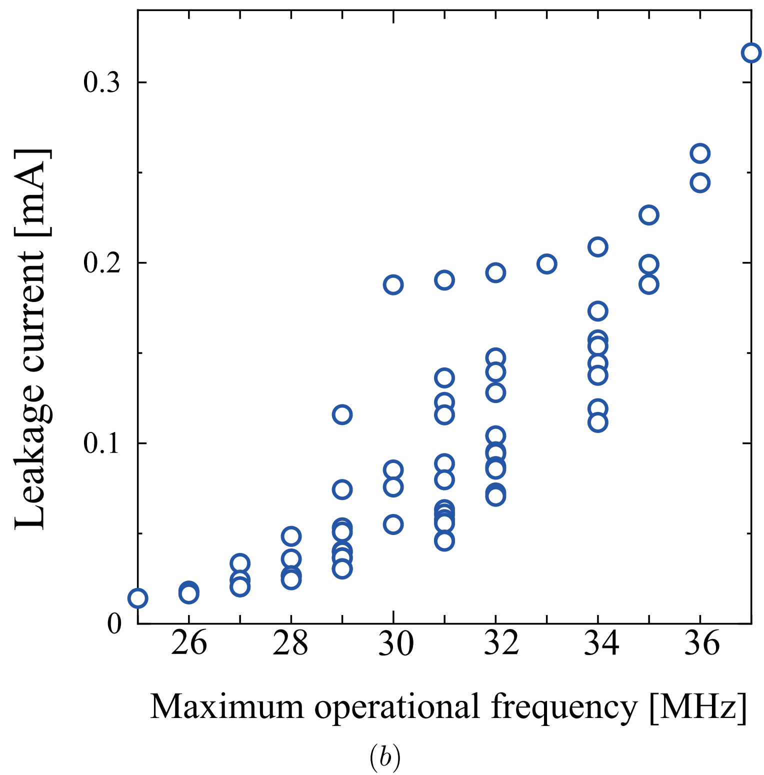
Although the “asymmetric” BBC can improve the energy efficiency, the optimization complexity becomes a major challenge. This is because the number of voltage combinations to be considered significantly increases. Using brute force search [27] for chip measurements causes a tremendous testing cost and cannot be tolerated for a large number of voltage combinations. Therefore, an efficient power optimization methodology which can treat the asymmetric BBC has become imperative.

The power optimization methodology reported by *Kumar et al.* [18] is one of the few studies in which asymmetric body bias control might be used. This method is based on leakage and delay models which are constructed with the second order polynomial approximation as:

$$Delay = D_0 \sum_{i=0}^{2} \sum_{j=0}^{2} a_{ij} VBN^j VBP^i \tag{3.3}$$

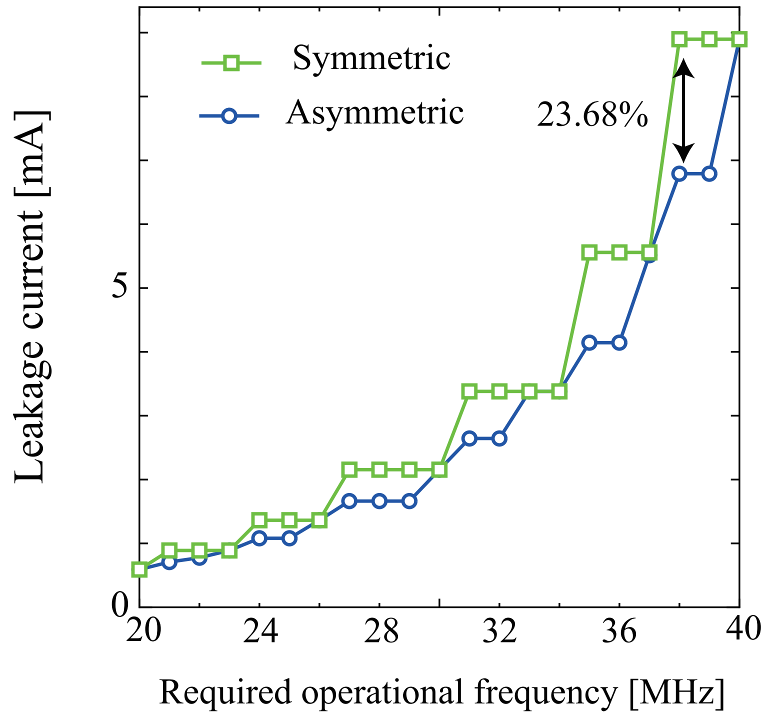


(a)

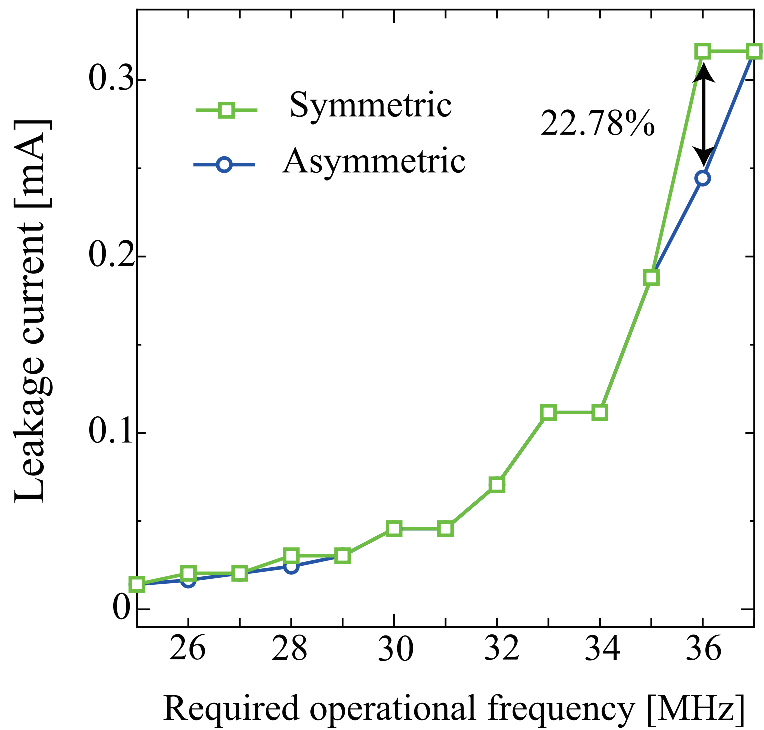


(b)

Figure 3.5: Leakage current characteristics vs f_{max}: (a) V850-Estar (b) MuCCRA4-BB.



(*a*)



(*b*)

Figure 3.6: Extracted optimal voltage conditions with asymmetric BBC: (a) V850-Estar (b) MuCCRA4-BB.

$$Leak = L_0 \sum_{i=0}^{2} \sum_{j=0}^{2} b_{ij} VBN^j VBP^i \tag{3.4}$$

Here, D_0 and L_0 represent the critical path delay and the leakage current at given temperature and process conditions without any body bias. However, these equations clearly cannot treat V_{DD} voltage. Ignoring the effects of the V_{DD} voltage can cause large leakage current at high-performance requirements. Although they later proposed a power optimization methodology [27] which can treat the power supply voltage and both of the body bias voltage simultaneously, it is based on a brute force search using chip measurements, since equations (3.3) and (3.4) do not consider the power supply voltage. Relying only on brute force search causes a tremendous testing cost which significantly increases when the search space goes wider.

Considering the above observations, in this thesis, power and delay models which consider V_{DD} and the asymmetric body bias condition are firstly proposed. The proposed models are based on well-known equations, but, simplified so as to be applied to a real chip processor. The coefficients for the models can be extracted with real chip measurements; thus, the error is minimized to only a few percents in average. Based on these models, a power optimization methodology considering simultaneously the power supply and asymmetric body bias condition is proposed. Thanks to the adopted models, the proposed power optimization does not require a brute force search when testing all the candidate voltage patterns. The proposed method allows utilizing given voltage regulators more efficiently compared to the conventional methods.

Another important point that should be carefully considered is that power optimization methods based on models, in general, suffer from deviations between the real chip measured values and the calculated ones. Although such deviations are inevitable, the calculated voltages might cause timing faults when supplied to the real chip. Therefore, such errors have to be compensated with a smart mechanism that enables the voltage adjustment to meet the required system performance.

In order to consider the error between the model and real VLSI chips, a low-overhead adjustment technique to compensate them is proposed. By adding a low overhead controller, the obtained voltage combination assures that the target chip can correctly operate at the required frequency. The proposed optimization is shown in chapter 4.

3.2 Overhead of Body Bias Controller

For low-power VLSI systems, the power overhead from the voltage controller has to be considered. Otherwise, the overhead might degrade the energy efficiency of the BBC.

As previously discussed, the body bias is conventionally controlled with DAC-based systems. Such DAC-based controllers can realize sophisticated and complex body bias control as investigated in [54, 60]. Nevertheless, as discussed below, they cannot be always optimal for low-power design.

DAC-based designs generally require another power source for the analog circuits in addition to the power supplier for digital ones [54, 55]. This is because general analog circuits need to be driven by higher voltages than that of digital circuits. Therefore, the power supply voltage for digital circuits cannot be shared with analog ones. An additional

power source eventually increases the entire system cost. Although the I/O voltage can be shared with the DACs as adopted in [55], such method obligates the DAC voltages to be highly depending on the I/O cell configurations. In fact, although the work in [55] utilizes 1.8V as the I/O voltage, 3.3V might be required for other I/O cells. Such I/O voltage might increase the power overhead of the body bias generator. Otherwise, an additional 1.8V power source is required.

On the other hand, *Kamae et al.* [57] proposed the DAC-based configuration for near-threshold power supply voltages. They modified the conventional DAC for low-power supply operations; nevertheless, their configuration incurs a considerable power overhead which can reach up to 600μW. Such an overhead cannot be ignored when ultra low-power chips are considered. Although this overhead might be reduced by a configuration at which FBB can only be available [70], the leakage current cannot be reduced if it is excessive.

Compared to analog circuits, digital circuits can operate at low supply voltage [23]. Therefore, they can be a viable solution to solve the power overhead of analog circuits. There are some studies that replace analog circuits with digital ones [28–30]. By adopting this idea, a body bias generator can operate at the same supply voltage as that for digital circuits. In this way, the use of an additional analog power source is no longer required. Moreover, digital circuits do not consume quiescent current, unlike analog circuits. This constitutes an additional reason to use such circuits for more efficient body bias control.

Based-on digital circuits, *Mauricio et al.* [58] proposed a "DAC-less" body bias control scheme. Although it is difficult to implement a sophisticated voltage tuning algorithm like [60], the "DAC-less" configuration can reduce the system power overhead. In [58], a target delay can be tuned to match the length of the reference pulse. Therefore, by setting this pulse length to a certain time, the target delay can also be accordingly adjusted. With pre-layout simulations, they showed that their proposed system is useful to mitigate process variations and can operate at the same supply voltage as that for the digital circuit (i.e., 1.0V). However, they do not show whether their system is still useful for the near-threshold region or not. Since recent low power processors operate at such low-voltage region [23], it is necessary to validate such a property. Besides, to treat dynamic frequency scaling in their system, an additional pulse generator which can automatically output the required pulse length has to be implemented. Otherwise, they cannot automatically adjust the system delay when a required frequency is altered. Furthermore, since the entire work is based on simulations, the actual efficiency (e.g. power overhead, immunity for conditional variations at a real environment, etc..) of their system is not proved.

Quelen et al. also proposed a DAC-less body bias controller in [71]. This architecture is the most similar work to the proposed one in this thesis. According to the critical path information and reference clock frequency, the body bias for a given target system is automatically tuned. However, for the body bias controller, an additional analog power supply (1.8V) is required due to its configuration. Although DAC-less configuration is employed, this work cannot fully utilize its advantages.

Regarding the above state of the arts, this thesis also purses a light-weight DAC-less body bias controller rather than DAC-based one for ultra low-power VLSI design. The proposed scheme is named "Digitally-assisted Automatic Body-bias Tuning" (DABT). Unlike [58], our system automatically tunes the body bias voltage even at a near-threshold region when the operating clock frequency is altered. In addition, DABT does not require

any additional voltage suppliers while it is necessary for the work [71]. DABT is fabricated using the SOTB 65-nm FD-SOI technology. Real chip measurements prove that DABT can operate even at 0.35V of supply voltage. Moreover, to the best of author's knowledge, the proposed scheme can achieve the lowest power overhead when compared to existing implemented body bias generators. The proposed architecture and its implementation are introduced in chapter 5.

4

Power Optimization Enabling Asymmetric Body Bias Control

4.1 Adopted Power and Delay Models

In this chapter, a power optimization methodology enabling the asymmetric BBC is proposed and evaluated. As previously mentioned, it is based on power and delay models. In this section, power and delay models for the optimization are proposed. They are based on well-known equations, but, simplified so as to be applied to real chip systems. The model coefficients can be easily obtained by real chip measurements. The proposed models are validated with the real test-chips of V850 and MuCCRA4, listed in Table 3.1, as case studies.

4.1.1 Power consumption

The leakage current is composed of the sub-threshold leakage current, gate leakage current, gate induced drain leakage (GIDL) and p-n junction leakage current in MOSFET [13]. These leakage currents are formulated by quite complex equations as reviewed in Chap. 2. Although the p-n junction leakage current is negligible thanks to the FD-SOI structure, treating the rest of these complex equations for the optimization is still not a practical way.

Regardless of the complexity of the leakage current equations, the actual leakage current dependencies to the body bias and power supply voltage are simple. In order to show them, Fig. 4.1 depicts HSPICE simulation results of the leakage current. These are obtained by sweeping the power supply and body bias voltage. A 65-nm and 28-nm FD-SOI technologies are used for these simulations. As can be seen from the graphs, the entire leakage current of MOSFET has a simple exponential dependency to the power supply and body bias voltages. Hence, the leakage current can be simplified with the following exponential

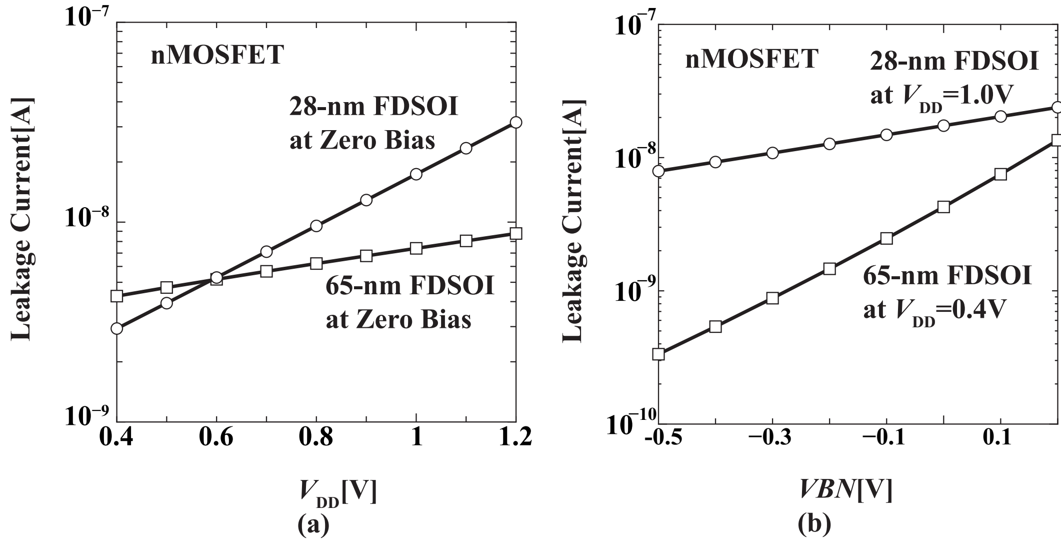


Figure 4.1: Leakage current of FD-SOI (a) characteristics of V_{DD} (b) characteristics of VBN

equation:

$$I_{leak} = I10^{AV_{DD}+BVBN} \tag{4.1}$$

Here I, A and B correspond to the coefficients of an exponential term, the exponent part of V_{DD}, and the exponent part of VBN, respectively. This model is quite similar to equation (2.13); but, the p-n junction current is ignored here. As can be clearly seen, equation (4.1) cannot treat the asymmetric body bias condition. In order to distinguish VBP voltage, the leakage model is extended as:

$$I_{leak} = I_n 10^{A_n V_{DD}+B_n VBN} + I_p 10^{A_p V_{DD}+B_p(V_{DD}-VBP)}. \tag{4.2}$$

The first and second terms represent the leakage current of nMOSFET and pMOSFET, respectively. Subscript n and p are given to I, A and B for the corresponding polarity. Note that, when zero bias is supplied, VBN and $V_{DD}-VBP$ become "0". Thus, the coefficients I_n, I_p, A_n, and A_p can be easily obtained by measuring the leakage value at zero bias. Once A and I are obtained, the coefficient B can be calculated with the body bias dependency. It is also worth noting that the leakage current at each pMOSFET and nMOSFET can be approximately measured by setting the other polarity to a strong RBB. For example, on the condition that VBN is in deep RBB, the measured leakage current is mostly dominated by pMOS. That is why the coefficients for pMOSFET are independently extracted, even during the real chip testing. In the same way, the coefficients for nMOSFET can also be extracted.

Unlike the leakage power, the switching power is the product of switching activity α_{at}, capacitance C, frequency f, and V_{DD}^2 as explained in the previous chapter. Thus, it does not depend on the body bias, but, only on V_{DD}. Although C might be slightly influenced by the body bias, it is assumed as a constant in this thesis. In this case, $\alpha_{at}C$ can be easily

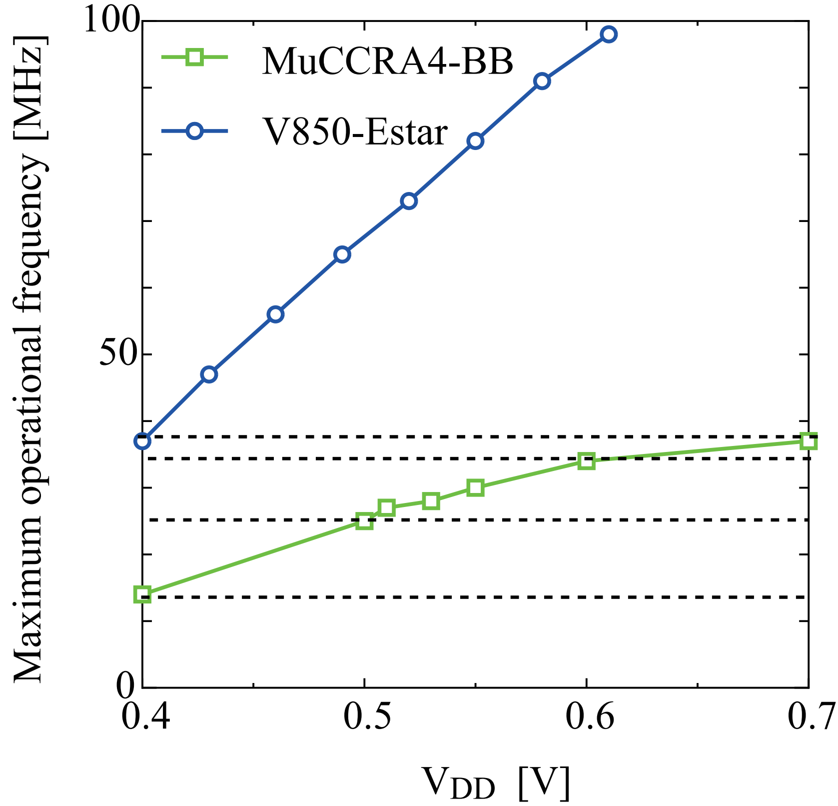


Figure 4.2: V_{DD} frequency characteristics at zero bias state.

calculated by dividing the dynamic current over the operational frequency and V_{DD}. Consequently, the total power considering asymmetric body bias condition can be formulated as:

$$\begin{aligned} P_{all} &= (I_n 10^{A_n V_{DD} + B_n VBN} + I_p 10^{A_p V_{DD} + B_p (V_{DD} - VBP)} \\ &+ (\alpha_{at} C) f V_{DD}) * V_{DD}. \end{aligned} \tag{4.3}$$

Table 4.1 lists the coefficients of the power model for both V850 and MuCCRA4.

4.1.2 Operational frequency

Equation (4.3) calculates the power consumption with a certain clock frequency (f) and a maximum required frequency f_{max}. In general, the delay is given by the alpha power law [41] as shown in equation (2.6). Here, Fig. 4.2 shows the V_{DD} dependency on f_{max} for V850 and MuCCRA4. f_{max} was obtained by checking the function-fault point of a test program for each target system. From this figure, it is observed that the f_{max} of MuCCRA4 is saturated at a relatively higher V_{DD} while that of V850 is not. On the condition that the saturation occurs, α gets closer to “1” rather than “2” [41]. The value of α is decided to be “1.3", since this value was able to construct the most accurate model for MuCCRA4. In the

case of V850, α was decided to "2" because of the slower f_{max} saturation. In order to treat the delay of nMOS and pMOS separately, as shown in [72], the model can be extended as:

$$t_d = t_{dp} + t_{dn} = \frac{xpV_{DD}}{(V_{DD} - |V_{THP}|)^{\alpha}} + \frac{xnV_{DD}}{(V_{DD} - V_{THN})^{\alpha}}.$$

Here, the threshold voltage V_{TH} has a body bias dependency. In order to easily treat it, V_{TH} is approximated as:

$$V_{THN} = V_{t0n} - K_{\gamma n} VBN, \tag{4.4}$$

$$V_{THP} = |V_{t0p}| - K_{\gamma p}(V_{DD} - VBP). \tag{4.5}$$

where V_{t0} is the threshold voltage at zero-bias [13]. It is important to mention that, as shown in the leakage model, $V_{DD} - VBP$ is used for pMOSFET so as to remove the body bias term at the zero bias condition. With equations (4.4), (4.4) and (4.5), t_d at given voltage combinations can be calculated. Finally, f_{max} can be obtained by:

$$f_{max} = \frac{1}{t_{dp} + t_{dn}}. \tag{4.6}$$

Here, t_{dp} and t_{dn} are, respectively, obtained by:

$$t_{dp} = \frac{xpV_{DD}}{(V_{DD} - |V_{t0p}| + K_{\gamma p}(V_{DD} - VBP))^{\alpha}}, \tag{4.7}$$

$$t_{dn} = \frac{xnV_{DD}}{(V_{DD} - V_{t0n} + K_{\gamma n} VBN)^{\alpha}}. \tag{4.8}$$

By measuring VBN and VBP dependency of f_{max}, $K_{\gamma n}$ and $K_{\gamma p}$ can be obtained. Also, xp and xn can be calculated by the f_{max} at the zero bias condition. These parameters for V850 and MuCCRA4 are listed in Table 4.1. Here, in order to easily calculate these coefficients, $x_p = x_n$ is assumed. As shown later, these simplifications do not degrade the quality of the model. Once these parameters are obtained, f_{max} can be computed at a given voltage combination.

4.1.3 Accuracy of the proposed model

In order to validate the proposed models for the leakage current and maximum operational frequency, the accuracies of these models are observed in this section.

Fig. 4.3 shows the difference in terms of leakage current between the real chip values and the calculated ones by the model. In Fig. 4.3 (a), the maximum error with V850 and MuCCRA4 is 4.727% and 2.380%, respectively. Although the errors become relatively higher in the body bias dependency, as depicted in Figs. 4.3 (b) and (c), the worst ones are still 10.27% and 15.83% for V850 and MuCCRA-4BB, respectively. When considering the error average from Figs. 4.3 (b) and (c), they are only 3.020% (V850) and 4.354% (MuCCRA4). Note that, since the leakage current of each polarity (pMOS and nMOS) is taken by setting the other polarity to a strong RBB, the obtained model is affected by this experimental setting. Nevertheless, the average errors are still a few percent.

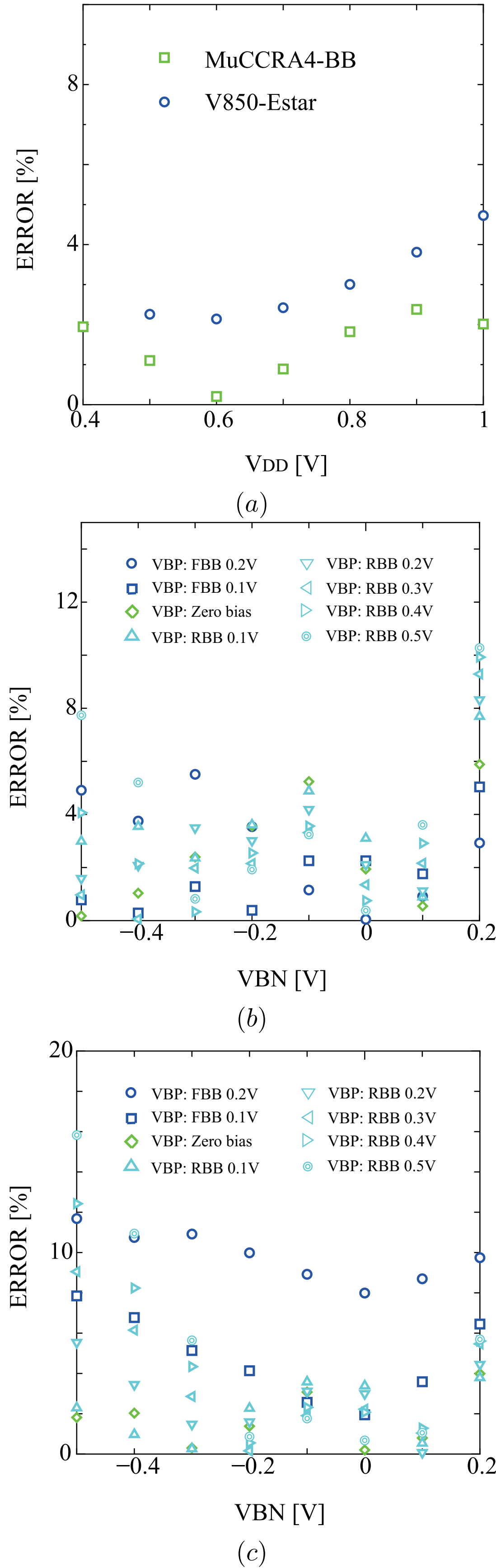


Figure 4.3: Error of the leakage current model (a) power supply dependency (b) body bias dependency :V850-Estar (c) body bias dependency: MuCCRA4-BB.

Table 4.1: Coefficients of the model.

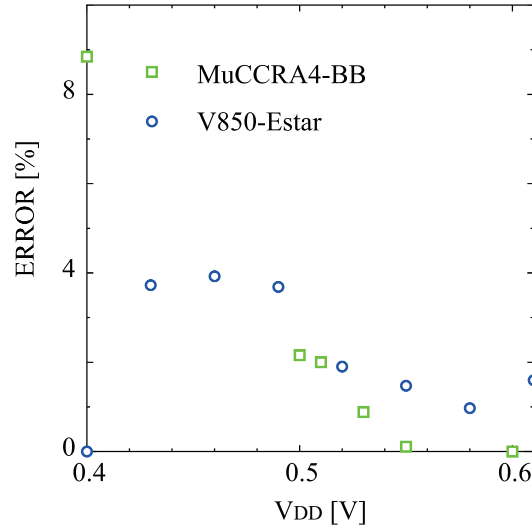
	V850-Estar	MuCCRA4-BB
I_n	2.2137×10^{-3}	3.2250×10^{-5}
I_p	1.5635×10^{-3}	2.4007×10^{-5}
A_n	0.47169	0.56483
A_p	0.39410	0.45140
B_n	2.08830	1.94902
B_p	1.95555	2.00777
x_p, x_m	1.4172×10^{-9}	5.8111×10^{-9}
$K_{\gamma n}$	0.11446	0.13512
$K_{\gamma p}$	0.11098	0.13430
$\alpha_{at}C$	2.0574×10^{-10}	2.1100×10^{-10}

In a similar way, Fig. 4.4 depicts the difference in terms of f_{max} between the real chip values and the calculated ones. Since V850 did not work properly at VBN=0.2, this voltage is omitted from this graph. In Fig. 4.4 (a), the maximum errors of V850 and MuCCRA4 do not exceed the 3.925% and 8.844%, respectively. Moreover, when considering the body bias dependency, as shown in Figs. 4.4 (b) and (c), the errors of V850 and MuCCRA4 are still 7.650% and 3.379%, respectively, at maximum. In average, the errors are only 2.524% (V850) and 1.409% (MuCCRA4), as illustrated in Figs. 4.4 (b) and (c). Similarly to the leakage accuracy, and despite the fact that the model includes some approximations, the average errors in terms of f_{max} are still a few percent. These values are summarized in Table 4.2.

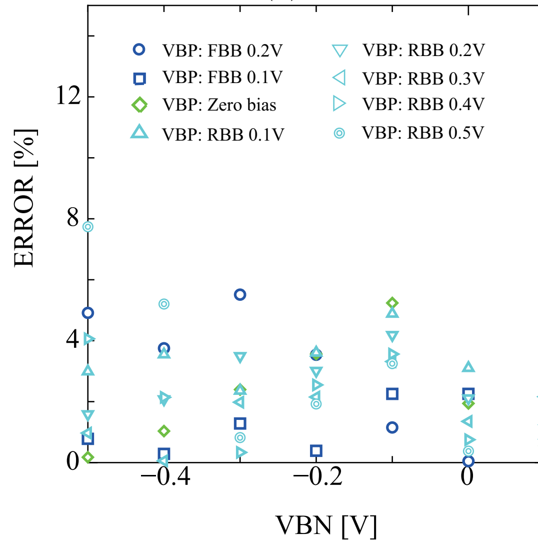
Since the proposed model can represent the f_{max} and the power consumption of a target system, the power optimization can be performed using these models. However, the f_{max} model has a certain error and might cause timing faults in real chips. Therefore, a light-weight real-chip power optimization methodology is proposed. The proposed methodology assures that target systems can surely operate with the calculated voltages.

Table 4.2: Summary of the error of the proposed model.

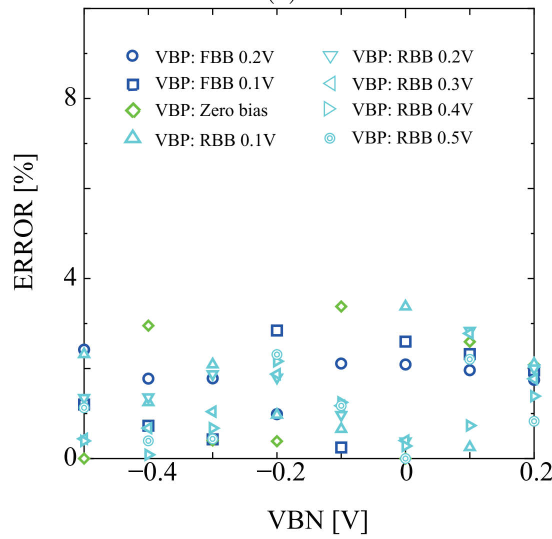
	V850-Estar		MuCCRA4-BB
Leakage model error (Power supply dependency)	Ave.	2.901%	1.480%
	Max	4.727%	2.380%
Frequency model error (Power supply dependency)	Ave.	2.160%	2.332%
	Max	3.925%	8.844%
Leakage model error (Body bias dependency)	Ave.	3.020%	4.354%
	Max	10.27%	15.83%
Frequency model error (Body bias dependency)	Ave.	2.524%	1.409%
	Max	7.650%	3.379%



(a)



(b)



(c)

Figure 4.4: Error of the f_{max} model (a) power supply dependency (b) body bias dependency :V850-Estar (c) body bias dependency: MuCCRA4-BB.

4.2 Power optimization and result

4.2.1 Assumptions and considerations

Before explaining the proposed optimization, we first assume that the body bias and power supply voltages are controlled by DACs which have k voltage steps for the body bias (VBN and VBP) and i steps for the power supply (V_{DD}). In other words, we have $\boldsymbol{VBN} = \{VBN_1, VBN_2, ..., VBN_k | VBN_1 > VBN_2, ..., > VBN_k\}$, $\boldsymbol{VBP} = \{VBP_1, VBP_2, ..., VBP_k | VBP_1 < VBP_2, ..., < VBP_k\}$ and $\boldsymbol{V_{DD}} = \{V_{DD1}, .., V_{DDi} | V_{DD1} < V_{DD2}, ..., < V_{DDi}\}$. Also, we assume that the frequency is controlled with a discrete set $\boldsymbol{F} = \{f_1, ..., f_m | f_n = f_1 + (n-1) \times fstep (n = 1, ..., m)\}$. Here, the frequency is controlled with a constant frequency step $fstep$.

The proposed optimization is performed in two steps. The first step is to optimize the power using the proposed models. This model-based optimization is referred as the *Initial optimization*, hereafter. The *Initial optimization* can be performed with a greedy algorithm. This is because the search space is not so large when the proposed models are used. Indeed, the body bias generator in [55] has 19-steps (25-steps) for the p-well (n-well) voltages. Even if these values are multiplied 3 times ($|\boldsymbol{VBP}| \times |\boldsymbol{VBN}| \times |\boldsymbol{V_{DD}}|$), the search space is still small enough to handle. The second step consists of voltage adjustment with the real-chip timing information to compensate for any possible deviations between the calculated and measured values. This procedure is called *Error adjustment*.

4.2.2 Initial optimization

First, the *Initial optimization* uses the proposed model so that the maximum operational frequencies are calculated for all the given voltage combinations. Then, these calculated frequencies are round-up to the next value in $\boldsymbol{F}$. At each voltage combination, the power consumption is calculated with the corresponding f_{max}. At the end of this calculation, f_m and f_1 are obtained as the highest and lowest frequencies, respectively, among the calculated data considering $fstep$. By grouping the data (the voltage combinations and their corresponding power) with each frequency in $\boldsymbol{F}$, the data structure depicted in Fig. 4.5 is obtained, except for the fourth column. Here, the voltage combinations for VBN, VBP and V_{DD} are denoted by Comb$v$ ($v = 1, ..., k \times k \times i$). $k \times k \times i$ is the total number of the possible voltage combinations with the assumed voltage sources which have k voltage steps for body bias and i for V_{DD}, as previously defined. As shown in Fig. 3.5, there are some voltage combinations which result in the same f_{max}. From these candidates, the minimum-power condition must be selected. This is done by sorting the power consumption of each (V_{DD}, VBN, VBP) combination in the descending order, as shown in Fig 4.5. However, since this selection does not consider the other frequency groups, it is possible that a better candidate in terms of power is located in another group. This means that, for instance, the minimum-power voltage combination to achieve f_{n+1} might also be optimal for f_n.

In order to consider such situations, the minimum-power point at each frequency group is compared with other minimum-power points at higher frequencies. The fourth column of Fig. 4.5 illustrates such comparison in details. Here, the true optimal minimum power consumption for f_{n+1} is denoted as $OptP_{n+1}(f_{n+1})$. The minimum power point at the f_n group (i.e., P_{min-n} in this figure) is compared with $OptP_{n+1}(f_n)$. $OptP_{n+1}(f_n)$ represents

Frequency	Power	Voltage combination	Optimal Power for each frequency
fm	P1 P2 $Pmin_m$ Sort	Comb1 Comb2 Comb3	$OptP_m(f\,\mathrm{m}) = Pmin_m$
⋮	⋮	⋮	⋮
fn+1	Ps Ps+1 $Pmin_n+1$ Sort	Comb$_{\text{u-4}}$ Comb$_{\text{u-3}}$ Comb$_{\text{u-2}}$	$OptP$n+1(f n+1)= min. ($OptP$n+2(f n+1), $Pmin_n+1$)
fn	Ps+3 $Pmin_n$ Sort	Comb$_{\text{u-1}}$ Comb$_{\text{u}}$	$OptP$n(f n)= min. ($OptP$n+1(f n), $Pmin_n$)
fn-1	Ps+5 Ps+6 $Pmin_n\text{-}1$ Sort	Comb$_{\text{u+1}}$ Comb$_{\text{u+2}}$ Comb$_{\text{u+3}}$	$OptP$n-1(f n-1)= min. ($OptP$n(f n-1), $Pmin_n\text{-}1$)
⋮	⋮	⋮	⋮
f1	Pk×k×i-1 $Pmin_1$ Sort	Comb$_{\text{k×k×i-1}}$ Comb$_{\text{k×k×i}}$	$OptP$1(f 1)= min. ($OptP$2(f 1), $Pmin_1$)

Figure 4.5: Data structure obtained by the model. The voltage combinations (i.e., V_{DD}, VBP, VBN), are denoted by Comb$v$ ($v = 1, ..., k \times k \times i$). The power minimum point in each frequency group is represented by P_{min}. The true optimal power consumption at f_n of operational frequency is defined as $OptPn(f_n)$.

the power point at f_n of operational frequency and the voltage combination which is optimal for f_{n+1}. According to the results of this comparison, the voltage combination achieving lower power is selected, and it is considered as the true optimal point for f_n.

Following the above procedures, $OptP_m(f_m)$ is firstly obtained. This is because there is no possibility that the true optimal point belongs to another group as there are no higher frequencies than f_m. Then, the comparison of P_{min-n} and $OptP_{n+1}(f_n)$ is repeated from $n = m - 1$ to $n = 1$. As a result, the fourth column can always store the true-optimal point for each element of $\boldsymbol{F}$. After obtaining the true-optimal voltage combinations, they are sent to *Error adjustment* phase.

4.2.3 Error adjustment

The *Error adjustment* phase is performed only by tuning the body bias voltages as shown in Fig. 4.6. On the target chip, and for each of the target frequencies f_n (n = 1, .., m), it

is checked whether the obtained voltages by the *Initial optimization* surely meet the target performance or not. If it is the case, there is a possibility that the obtained voltage is excessive for the target frequency. Therefore, the body bias should be tuned towards the RBB direction to reduce the leakage power. Either VBP or VBN, which can reduce more leakage current, is controlled here. If the current body bias combination is (VBN_x,VBP_y), the next candidates at this control stage are (VBN_{x+1},VBP_y) and (VBN_x,VBP_{y+1}). Here, the subscript number "$x + 1$" and "$y + 1$" represent the next voltage combination in the RBB direction in the set of $\boldsymbol{VBN}$ and $\boldsymbol{VBP}$, respectively. By calculating and comparing the leakage current at both of the voltage patterns with the model shown in equation (4.2), the voltage combination achieving lower power can be selected. After this voltage selection and control, it is checked whether the new voltage candidate can perform the required frequency or not. If it is not the case, the *Error adjustment* for the frequency f_n is finished and the voltage candidate at the previous iteration is chosen. On the other hand, if the timing is met, the voltage control performs the same comparison for the next iteration.

In the case where the first f_{max} test of the *Error adjustment* is not passed, the result of the *Initial optimization* has to be adjusted towards the FBB direction. In order to decide which VBN or VBP should be controlled, the same procedure for the "RBB adjustment" is adopted, as represented in Fig.4.6. If the current body bias combination is (VBN_x,VBP_y), the next candidates at this control stage are (VBN_{x-1},VBP_y) and (VBN_x,VBP_{y-1}). In this figure, the subscripts "$x - 1$" and "$y - 1$" represent the next voltage combinations in the FBB direction in the $\boldsymbol{VBP}$ and $\boldsymbol{VBN}$ sets, respectively. By calculating and comparing the leakage currents for both of the two candidates, the appropriate one can be selected. This "FBB adjustment" is repeated until the timing is met. After the "FBB adjustment", "RBB adjustment" is performed since there is a possibility that the required frequency can also be met with less power by moving towards the RBB direction from the current body bias combination. As a result, the proposed error compensation keeps the leakage to its smallest while meeting the required frequency.

4.2.4 Optimization results

In this subsection, the effectiveness of the proposed optimization is evaluated. Although the proposed *Error adjustment* can be implemented as an on-chip controller, as explained later in Section 4.2.6, the efficiency of the proposed optimization based on a simple program implemented in C language is shown in this evaluation.

In this experiment, we assume that the number of the body bias steps (k) is eight for each of VBP and VBN, similarly to the experiment in Section 3.1. Thus, we have $\boldsymbol{VBP} = \{0.2, 0.3, .., 0.9\}$ and $\boldsymbol{VBN} = \{0.2, 0.1, ..., -0.5\}$ for V850, and $\boldsymbol{VBP} = \{0.4, 0.5, ..., 1.1\}$ and $\boldsymbol{VBN} = \{0.2, 0.1, ..., -0.5\}$ for MuCCRA4-BB. Also for this experiment, the number of the voltage steps for V_{DD}, is assumed to be two: $\{0.4, 0.5\}$ for V850 and $\{0.5, 0.6\}$ for MuCCRA4. Although the number of the voltage steps is limited in this experiment, the author believes it is enough to observe the validity of the proposed method. As for the frequency parameter, the discrete step for the operational frequency is defined as 1MHz. Table 4.3 summarizes the used voltage sets in this experiment.

The C program for the evaluation emulates both *Initial optimization* and *Error adjustment* phases of the proposed method. As described before, the *Initial optimization* requires

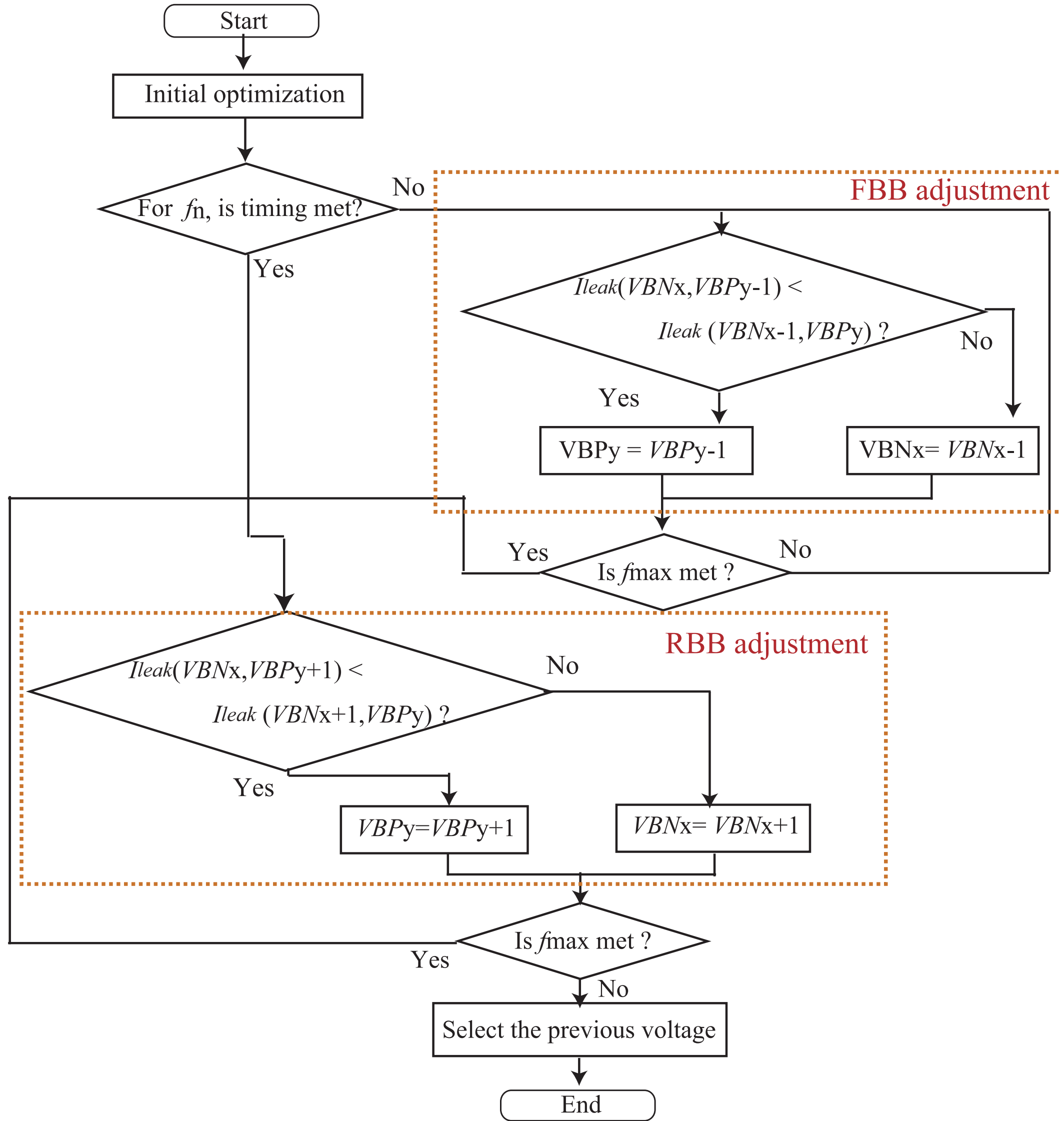


Figure 4.6: Error compensation step in the proposed optimization.

the model coefficients listed in Table 4.1, which are inputted to the program. After the *Initial optimization*, real chip timing information for each of the voltage candidates is needed for the *Error adjustment*, as depicted in Fig. 4.6. The measured f_{max} is also sent to the C program. After running the program, the final optimized voltage combination (i.e., post-Error adjustment) is obtained.

As previously mentioned, the proposed power optimization is based on models and an error compensation algorithm. Consequently, some deviations might occur when compared to the optimization which is completely done using chip measurements. In order to show such deviations, the optimization without the models is also conducted for the symmetric and asymmetric BBC. That is, the greedy optimization in Fig. 4.5 is conducted with real

Table 4.3: Used Voltage sets for the proposed optimization evaluation.

V850-Estar			MuCCRA4-BB		
V_{DD}	VBN	VBP	V_{DD}	VBN	VBP
0.4 0.5	0.2	0.2	0.5 0.6	0.2	0.4
	0.1	0.3		0.1	0.5
	0	0.4		0	0.6
	-0.1	0.5		-0.1	0.7
	-0.2	0.6		-0.2	0.8
	-0.3	0.7		-0.3	0.9
	-0.4	0.8		-0.4	1.0
	-0.5	0.9		-0.5	1.1

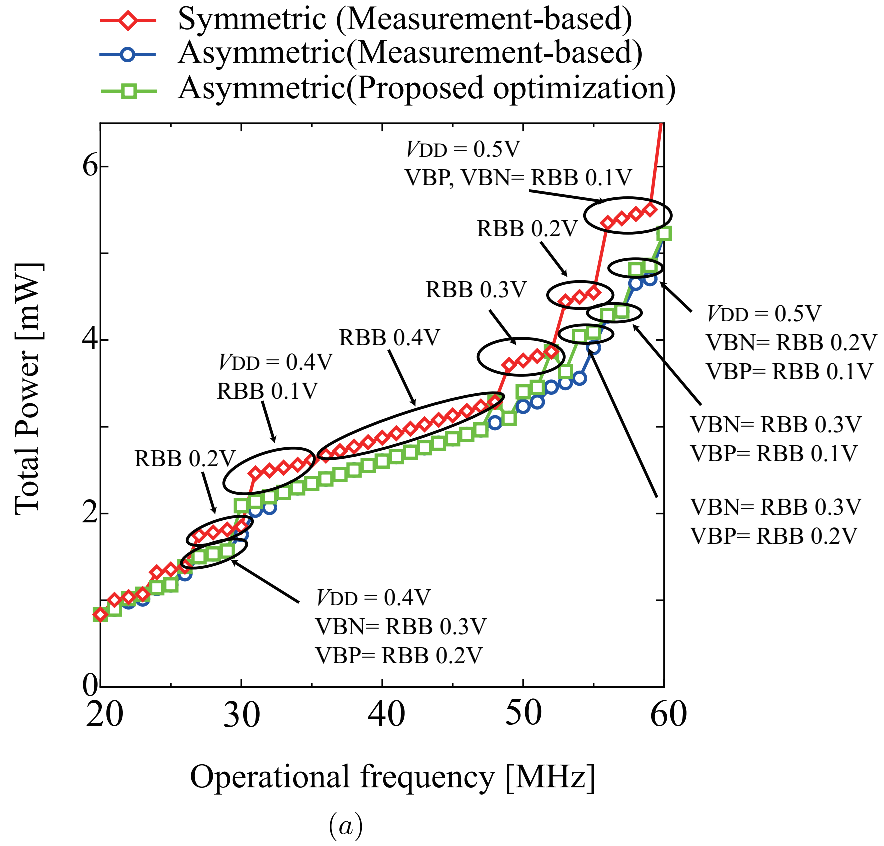
chip measurements. Based on the measurement results of f_{max} and their corresponding power consumptions for all the voltage combinations, the data structure shown in Fig. 4.5 is constructed. Using this structure, the optimized voltage combination for each frequency in $\boldsymbol{F}$ (i.e., f_n) is extracted, as previously explained in Section 4.2.2. Hereafter, this optimization is referred as "measurement-based optimization", for both symmetric and asymmetric.

The total power comparison results between the asymmetric and symmetric BBC are shown in Fig. 4.7. The plotted power consumption includes both switching and leakage power.

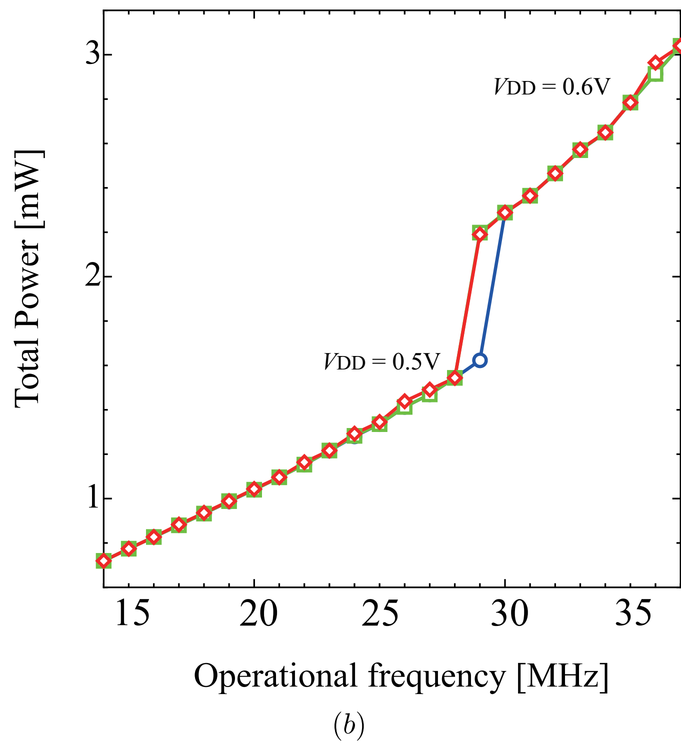
As shown in Fig. 4.7 (a), the proposed optimization can lower the power consumption when compared to the symmetric BBC. For example, at 56MHz, the symmetric BBC needs to set both VBN and VBP to 0.1V of RBB. On the other hand, by considering the asymmetric conditions, the proposed algorithm finds a more optimal condition on which VBN is 0.2V of RBB and VBP is 0.1V of RBB. In average, 9.617% of power consumption can be reduced. Asymmetric conditions are especially useful for the high-performance region where leaky conditions manifest. For instance, at 60MHz, the proposed method can reduce up to 22.77% of power consumption compared to symmetric BBC. Although the proposed approach exhibits some power overhead (error) compared to the measurement-based optimization, the average is only around 2.56%.

On the other hand, in Fig. 4.7 (b), only a few differences can be observed between the proposed asymmetric BBC and symmetric BBC. In fact, the average total power reduction in this graph is only 0.34% when compared to the symmetric BBC. Even when the maximum reduction is considered, it is only 1.77% (26MHz of operational frequency). Since MuCCRA4-BB is a switching current dominant system, the effect of the leakage reduction is quite negligible. Indeed, the large power step in this graph is caused by altering the V_{DD} voltage. In other words, the proposed approach can efficiently reduce the power consumption in leakage dominant systems. On the other hand, if the target system is a switching current dominant, the efficiency of asymmetric BBC is reduced, and symmetric BBC can be enough to optimize its power consumption.

Thanks to the proposed model, the power supply voltage can also be optimized unlike [18]. Otherwise, a fixed V_{DD} may degrade the benefits of asymmetric BBC. In order to show



(a)



(b)

Figure 4.7: System total power consumption comparison results:(a) V850 (b) MuCCRA4-BB.

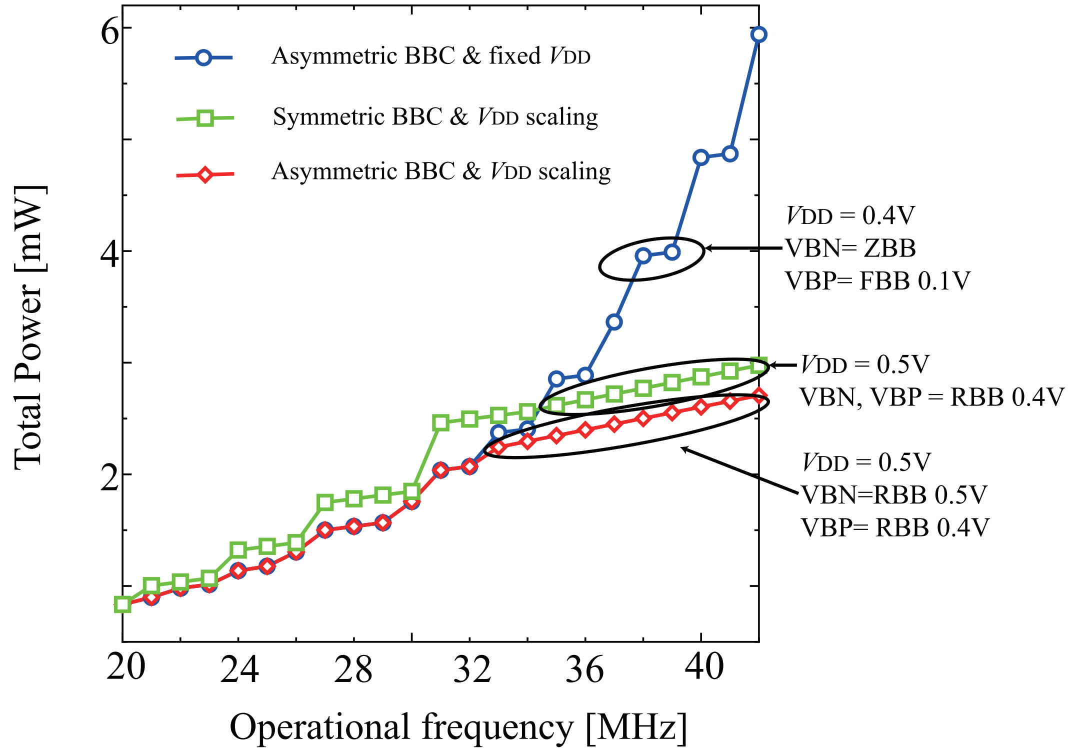


Figure 4.8: Effect of V_{DD} voltage scaling.

the importance of scaling V_{DD}, Fig. 4.8 compares the power consumption among the case of "Symmetric BBC & V_{DD} scaling", "Asymmetric BBC & fixed V_{DD}" and "Asymmetric BBC & V_{DD} scaling". Here, V850 is used as a case study and the values plotted in this graph are obtained using the measurement-based optimization. At low performance conditions, the asymmetric BBC can surely reduce the power consumption compared to the symmetric one; however, the relationship is inversed at higher operating frequencies when V_{DD} is not scaled. The power consumption of "Asymmetric BBC & fixed V_{DD}" at 32MHz is 20.5% lower than that of "symmetric BBC & V_{DD} scaling"; but, it becomes 49.9% higher at 42MHz. This is because excessive FBB causes large leakage overhead and offsets the gain of the asymmetric BBC. For example, the "Asymmetric BBC & fixed V_{DD}" at 38MHz adopts ZBB of VBN and 0.1V FBB of VBP. On the other hand, "Symmetric BBC & V_{DD} scaling" sets the both VBN and VBP to 0.4V RBB. Nevertheless, the proposed methodology can avoid this situation and further reduce the power consumption.

4.2.5 Body bias asymmetricity

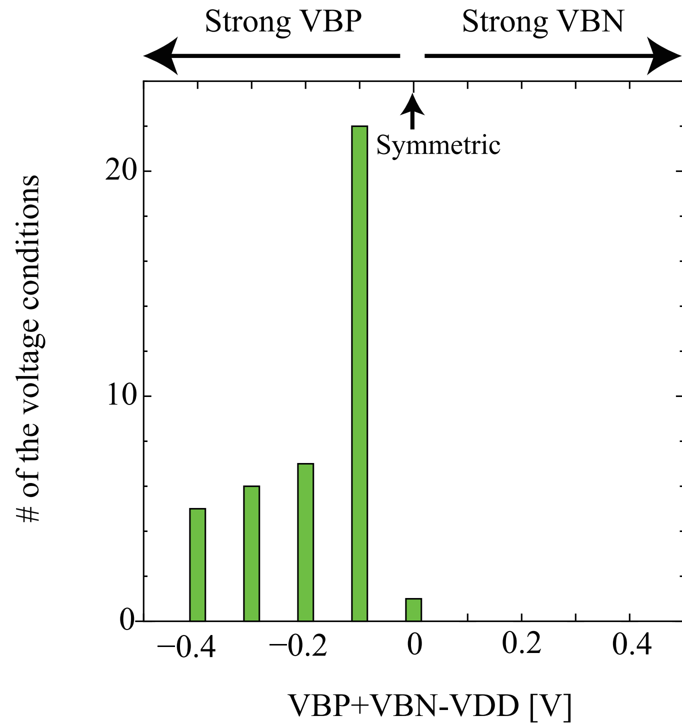
One of the straightforward ideas for asymmetric BBC is to extend the results obtained by the conventional symmetric BBC with some equations. Hereafter, it is demonstrated that such method is quite difficult in practice. In order to discuss this matter, we define "Body Bias Asymmetricity" (BBA) as:

$$BBA = VBP + VBN - V_{DD} \tag{4.9}$$

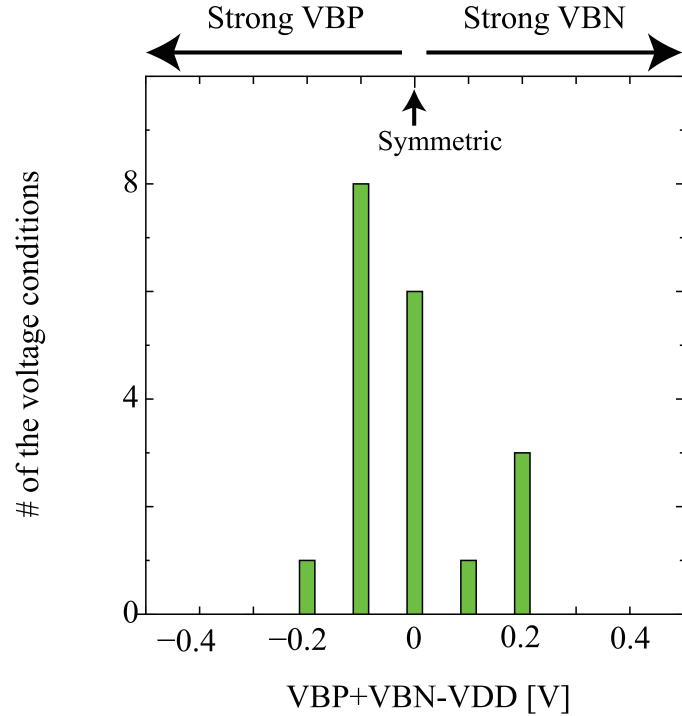
BBA represents the voltage balance between VBP and VBN. When VBP is set to be more towards the FBB direction than VBN, *BBA* is lower than zero. On the other hand, when VBN is set to be more towards the FBB direction than VBP, *BBA* is higher than zero. When the body bias combination is symmetric, *BBA* is equal to zero. For example, when a body bias condition of $VBP = 0.4$V, $VBN = -0.1$V and $V_{DD} = 0.4$V is used, VBP is zero bias and VBN is 0.1V of RBB. In this case, we obtain $BBA = VBP + VBN - V_{DD} = -0.1V$ since VBP is asymmetrically set to 0.1V towards FBB than VBN.

Using the above definition, the *BBA* values of the measurement-based optimal voltage combinations, used for V850 and MuCCRA4 in Fig. 4.7, are calculated. The distribution maps of these calculated values are shown in Fig. 4.9. The number of asymmetric voltage combinations for each *BBA* value (vertical axis) is also extracted from Fig. 4.7.

As can be seen in these plots, the BBA tendency is quite different in the two evaluated systems. Highly unbalanced voltage combinations (e.g., $BBA = -0.4$) are observed in the V850 case, while only near balanced combinations (e.g., $-0.2 \leq BBA \leq 0.2$) are used for MuCCRA4. Also, for V850, the results show that VBN should be set more towards the RBB direction than VBP while, for MuCCRA4, stronger VBN can be optimal at some points. Hence, the asymmetricity is highly dependent on the architecture of the target chip. Indeed, the used standard-cells in each design vary from one system to another. It means that the leakage dominant polarity (pMOS or nMOS) might be changed by this parameter because the ratio of the number of the used nMOS and pMOS is different. Moreover, even if we can notice which nMOS or pMOS leakage current is dominant, the degree of asymmetricity is not always the same as shown in Fig. 4.9. For example, nMOS leakage current is dominant in V850 because Strong VBP is utilized rather than VBN. Nevertheless, the distribution of the asymmetricity varies from $BBA = 0$V to $BBA = -0.4$V. Therefore, it is difficult to simply formulate these factors and extend the results of the optimized symmetric condition to the asymmetric one. In conclusion, when the asymmetric BBC is required, it has to be considered as an optimization phase.



(a)



(b)

Figure 4.9: Voltage asymmetricity of the optimization results :(a) V850 (b) MuCCRA4.

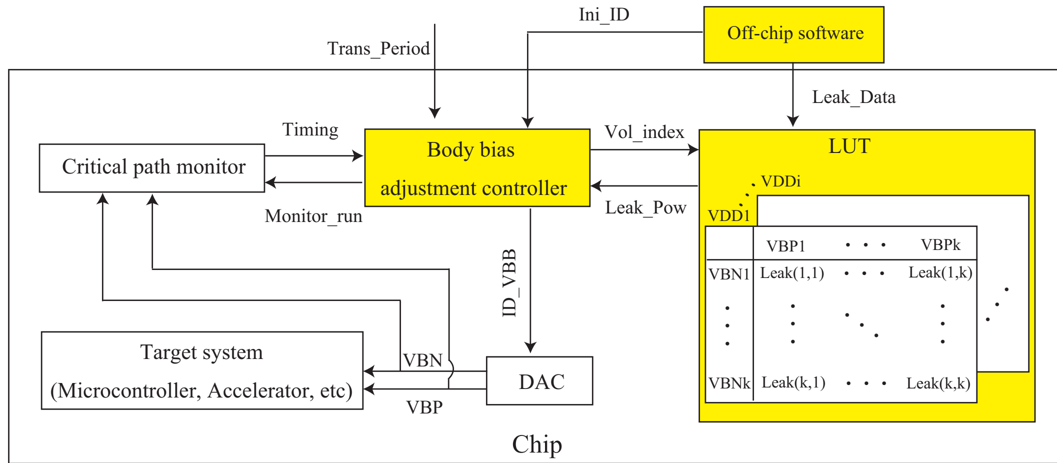


Figure 4.10: On-chip implementation of the *Error adjustment* phase. The highlighted parts are the additional components to the conventional body bias control scheme.

4.2.6 Hardware implementation and overhead analysis

Although the *Initial optimization* of the proposed method can be carried out with models, the *Error adjustment* phase needs to check the timing information at each of the voltage-adjustment iteration. It also increases the testing time when it is carried out manually. Nevertheless, since the timing information can be easily obtained using critical path monitors which are embedded in conventional processors [45, 73, 74], the error adjustment scheme can be implemented by an on-chip controller, as shown in Fig. 4.10. In addition to the conventional body bias scheme, it can be implemented with an additional controller and Look Up Table (LUT). The LUT stores the leakage power for all patterns of possible voltage combinations. Off-chip software can calculate this data and send it to the on-chip LUT. Also, the *Initial optimization* can be performed by an off-chip software. So, the initial voltage ID ("Ini_ID") obtained by the *Initial optimization* for the on-chip DAC is sent to the "Body bias adjustment controller".

After that, the "Body bias adjustment controller" checks the timing information at the body bias voltage of "Ini_ID" by activating "Monitor_run". According to the information of "Timing", either an "FBB adjustment" or "RBB adjustment" (previously shown in Fig. 4.6) is executed. In order to perform this adjustment, the power information is required, as shown in Fig. 4.6. By sending the index value of the target voltage ("Vol_Index") to the LUT, it replies with the leakage power ("Leak_Pow"). Based on the received data, the controller decides the body bias voltage and send the new voltage ID ("ID_VBB") to the DAC. According to the "ID_VBB", the DAC changes the supplied body bias voltages accordingly. Since body bias transition requires a certain time, the "Body bias adjustment controller" waits during the transition time which is defined by "Trans_Period". Later, it asks the timing information of the target system again. From this information, the controller decides whether the next iteration of the voltage adjustment is needed or not. This procedure is repeated until the "RBB adjustment", depicted in Fig. 4.6, is finished.

Although adding the on-chip body bias controller greatly simplifies the power optimization, it causes a certain power overhead that may hinder the intended efficiency of the power optimization. For this reason, the additional parts (highlighted in yellow in Fig. 4.10) are implemented with the SOTB 65-nm technology to evaluate their overhead. The additional on-chip parts are designed in Verilog-HDL and the LUT was configured in order to treat the voltage-sets represented in Table 4.3. In addition, Synopsys IC-Compiler and Design-Compiler are used as the layout and synthesis tools, respectively. Since the capacitor on the well is large, the transition time of the BBC is slow. Hence, the operating frequency of the body bias controller does not have to be fast, and 2MHz of operational frequency is chosen in order to reduce the power overhead. The power overhead for the error adjustment process is obtained by IC-Compiler. The power evaluation of the designed on-chip optimization modules (with the high threshold voltage in Table 3.1) showed that it exhibits 23.43 μW of power overhead at 0.55V of supply voltage.

Considering the case of V850, for example, the proposed optimization reduces the power consumption by up to 22.77% compared to the symmetric BBC, as previously explained. Even if the power overhead is added to this result, it is still 22.43%. Moreover, when considering the power overhead, the average power reduction from the symmetric BBC is still 8.617%. It is important to mention that the power consumption for V850 is obtained with 0.4V and 0.5V of V_{DD}, as depicted in Table 4.3. Hence, the power overhead which is obtained by 0.55V of V_{DD} is a pessimistic evaluation. Therefore, the overhead of the on-chip *Error adjustment* mechanism does not hinder the efficiency of the proposed optimization. Furthermore, implementing such a mechanism tremendously reduces the testing cost of the chip measurements. Note that, the difference of the threshold voltage between the controller and V850 can be easily managed. This is because, as investigated in some studies [75, 76], it is possible to implement a multi-threshold voltage design in a chip. In other words, the threshold voltage mismatch does not hinder the obtained results.

4.2.7 Threshold voltage variations

VLSI systems suffer from process and temperature variations, and the body bias control plays an important role in adjusting them. However, it is tedious to obtain the model coefficients for every variated chip. Instead, such variations can be adjusted by the error adjustment step in Fig. 4.6 to a certain degree. This means that "$Ileak$" in Fig. 4.6 without V_{TH} deviations is utilized even for variated chips.

In order to observe how this step works under the chip variations, the error adjustment of V850 is emulated on the condition that the threshold voltages have $\pm10\%$ deviation from the predefined values. This is because, the process and temperature variations shift the transistor threshold voltages. Although the temperature affects the mobility, we ignore this effect for the sake of simplicity. We label the variations for nMOS/pMOS as FF, and SS where S, and F represent the slow, and fast conditions, respectively.

Unless a transistor which can be accessed from outside the chip is implemented, it is difficult to check the threshold shift with a real VLSI system chip. Therefore, to emulate the real chip values of "$fmax$" used to perform the error adjustment (depicted in Fig. 4.6), equations (4.6), (4.7), and (4.8) are slightly modified. Also, equation (4.2) is changed to calculate the final optimization results under the variations. When the threshold voltages have

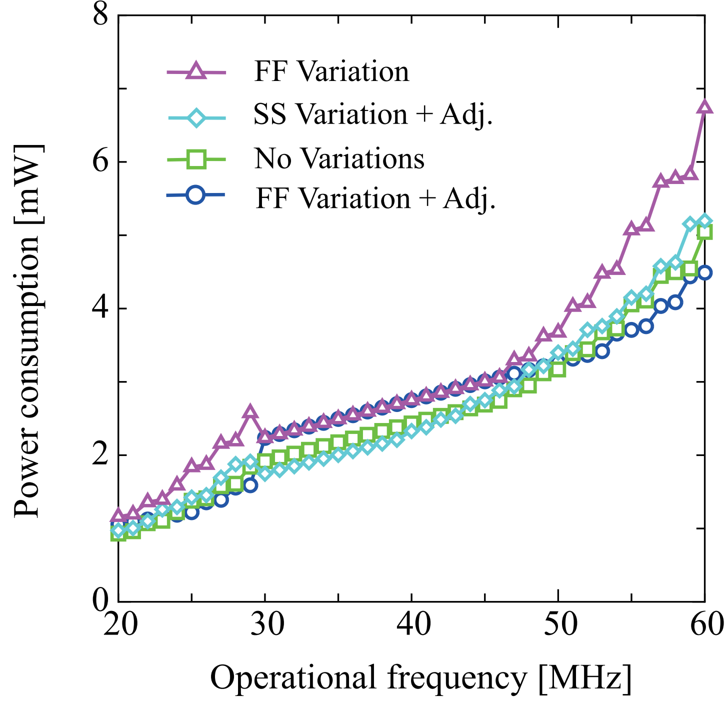


Figure 4.11: Power optimization results under the threshold variations

variations, the subthreshold leakage current is changed along with an exponential function. This leakage current is dominant compared to the others, hence, the model can be extended as:

$$I_{leak+\Delta} = I_n 10^{A_n V_{DD} + B_n VBN + \Delta_n} + I_p 10^{A_p V_{DD} + B_p (V_{DD} - VBP) + \Delta_p}, \tag{4.10}$$

Here, Δ_n and Δ_p represent the chip variation for nMOS and pMOS leakage current, respectively. The f_{max} model including the threshold variation is:

$$f_{max+\Delta} = \frac{1}{t_{dp+\Delta} + t_{dn+\Delta}}, \tag{4.11}$$

$$t_{dp+\Delta} = \frac{xpV_{DD}}{(V_{DD} - |V_{t0p}| + \Delta V_{tp} + K_{\gamma p}(V_{DD} - VBP))^{\alpha}}, \tag{4.12}$$

$$t_{dn+\Delta} = \frac{xnV_{DD}}{(V_{DD} - V_{t0n} + \Delta V_{tn} + K_{\gamma n} VBN)^{\alpha}}. \tag{4.13}$$

Here, ΔV_{tp} and ΔV_{tn} represent the threshold variation of pMOS and nMOS, respectively.

Fig. 4.11 shows the optimization results under the variations. As reference values, the power consumptions without the variations (“No Variations” curve) are also depicted. These values can be obtained by the *initial optimization* since no variations are included. The power consumption at the FF condition without adjustment (“FF Variation” curve) is

clearly the largest. This is because, although the power is optimized for TT conditions, the obtained conditions are excessive for the FF conditions. Moreover, this causes the large power loss as shown at 29MHz of the operational frequency because the balance between the switching and leakage current differs by the process variations. However, the error adjustment ("FF Variation + Adj." curve) can converge the excessive power around the values without variations. Considering the adjusted value at 60MHz, 33.3% of power consumption is reduced after the variation adjustment of FF. Also, if the chip is varied to SS, the target system does not work properly without the error adjustment. Nevertheless, the error adjustment ("SS Variation + Adj." curve) can tune the body bias so that the target system can operate at the target frequencies. This adjustment comes with a reasonable power overhead. In fact, when compared to the case without variations, the largest overhead is 16.65% at 28MHz.

4.3 Noise margin

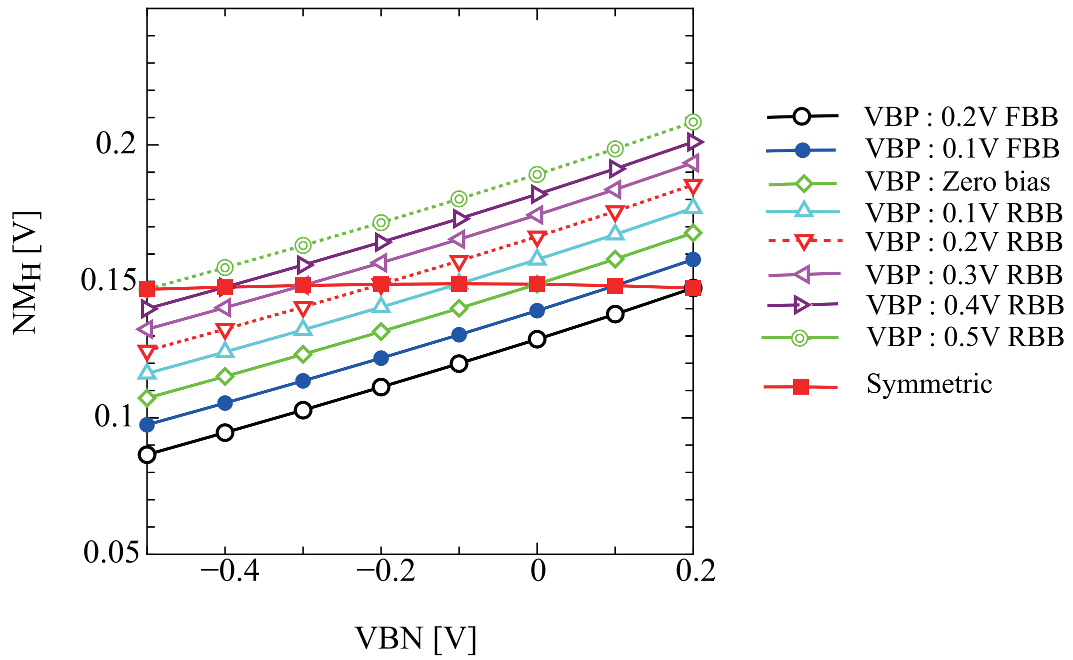
The noise margins can be reduced at the asymmetric body bias conditions, but, they still exist. The noise margin is defined as the voltage difference between the worst logic output voltage and the acceptable input logic voltage. For logic "0" (NM_L), it is:

$$NM_L = V_{IL} - V_{OL} \tag{4.14}$$

where V_{IL} and V_{OL} are the maximum input and output voltages as logic "0", respectively. Also, the margin for logic "1" (NM_H) is:

$$NM_H = V_{OH} - V_{IH} \tag{4.15}$$

where V_{OH} and V_{IH} are the minimum output and input voltages as logic "1", respectively [13]. In order to observe these noise margins at the asymmetric conditions, HSPICE simulations with an inverter in the SOTB standard cell library are conducted. The obtained NM_L and NM_H are depicted in Fig. 4.12 with 0.4V of V_{DD}. The body bias voltages in this simulation range from 0.2V of FBB to 0.5V of RBB with 0.1V of a voltage step to make it consistent with the conducted experiments in this thesis. As can been seen from the figures, NM_L and NM_H are decreased at the asymmetric body bias conditions. All of the obtained NM_Ls are around 0.17V at the symmetric conditions, while the worst case of the asymmetric condition is around 0.1V. Similarly, NM_Hs at the symmetric conditions are around 0.15V; but, the minimum case of the asymmetric body bias condition is around 0.08V. Furthermore, the noise margin can also be defined for the latch cell as depicted in some well-known works [77, 78]. It is called "Static noise margin" (SNM). SNM can be obtained by drawing the butterfly curve and the largest square inside the butterfly curve as shown in Fig. 4.13. The side length of the smaller square is defined as the static noise margin. Here, V_{DD}=0.4V and zero bias are used for this figure. The obtained static noise margins for the latch cell are shown in Fig. 4.14. 0.4V of V_{DD} is used here. As shown in this graph, when compared to the symmetric conditions, some of the static noise margins are degraded at the asymmetric body bias pairs. In fact, the smallest noise margin of the asymmetric BBC is 82.5% of the worst case of the symmetric BBC. Considering these graphs, the noise margin is slightly degraded with introducing asymmetric BB. If these degradations are allowed, the proposed approach offers a reasonable power reduction.



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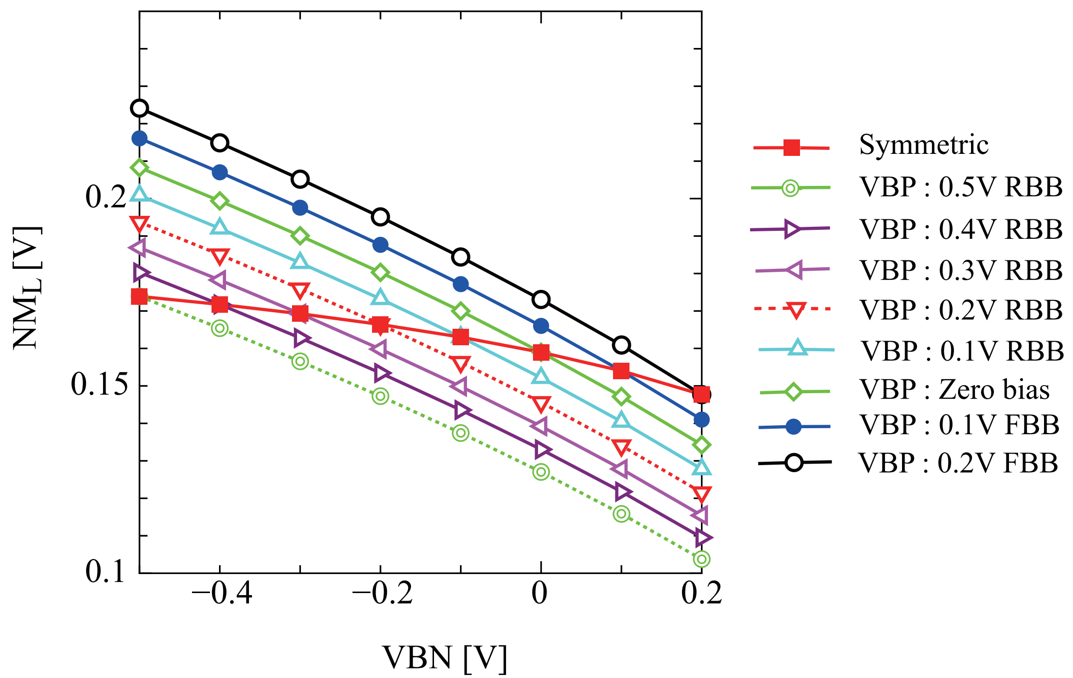


(b)

Figure 4.12: Simulated noise margin: (a) NM_H (b) NM_L.

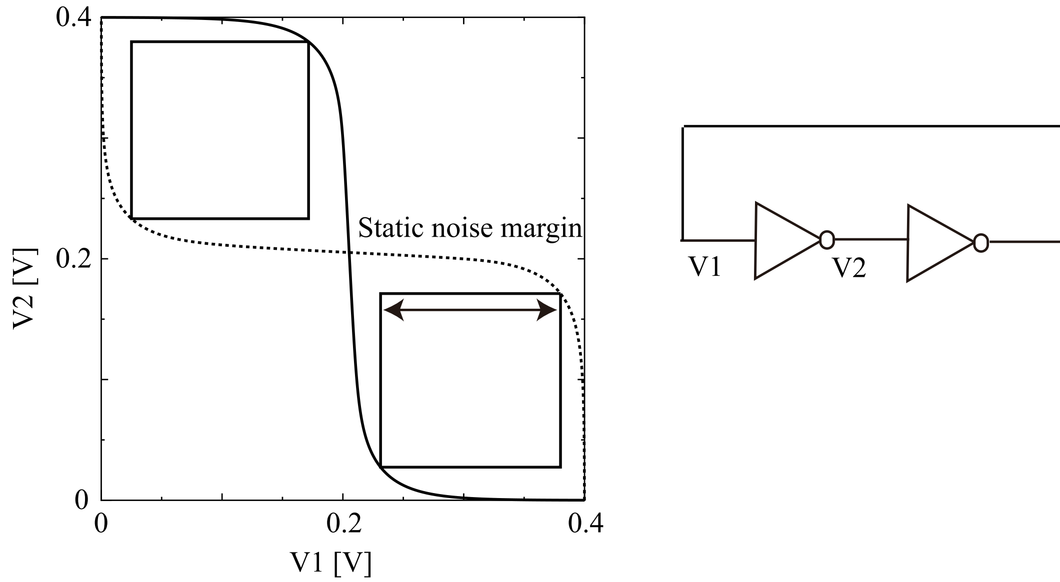


Figure 4.13: Definition of the butterfly curve and static noise margin

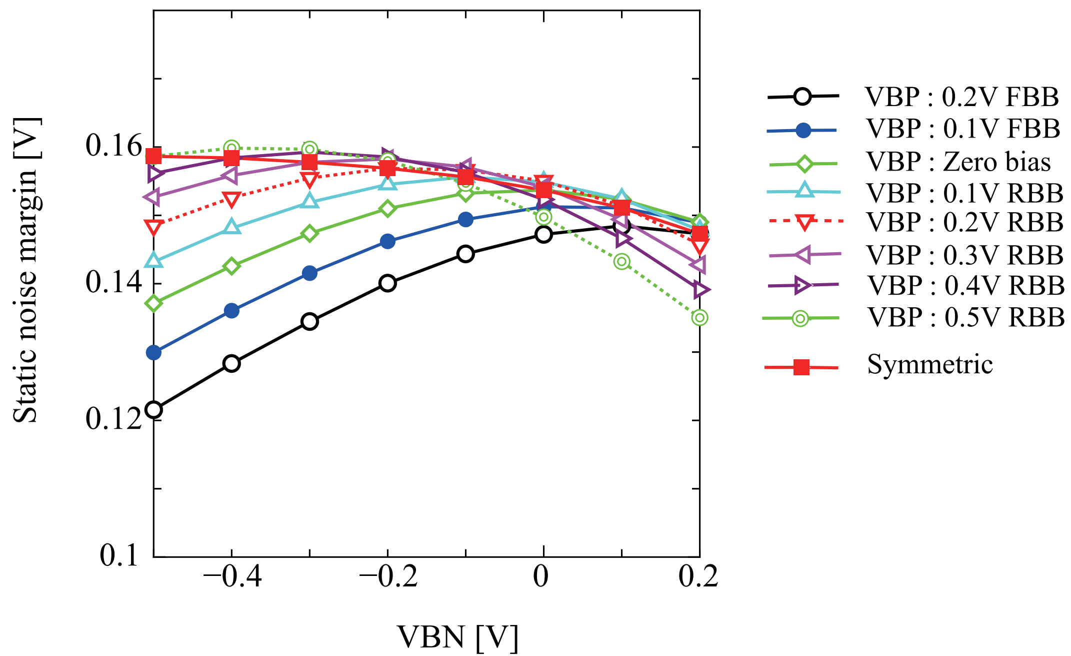


Figure 4.14: Simulation results of the static noise margin: V_{DD}=0.4V

4.4 Summary

In this chapter, a power optimization based on asymmetric body bias control is proposed and evaluated. First of all, simple leakage power and performance models are proposed to perform the optimization. The proposed models can be simply utilized with practical systems because its coefficients can be extracted from real chip measurements, thus, guaranteeing high accuracy. The accuracy of the proposed model is observed with two different types of the systems: an embedded microcontroller (V850-Estar) and a dynamically reconfigurable processor (MuCCRA4-BB). The conducted experiments proved that the body bias and power supply dependency for the delay and power are correctly modeled with a few percent of error in average.

Moreover, a power optimization methodology based on these models is proposed. Thanks to the models, the proposed optimization does not require a brute force search using on-chip measurements. In addition, it achieves higher power reduction than the case where only symmetric voltage combinations are considered. In fact, when compared to symmetric BBC, the proposed optimization achieves an average of 9.617% of power reduction which can reach up to 22.77% in the case of V850. On the other hand, the experimental results reveal that the efficiency of asymmetric BBC is reduced when applied to a switching current dominant system. Furthermore, since the model for the delay has certain errors from real chip values, the proposed methodology incorporates a light-weight error compensation scheme. Thanks to this scheme, the power optimization was performed with 2.560% of error (i.e., power overhead) from the measurement-based optimization which requires a tremendous testing time.

5

Digitally Assisted Automatic Body Bias Tuning Scheme

5.1 Digitally Assisted Automatic Body Bias control scheme (DABT)

DABT is based upon digital circuit components for controlling body bias instead of using analog DAC circuits. Fig. 5.1 depicts a simplified block diagram of the proposed system architecture. It consists of a target system (e.g., microcontroller, accelerator, etc), a charge-pump circuit, a performance emulator of the target system, a discharge circuit, a phase-frequency detector, and a wake-up detector. All of these components, except for the charge-pump, can be implemented with digital circuits, as shown in this section. Before describing the detailed implementation of DABT, the conceptual idea is firstly shown.

5.1.1 DABT concept overview

A charge-pump is a voltage generator circuit whose output voltage is generated by accumulating electric charges into a capacitor. It can generate Reverse Body Bias (RBB) by charging the well capacitors. Although a charge-pump cannot precisely control the output voltage, its power overhead is quite small [79, 80]. Thus, it can be suitable for low-power and low supply voltage systems.

In order to regulate the output voltage of the charge-pump, the proposed system employs a controller which is depicted in Fig. 5.1 as "Bias controller". When the target system is in the standby state, it controls the charge-pump so as to supply a strong RBB to the target system. Hereafter, this state of DABT is referred to as the "standby mode". When the target system operates at a certain frequency, the controller adjusts the body bias voltages in order to satisfy the required performance. This state is called "active mode" for the remaining parts of this thesis. When the frequency is altered at the active mode, the controller automatically changes the body bias voltages to adjust to the new value. For this purpose,

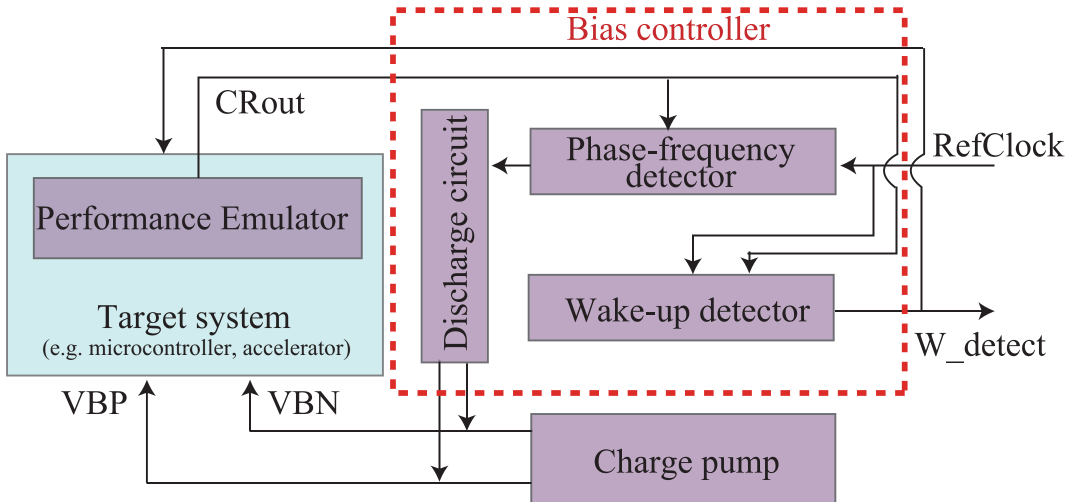


Figure 5.1: Simplified block diagram of DABT

the performance emulator monitors the current maximum operational frequency (f_{max}) of the target system and outputs it to “CRout” as a rail-to-rail oscillation signal, as depicted in Fig. 5.1. Here, the same body bias voltages provided to the target system are supplied to this performance emulator. The period of “CRout” is designed so as to track the maximum operational clock of the target system with the given body bias voltage.

The phase-frequency detector compares the reference clock (represented by “RefClock” in Fig. 5.1) with the output of the performance emulator “CRout”. The period of “RefClock” is set to be a system clock which enables the required performance. When “CRout” is slower than “RefClock”, discharge switches in the bias controller release the electric charges of the body bias to change it towards the forward direction. On the other hand, if “CRout” is faster than “RefClock”, discharge switches are opened and the well capacitor is charged by the charge-pump to change it towards the reverse direction. In other words, the controller adjusts the electric charges of the well and, finally, the bias voltages are set to be around the voltage which can keep the required speed.

Note that when the oscillation frequency of “RefClock” is variable (e.g., Dynamic Frequency Scaling), the phase-frequency detector can still detect it and the body bias voltages can be automatically adjusted. Moreover, since “RefClock” is an oscillation signal like a common system clock, this architecture does not need any additional pulse signal for various operational frequencies. It is also important to mention that since the body bias voltages are controlled by “RefClock” and the phase-frequency detector, we do not have to define a voltage step unlike the other DAC-based systems.

The wake-up detector observes the body bias condition when the target system is changed from low performance, or standby mode, to high. The target system is ready to work with the required clock frequency after the body bias voltages have been changed. In DABT, as shown in Fig. 5.1, the “W_detect” signal provides such information. When “RefClock” is increased, “CRout” tracks it immediately by changing the body bias to the forward direction, and with a certain time margin after “CRout” reaches “RefClock”, “W_detect” is asserted to inform that the system is ready to be used.

5.1.2 Performance emulator and Charge-pump

Fig. 5.2 depicts the body bias generator adopted in the proposed DABT, called VBBGEN [80]. VBBGEN is a Dickson type 6-stage charge-pump consisting of a series of diodes and capacitors. [1] It accumulates electronic charges in each capacitor with complementary oscillation signals ("CLK" and "CLKB") and outputs a higher voltage than V_{DD} or a lower voltage than V_{SS}. Here, "CLK" and "CLKB" are generated by internal ring oscillators. For example, when "CLK" is low in the charge pump for VBP, the voltage of node *N1* is equal to $V_{DD} - |V_{TH}|$, then, *M1* is cut off. Next, "CLK" goes high, the voltage of *N1* rises to $2V_{DD} - |V_{TH}|$ and the voltage of *N2* is charged to $2(V_{DD} - |V_{TH}|)$. This procedure is repeated for each capacitor, and a certain voltage output is generated. Similarly, the charge pump for VBN generates the negative voltage with a -$(V_{DD} - |V_{TH}|)$ step. The output voltages are also delivered to the internal ring oscillators. Hence, when deep reverse bias for the standby mode is supplied, the oscillation frequency is also lowered and the power overhead from the oscillators can be reduced. Fig. 5.3 shows the simulated waveform of VBBGEN designed with SOTB 65-nm technology (0.6V of V_{DD}). As can be seen, the higher (lower) voltage than 0.6V (0V) is obtained for the reverse bias on VBP (VBN). Since the impedance of the well is high [16], the ripples from the charge pumps can be smoothed out. Conventionally, since the typical power supply voltage and the original threshold of recent transistor technologies are lowered, the leakage current can flow from each capacitor to its previous stage, even through diodes are in the cut-off state. This degrades the output voltage and the efficiency of the charge-pump. Nevertheless, VBBGEN can avoid this problem since RBB is applied to cut-off diodes by feeding-back the voltage generated by the later stage, as depicted in Fig. 5.2 by the green-shaded region in the middle of "Charge pump for VBP" and "Charge pump for VBN". That is why VBBGEN is not influenced by the leakage current, and can generate a high voltage (or low voltage at the VBN side). In this implementation, VBBGEN always operates and accumulates electrical charges for the well. Nonetheless, when DABT is in the active mode, the discharge circuit, explained later, can sink the charge and converge the voltage in order to set the performance delay to meet the required speed.

Note that VBBGEN needs to output a larger current than that of the leak-out current at the well diode. Otherwise, adequate electrical charges are not deposited and the RBB cannot be obtained. Therefore, the VBBGEN is implemented so as to control the body bias of processor systems [80]. The used VBBGEN is not optimized for a specific design. Nevertheless, it was designed to drive a few nF of well capacitance while considering a few nA of leak-out current from the wells.

As for the performance emulator, represented in Fig.5.2, a simple ring oscillator is implemented. The number of the inverter stages are decided by referring the delay of a 5-stage standard pipeline MIPS, as shown later. Note that the only requirement for implementing a performance emulator is that the period of the digital output signal "CRout" should match the critical path delay of the target system.

[1] The basic V_{DD} voltage in the used PDK and the maximum RBB shown in [16] were respectively defined as 0.55V and 2.5V as explained later. Therefore, the number of the charge pump stages was decided to six, so as to achieve this maximum RBB at around 0.55V of V_{DD}. If stronger RBBs at lower V_{DD} are required, the number of stages should increase. When weaker RBBs at higher V_{DD} are needed, the number of the charge pump stages can be decreased.

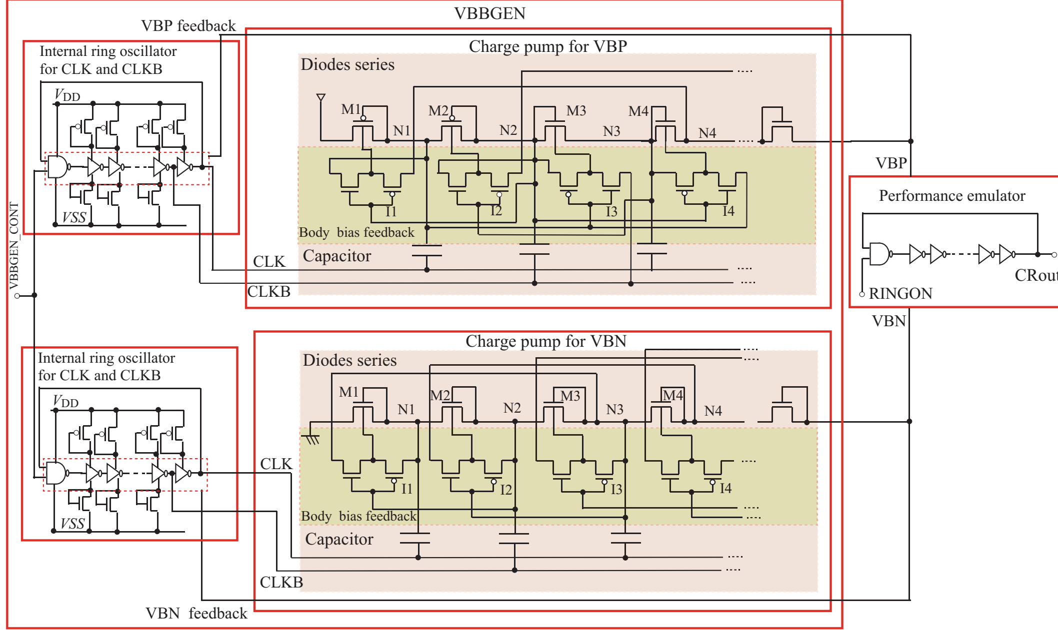


Figure 5.2: Performance emulator and Charge pump architecture

For more accurate performance tracking, a tunable configuration which can alter the logic depth and type [45, 81] can be easily integrated into DABT. Nevertheless, in order to focus on proving the concept of DABT in this thesis, a basic ring-oscillator (a simple inverter-based one) is used. Optimizing the configuration of the performance emulator is out of the scope of this thesis.

5.1.3 Discharge circuit and Phase-frequency detector

Fig. 5.4 shows the details of the adopted discharge circuit and the phase-frequency detector, previously depicted in Fig. 5.1. Here, a conventional phase-frequency detector which is generally used in Phase-Locked Loop (PLL) is adopted. In the detector, the “CRout” signal outputted from the performance emulator is compared with the reference clock, “RefClock”. When the frequency of “RefClock” is higher than that of “CRout”, a “Discharge” signal is sent to the discharge circuit. The discharge circuit consists of simple transistor switches. Since FBB voltages are also treated, the discharge switches are connected to V_{DD} for the VBN switch, and to V_{SS} for the VBP switch. This means that the maximum (minimum) voltage which can be supplied to the well is V_{DD} for VBN (V_{SS} for VBP). The discharge is stopped when DABT is at the standby mode; hence, the maximum RBB of VBBGEN can be supplied. Here, in order to control the body bias voltage, the discharge switch needs to be wide enough. Otherwise, it cannot cancel the current from VBBGEN. As a result, the electrical charges at the well are converged to the maximum RBB which can be outputted by VBBGEN. In the conducted simulation, the discharged current value from the switch needs to be at least two times higher than that of the charged one. Also, when the wells' area is small, too large switches might cause an excessive discharge from the wells. Such

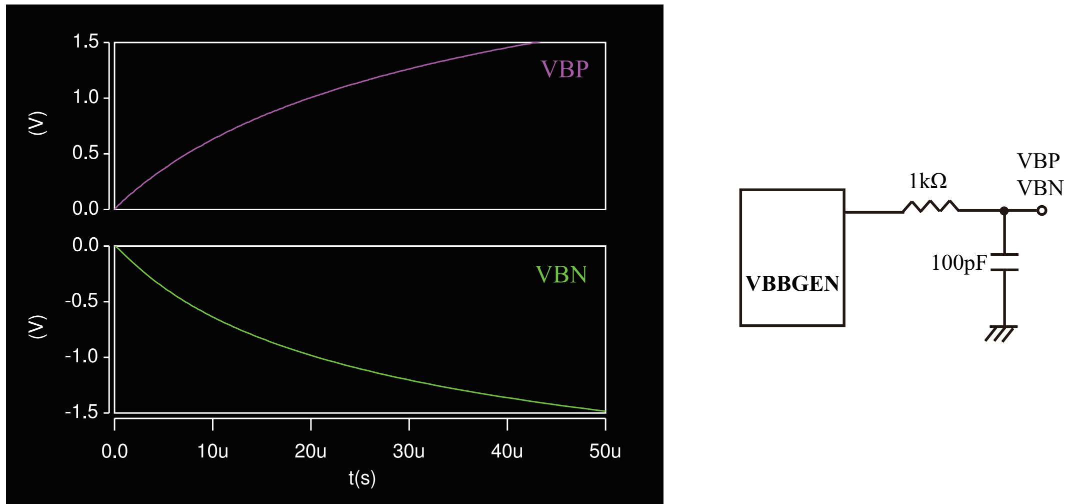


Figure 5.3: Simulated waveform of VBBGEN

discharge causes output voltage oscillations. Therefore, the maximum sizes for VBP and VBN switches depend on the size of the target well.

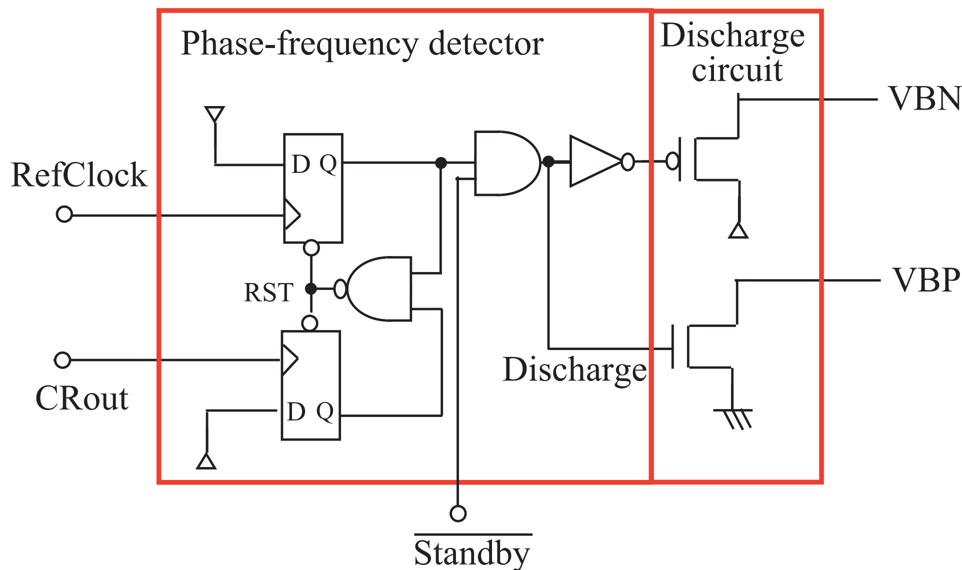


Figure 5.4: Discharge circuit and Phase and frequency detector architecture

Fig. 5.5 explains the behavior of the body bias control of DABT. At the standby mode, “DisCharge” signal is always negated; hence, strong RBB is supplied by the VBBGEN. as depicted in phase 1. When the “Standby” signal is negated, “CRout” and “RefClock” are compared. Since the period of “CRout” is wider than that of “RefClock”, the “DisCharge” signal is asserted and the body biases are controlled, as can be observed in phase 2. When “CRout” and “RefClock” match each other, this means that the performance is tuned to the target one. Therefore, the discharge is stopped (phase 3). Although the delay has converged

to the target one, VBBGEN continues to accumulate the charges of the well. Thus, after a certain interval of time, the period of "CRout" becomes a bit longer than that of "RefClock". Nevertheless, the discharge signal is sent to the switch immediately, and adjusts the delay of 'CRout", as depicted in phase 4.

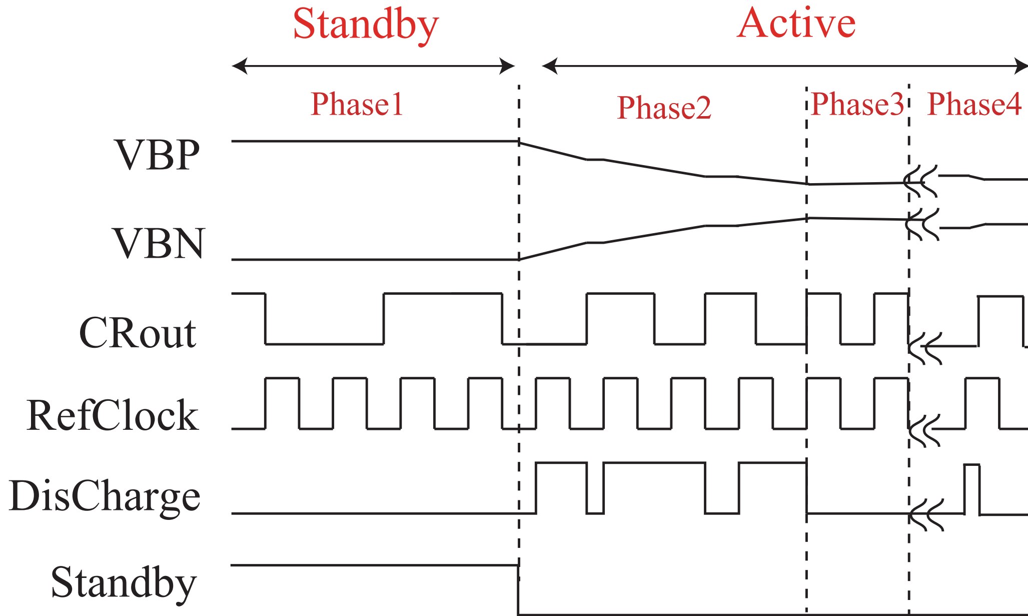


Figure 5.5: Timing diagram of the discharge circuit and phase-frequency detector

5.1.4 Wake-up detector

Fig. 5.6 illustrates the circuit diagram of the wake-up detector. The role of this circuit is to observe whether "CRout" has been correctly tracking "RefClock" or not. First of all, these input signals are sent to the edge detectors [82] which generates a pulse at each transition of the input signal. At every edge of "CRout", *Q1* is set to "1", and it is reset at every edge of "DRefClock"[2]. *Q1* is captured by the second flip-flop *Q2* at every rising edge of "DRefClock", and the third flip-flop *Q3* at every falling edge of "DRefClock". *Q2* is asserted when the transition of "CRout" occurs when "DRefClock" is high. On the other hand, *Q3* is asserted when a transition edge of "CRout" occurs while "DRefClock" is low. When both *Q2* and *Q3* are "1", "TranChk" is asserted. "TranChk" represents the situation where "CRout" transits twice in a single period of "DRefClock". When "TranChk" is always "1", it means that the frequencies of "CRout" and "RefClock" are the same. Therefore, the body bias transition can be detected by observing the number of the cycles where "TranChk" is "1". From this view point, "Counter" starts to count the number of such periods. When the count value reaches a certain threshold value, "W_detect" is asserted. In the present work, this threshold value is set to 3.5. On the other hand, VBBGEN might

[2]Since DABT tunes the body bias so as to match the phase and frequency of "CRout" and "RefClock", the *set* and *reset* of *Q1* might simultaneously occur when "RefClock" is directly used. In order to avoid this situation, "RefClock" is delayed to shift its phase.

cause excessive RBB due to its continuous operation, as shown in Fig. 5.5. Therefore, the "W_detect" signal is negated when TranChk is "0" within a few clock cycles.

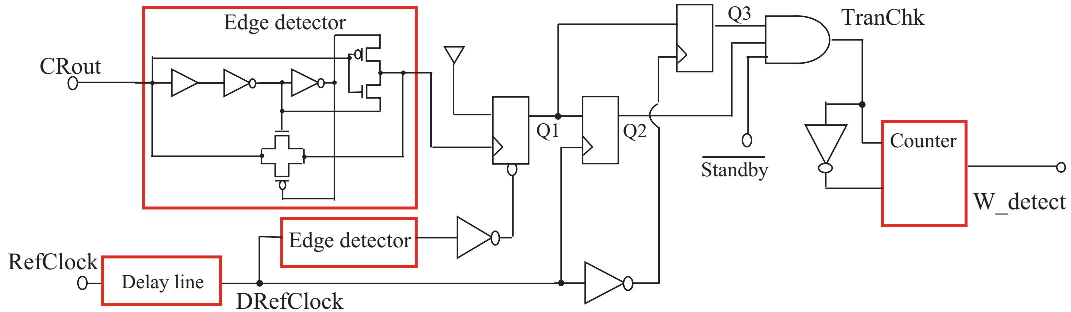


Figure 5.6: Wake-up detector

Fig. 5.7 shows a summarized timing diagram of the wake-up detector. When the period of "CRout" is larger than that of "DRefClock", "CRout" cannot transit twice in a single period of "DRefClock". Therefore, "TranChk" is "0", as illustrated by *A* in Fig. 5.7. On the other hand, when the frequencies of "DRefClock" and "CRout" are the same, "CRout" can transit twice in a single period of "DRefClock". Therefore, "TranChk" becomes "1", as depicted in Fig. 5.7 by *B*, and "W_detect" is asserted after 3.5 cycles (*C*).

Unlike the performance emulator, the wells of the phase-frequency detector and wake-up detector are implemented separately and shorted to the zero bias voltages. Hence, the behavior of the controller is not changed from the output voltage of the body bias.

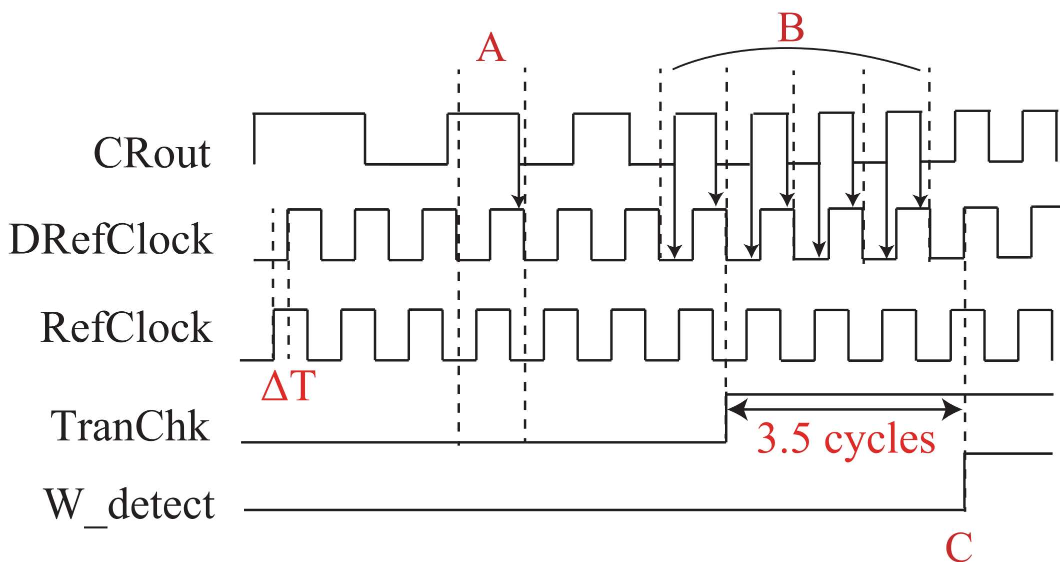


Figure 5.7: Timing diagram of the wakeup detector

5.2 Evaluation

5.2.1 Chip implementation & Measurement setup

Figs. 5.8 and 5.9 show a photo of the fabricated chip and the layout using SOTB 65-nm FD-SOI technology, respectively. The area of VBBGEN, using 2pF of capacitance for each stage, and the bias controller are 31889μm^2 and 4843μm^2, respectively. In addition to the components depicted in the block diagram of DABT (Fig. 5.1), the input and output buffers are also implemented in the actual layout. Since the current DABT is a prototype, it is designed so that any off-chip digital load can be connected to it after fabrication rather than implementing a specific application. Hence, the two performance emulators in Fig. 5.1 are implemented as macros of inverter chains. The number of the inverter stages is decided by referring to a MIPS processor's critical path. For the discharge switches, the low V_{TH} 3.3V MOS transistors provided by the PDK are used because its drain-source voltage there easily overcomes the voltage limitation of the core transistors (1.2V). The area breakdown for the entire DABT system layout is summarized in Table 5.1.

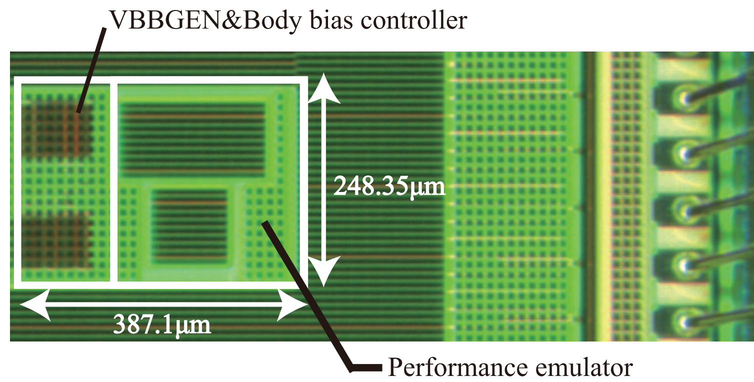


Figure 5.8: Photograph of the implemented real chip

Table 5.1: Area breakdown of the implemented components in DABT

Component	Area[μm^2]	Percentage
VBBGEN	31889	33.17%
Bias controller	4843	5.038%
Performance emulator and remaining parts	59404	61.79%
Total	96136	100%

In this implementation, the digital signals are connected to the I/O cells provided by the PDK library. The I/O cells for digital signals are composed of a level-shifter and an electrostatic-discharge (ESD) circuit. Through the level-shifter, the voltage level of the digital signals are amplified to 3.3V. Therefore, the digital signals communicate outside of the chip with this I/O voltage level. On the other hand, the I/O cells for body bias pins

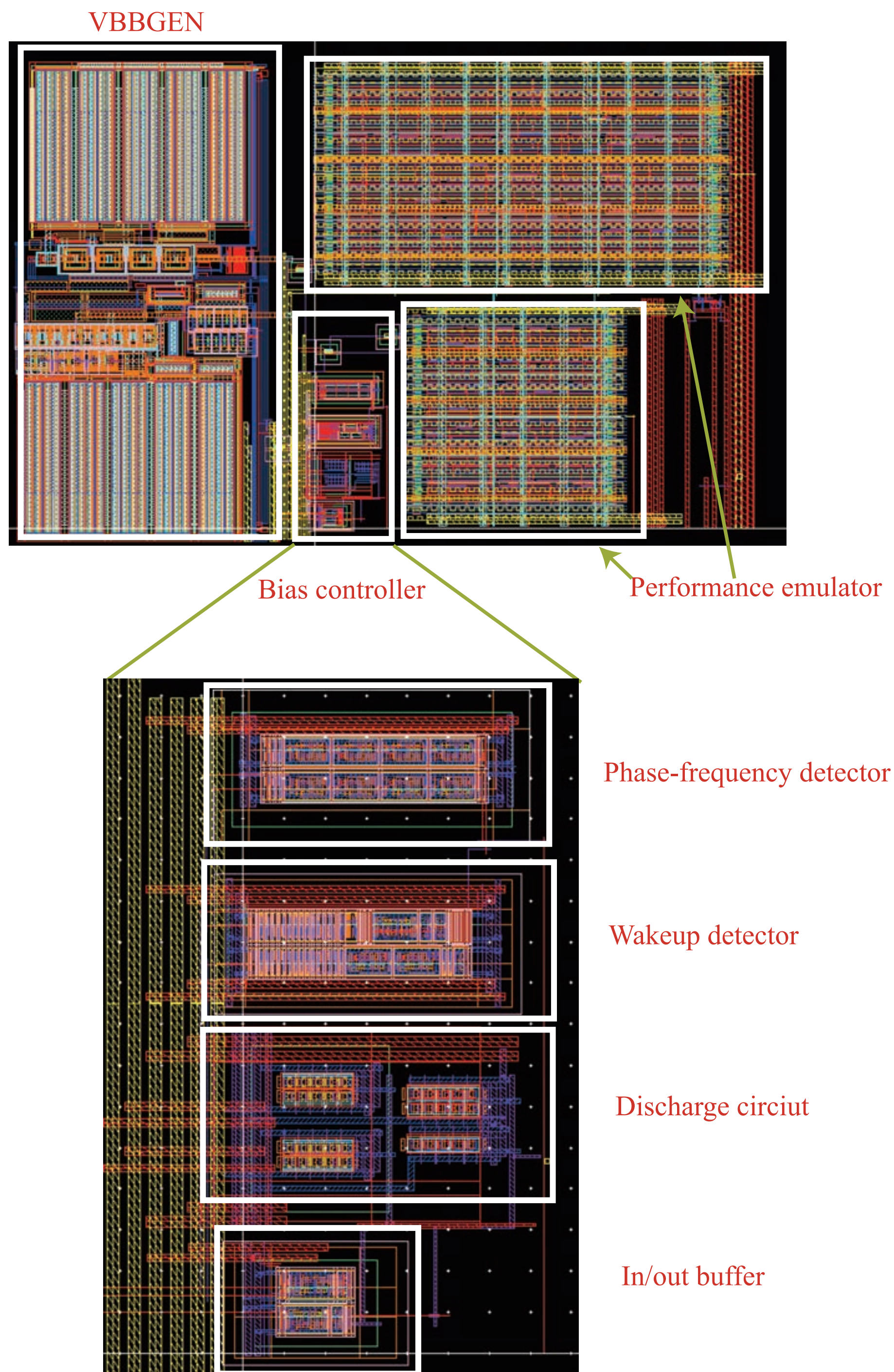


Figure 5.9: Layout of DABT

are different from that of digital signals. In fact, body bias pins do not adopt any ESD components since the well of the chip works as a large diode. That is why the body bias voltage level from DABT can be directly measured.

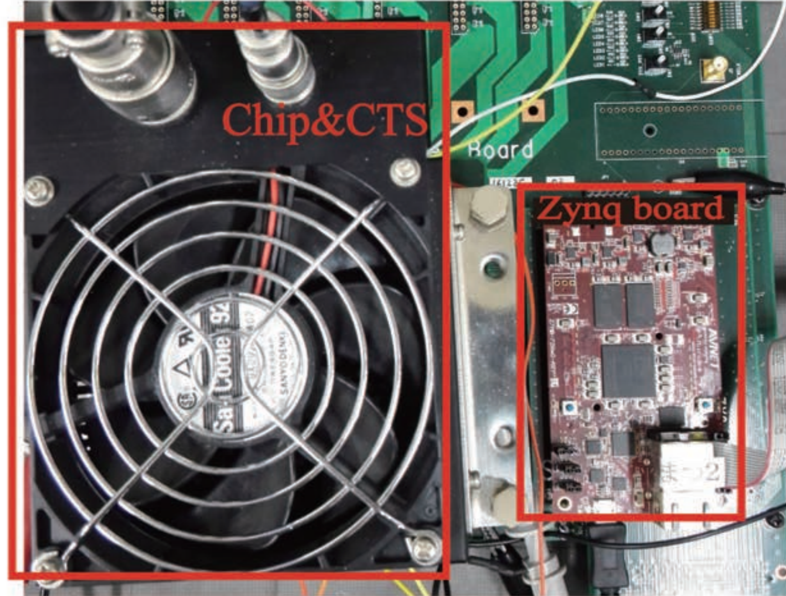


Figure 5.10: Testing board for the real chip measurements

There are parasitic capacitors on the p-n junction between the wells and p-substrate. From the device specification sheet given by the foundry, the leak-out current from a well and the parasitic capacitance are approximately few pA and a few hundred pF when a digital VLSI system (e.g. 1mm^2 of area) is implemented. The leakage current from the nMOS and pMOS devices to the well can be removed by the BOX layer as previously explained. Therefore, we consider the inverse saturation current on the p-n junction diode among the wells and p-substrate here. Consequently, the designed VBBGEN which can drive a few nF of load capacitance under a few nA leak-out current is sufficient to drive this load. The measured output impedance of the VBN and VBP charge pumps at $V_{DD} = 0.5\text{V}$ were $16.5\text{M}\Omega$ and $16.6\text{M}\Omega$, respectively. Also, according to the conducted SPICE simulations, the drain-source resistances of the discharge switch for VBP are from $19\text{k}\Omega$ to $51.5\text{k}\Omega$ between a range of 0.2V of FBB and 2.5V of RBB in our design. On the other hand, the resistance of the VBN switch is from $100\text{k}\Omega$ to $135\text{k}\Omega$ for the same body bias voltage range.

In SOTB technology, the maximum n-well and minimum p-well voltages are defined by the breakdown voltages of the BOX layer and p-n junction between p-well and n-well. The p-n junction and BOX breakdown voltages are set to 10V and 5V, respectively. However, from the view point of a long-term reliability, voltages lower than 5V on the BOX are recommended. That is why, 2.5V of maximum RBB is chosen similarly to [16] (i.e. p-well voltage=-2.5V, n-well voltage = V_{DD}+2.5V).

In order to test the implemented chip, an evaluation board is used. It is composed of a chip socket and an Avnet Microzed board based on Zynq-7000, as shown in Fig. 5.10. The

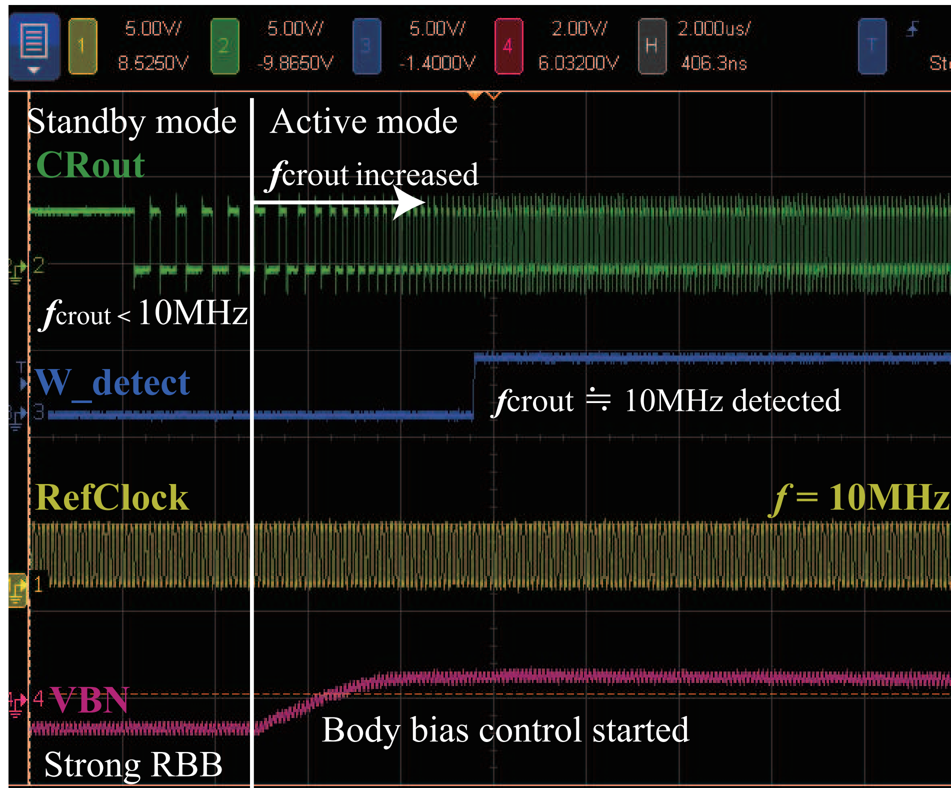


Figure 5.11: Oscilloscope waveforms snapshots depicting the behavior of the proposed system

Zynq board inputs the digital signals required by DABT. In addition to the input from the Zynq board, "RefClock" was provided via an external function generator which can freely control the frequency up to 75MHz. The output signals from DABT were monitored by an oscilloscope.

For chip heating during the high temperature testing, CTS-01A Compact Thermal System developed by ATE service corporation was used. The chip was warmed via a socket, and the chip temperature was measured by a thermal monitor using a thermocouple element [83]. The highest chip temperature used in this experiment was 70°C, which is defined as the highest value for commercial usage [13].

5.2.2 Chip measurement results

Fig. 5.11 depicts the waveform snapshots obtained from the test-chip illustrating the behavior of the proposed system when controlling the body bias voltage from the standby mode to the active mode. "CRout", "W_detect", "RefClock" and "VBN" are shown in this waveform. The frequency of "RefClock" which is inputted by the external function generator is set to 10MHz, and the power supply voltage for the entire DABT system is 0.5V. As can be seen in these waveforms, the behavior described in the previous section is obtained in the real chip. Before starting to control the body bias voltage, the oscillation frequency

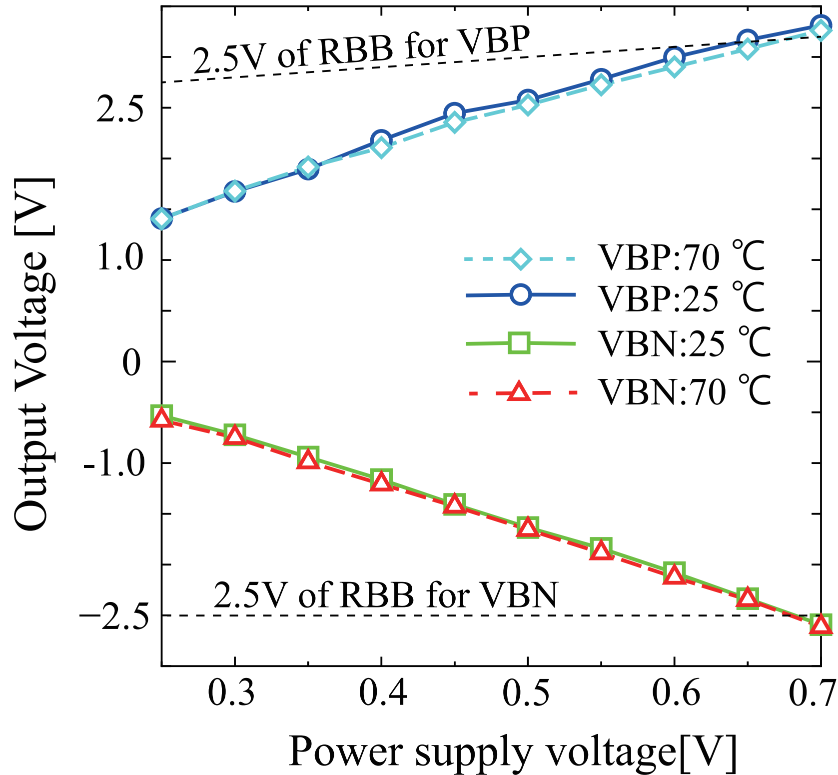


Figure 5.12: VBBGEN output voltage without body bias control

of “CRout” is clearly slower than that of “RefClock” due to the applied RBB. However, since DABT controls the body bias voltages according to the “CRout” frequency, the body bias voltage rises towards the FBB direction until “CRout” can oscillate around the target frequency. Hence, the frequency of “CRout” is gradually increased. When the oscillation signal reaches the target frequency, the body bias voltage becomes steady. Around 10MHz of “CRout” frequency, the employed Wake-up detector properly asserts the “W_detect” signal, as it can be seen in Fig. 5.11.

Standby mode

In order to treat DABT at the near-threshold region, it should be checked whether VBBGEN can operate at a low-voltage condition or not. Fig.5.12 shows the obtained output voltage of VBBGEN at room (25°C) and high temperatures (70°C). Indeed, even at lower voltages than 0.5V, VBBGEN is able to output RBB voltages accordingly. At 0.35V of supply voltage, VBBGEN can output 1.895V for VBP and -0.9411V for VBN at room temperature. Moreover, the output voltages did not degrade by the chip heating, as shown in the graph. In fact, at 0.35V of the supply voltage and a temperature of 70°C, 1.917V of VBP and -0.9887V of VBN are obtained. In this case, the difference between both temperatures were only 1.124% and 5.058% for VBP and VBN, respectively. Such results validate the fact that VBBGEN can actually operate as a voltage supplier for DABT at low-voltage

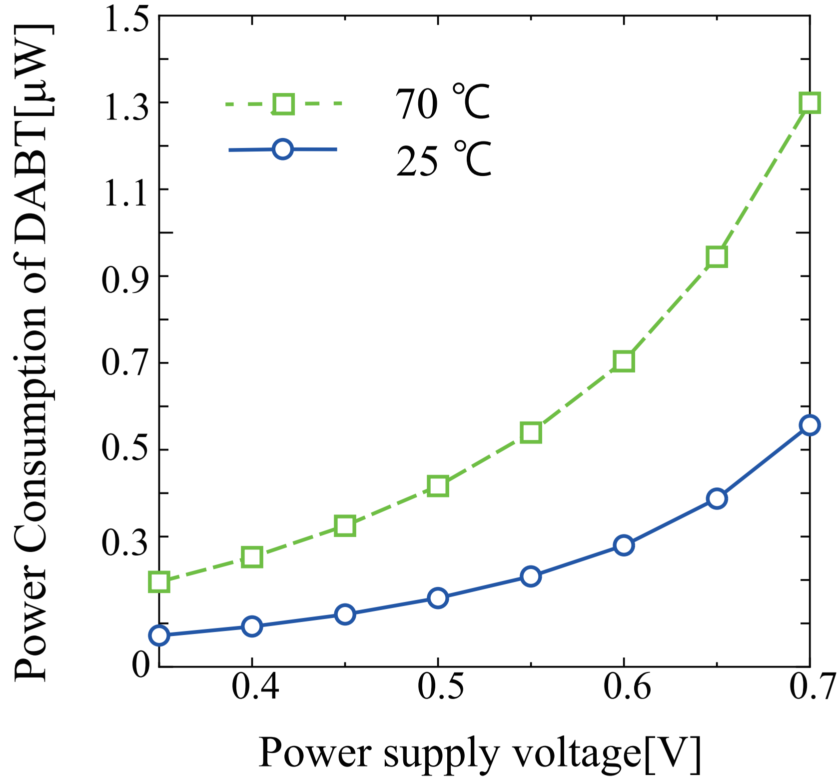


Figure 5.13: Measured power consumption for the standby mode

and high-temperature conditions. On the other hand, this graph implies that the maximum power supply voltage of DABT conforms with the norms defined in [16], where the maximum RBB in SOTB technology is 2.5V. In fact, as represented in Fig. 5.12, the output voltage of VBBGEN reaches this maximum RBB voltage at 0.65V of supply voltage.

Compared to just using a charge-pump circuit, DABT incorporates some controller components for performance tuning. When the performance tuning is not required, the corresponding parts can be stopped. Nevertheless, these components might cause a power overhead from the baseline charge-pump. Fig. 5.13 shows the power overhead of DABT in the standby mode. In almost all conditions, it consumes only a few hundred nano watts of power. For instance, at 0.5V of power supply voltage, the entire power overheads of DABT are 158.5nW and 416.5nW at room and high temperatures, respectively. Compared to other types of charge-pumps which can only generate RBB voltages in the standby mode, these overheads can be considered as quite reasonable. In fact, [79] consumes 350nA of current consumption, while DABT consumes 317nA at 0.5V of power supply and room temperature.

Voltage Transition

It is important to verify that DABT can control the voltage of a real system in a way that does not hinder the performance. In particular, the transition time is important as it may

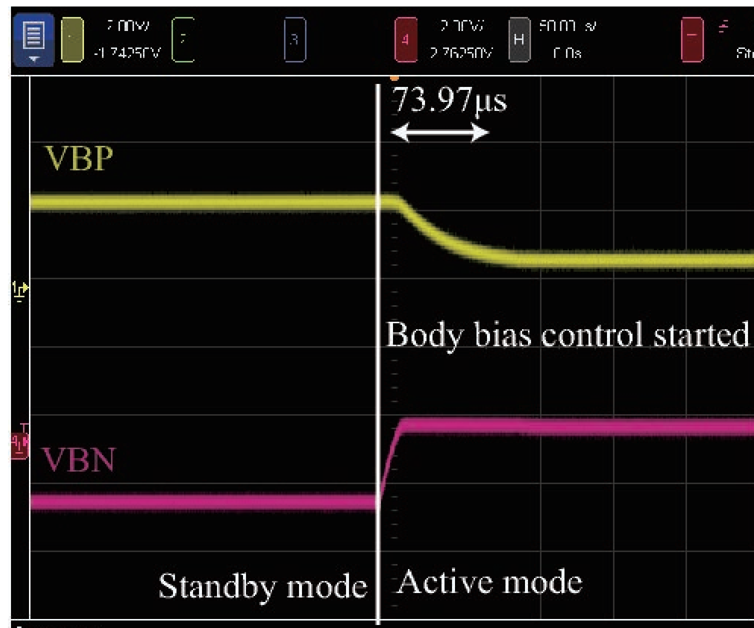
have a significant impact on the system performance. Here, we focus on the body bias transition time from the standby mode to the active mode. To measure this transition time, DABT was connected to a real chip *Dynamically Reconfigurable Processor* [69] which is also implemented in 65-nm SOTB technology and has 2.568mm^2 of circuit area. The measured waveforms are shown in Fig. 5.14. As an example, when 0.5V of V_{DD} and 40MHz of "RefClock" are considered, DABT is able finish the voltage transition within 737.5μs (Fig. 5.14 (a)). It worth mentioning that this transition time is proportional to the area of well. If smaller area wells are controlled, the transition time becomes faster. Indeed, when DABT was connected to a circuit of 0.1mm^2 area, the transition time was 73.97μs (Fig. 5.14 (b)). Since the transition time is also related to the voltage amplitude, the slew rate of body bias transition is calculated. The obtained values at 2.56mm^2 and 0.1mm^2 of load are 2.31mV/μs and 22.5mV/μs, respectively. These values are summarized in Table 5.2.

Active mode

Next, the characteristics of the body bias controllability and power overhead at the active mode are analyzed. Fig. 5.15 (a) shows the DABT body bias output voltages at 0.5V of V_{DD}. It can be seen from these graphs that DABT can control the body bias voltage without the need for DACs. The output voltage is changed according to the "RefClock" frequency. For example, at 2MHz of "RefClock", 2.057V of VBP and -1.0363V of VBN are obtained. Then, they are changed to 1.435V and 0.0469V at 14MHz. Here, on the condition that further lower voltage operations are required, DABT can operate at such voltage conditions. Fig. 5.16 (a) illustrates the body bias output voltages at 0.35V of V_{DD}. Note that, since the body bias voltage is controlled by the delay information of the performance emulator, the range of the input frequency is lower when compared to that of 0.5V. Nevertheless, the body bias voltages can be controlled with the input frequency even at 0.35V of V_{DD}.

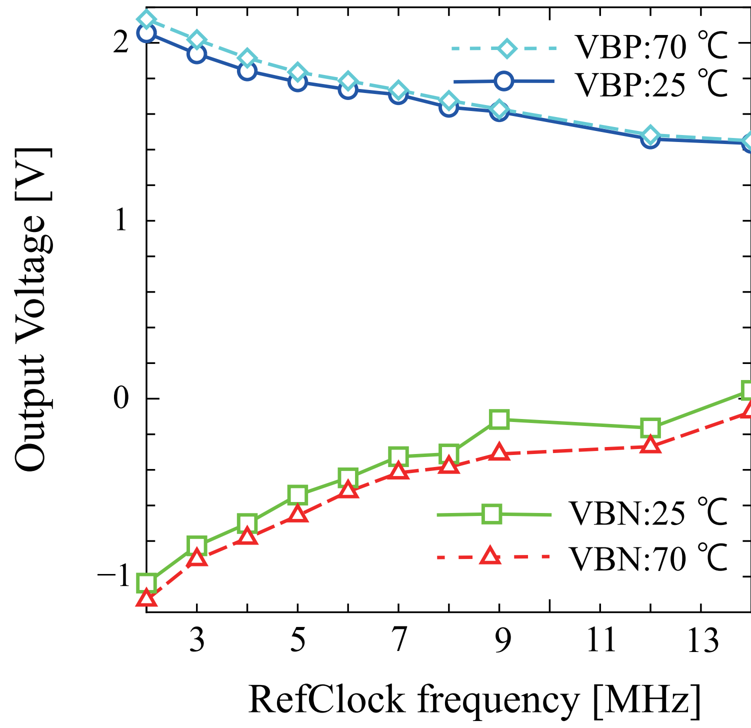
The proposed system is composed of digital circuits; thus, its power overhead highly depends on the frequency of "RefClock". Figs. 5.15 (b) and 5.16 (b) show the power overhead at 0.5V and 0.35V of V_{DD}, respectively. As a matter of fact, although the overhead is 944nW at 2MHz of "RefClock", it later increases to 6.560μW at 14MHz, as depicted in Fig.5.15 (b). Moreover, the power overhead naturally increases at a high temperature (8.317μW at 14MHz). Nevertheless, it is still in the order of micro watts. When observing the case at low V_{DD}, the power overhead is decreased from that of the 0.5V case since both of the input frequency and power supply are also lowered. For instance, it is only 0.1068μW at 0.1MHz of "RefClock". This tendency can also be observed by the breakdown of the power consumption. Figs. 5.17 (a) and (b) show the power consumption breakdown at room temperature when V_{DD} is set to 0.5V and 0.35V, respectively. The biggest portion of the power is different when the supplied V_{DD} is changed. In fact, at V_{DD}=0.5V and $f_{RefClock}$=14MHz, the largest power portion is consumed by the bias controller, and it is 54% of the total power, as represented in Fig. 5.17 (a). VBBGEN and the performance emulator consume 19% and 27% of the total power at this condition, respectively. On the other hand, at V_{DD}=0.35V and $f_{RefClock}$=0.7MHz, VBBGEN dissipates the largest power which is 50% of the total power, as illustrated in Fig. 5.17 (b). The power consumption of the digital parts is relatively lowered at this condition.

(a)

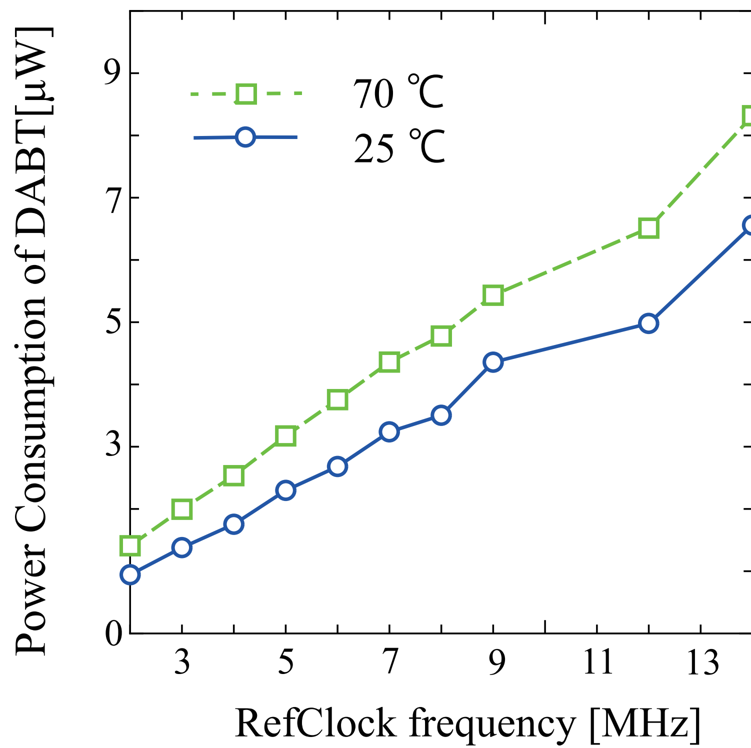


(b)

Figure 5.14: Measured waveform for the voltage transition from the standby mode to active mode: (a) 2.56mm^2 of load (b) 0.1mm^2

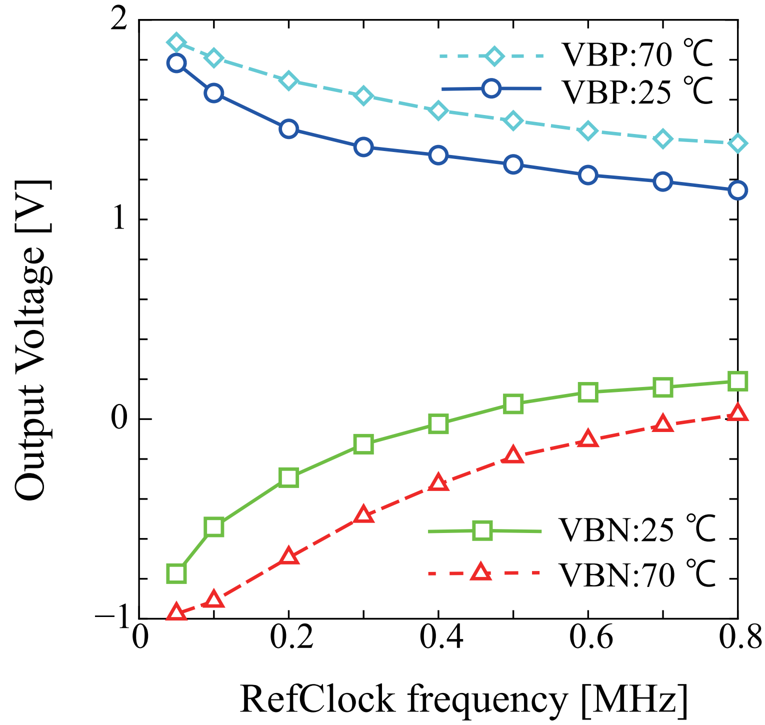


(a)

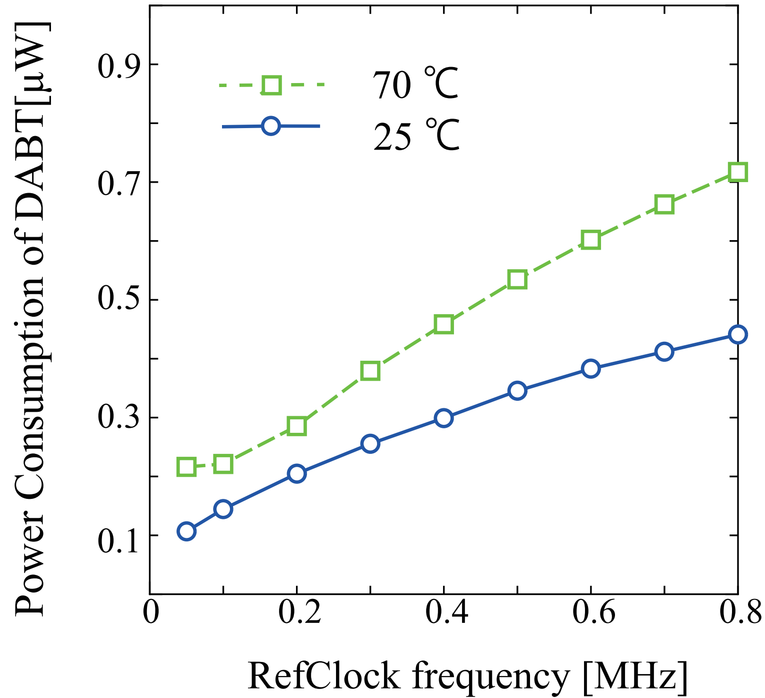


(b)

Figure 5.15: Measured characteristics of the active mode at 0.5V of V_{DD}: (a) Output voltage (b) Power consumption

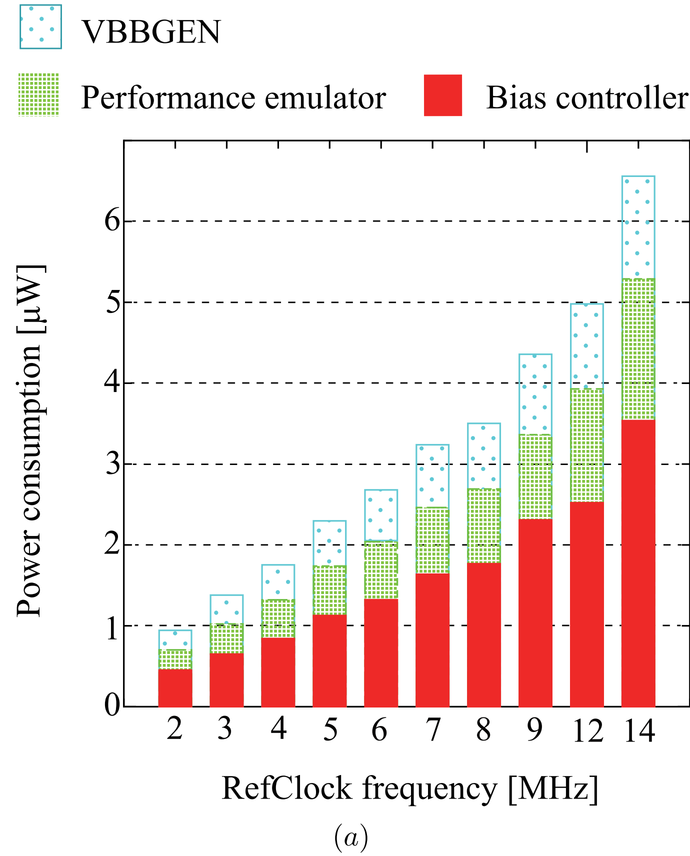


(a)

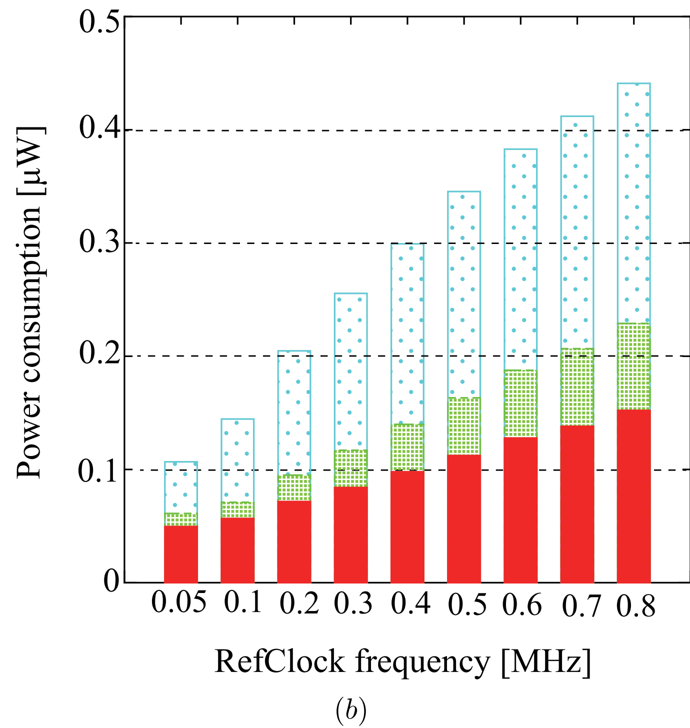


(b)

Figure 5.16: Measured characteristics of the active mode at 0.35V of V_{DD}: (a) Output voltage (b) Power consumption



(a)



(b)

Figure 5.17: The power breakdown of DABT at room temperature: (a)$V_{DD} = 0.5$V (b)$V_{DD} = 0.35$V

Comparing the output voltages at room and high temperatures, which can be seen in Fig. 5.15 (a) and Fig. 5.16 (a), the latter is more towards the RBB direction than the former. This is because, at low power supply voltage conditions, Inversed Temperature Dependency (ITD) occurs [81, 84]. At a high temperature, ITD effects decrease the gate delay. Thus, the obtained bias voltages are more in the RBB direction. In addition, lower power supply voltages increase the occurrence frequency of the ITD effect. Nevertheless, as shown in Fig. 5.16 (a), DABT properly reflects this effect. In other words, DABT can efficiently track the effects of ITD.

DABT performance tracking ability

Since DABT controls the body bias voltages using the delay of the performance emulator, the range of the available frequencies depends on the target system. As an example, the frequency ratio ($f_{CRout}/f_{RefClock}$) of DABT was measured. Here, f_{CRout} is obtained from the average of the different measured values. The obtained results are shown in Fig. 5.18. In this figure, when the ratio is equal to 1, the frequency of the performance emulator is tuned to the frequency of "RefClock". If the ratio is less than 1, it means that the frequency of the performance emulator does not reach the target frequency and higher frequencies than such a point cannot be used. While if the ratio is higher than 1, it means that the f_{CRout} cannot be slowed down to the target frequency due to the limitation of the used maximum RBB voltage. As can be seen in this graph, when a high V_{DD} voltage is used, the available voltage range is stretched. In fact, at 0.5V of V_{DD}, the frequency of "CRout" can correctly track the "RefClock" frequency from 0.5MHz to 73MHz. Here, 73MHz was the highest frequency which could be obtained in this experiment. On the other hand, at 0.35V of V_{DD}, the range is approximately from 70KHz to 0.7MHz. Since DABT controls the body bias by repeatedly charging and discharging the wells, the controlled frequency of the performance emulator has a certain frequency deviation. However, the frequency deviation can be small by carefully choosing the size of the discharge transistors and charge pumps. Fig. 5.19 shows the measured deviations from the target delay at V_{DD}=0.5V and room temperature. As shown in this graph, the variations are in the range of $\pm$ a few ns from the target value. Therefore, when we consider low frequencies (e.g. lower than 100MHz) this deviation can be manageable. However, it is difficult to apply DABT to a high-performance system where the ns deviation cannot be acceptable.

Comparison to other body bias controllers

The characteristics of DABT and their comparison with other fabricated body bias controllers are summarized in Table 5.2. It is important to mention that, although the scheme proposed by *Mauricio et al.* [58] is one of the most similar systems to DABT, their evaluation is based on pre-layout simulations. Therefore, the evaluation results of such a system are not included in Table 5.2 for a fair comparison.

As shown in Table 5.2, DABT achieves the lowest power consumption among the other body bias controllers. This is because, DABT adopts digital circuits for the bias controller, which allows the power supply voltage down to a near threshold region like 0.5V. Also, thanks to its low voltage requirement, a power supply voltage for other digital circuits (i.e.

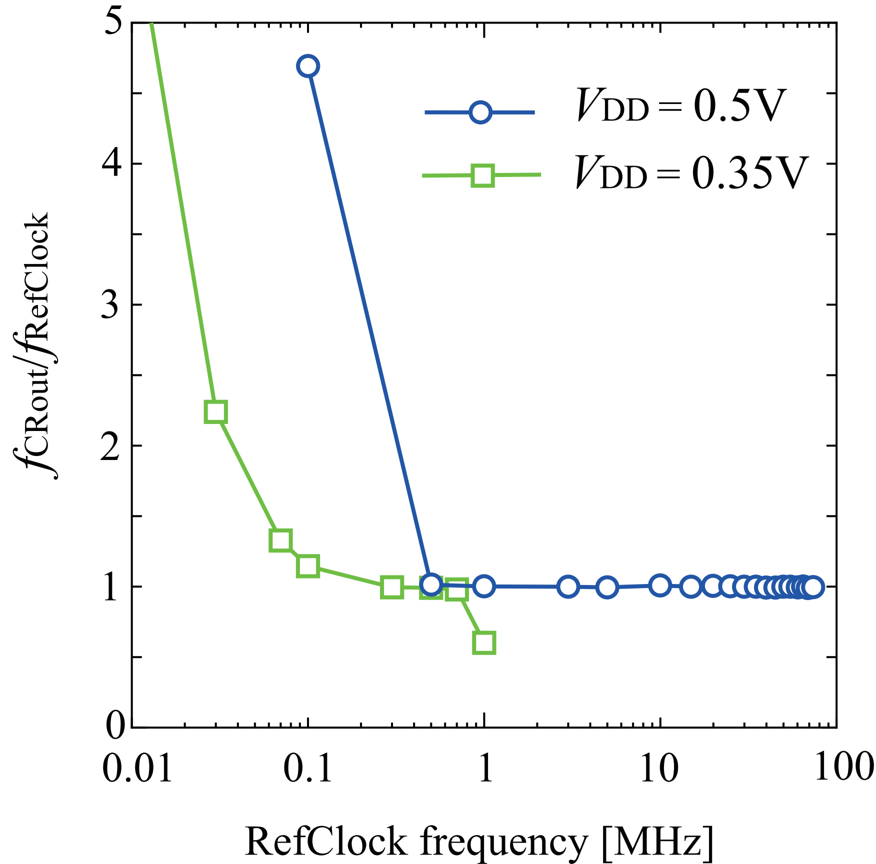


Figure 5.18: Available input frequency range of DABT

target systems) can be shared with DABT. In other words, DABT does not require another power source like [57]. Hence, DABT can simultaneously achieve a low power overhead with no additional power source, while the others cannot.

Since DABT is based on digital circuits, its power consumption depends on the operational frequency. Therefore, for higher operational frequencies, the power consumption of DABT might exceed that of [55]. Nevertheless, for low power and low operational frequencies, the power overhead can be significantly lower than that of [55]. Also, even if the power overhead of DABT can be slightly higher than [55], its design has the advantage that an additional power source is not required. In the case where the system needs to operate at a much higher performance and an additional power source can be provided, the power overhead of a DAC-based system can be lower than that of DABT. Furthermore, the maximum power supply voltage for DABT is 0.65V, as previously shown, which is more appropriate for lower frequencies. From this view point, we can say that DABT is suitable for low-power chips rather than high performance systems.

The body bias controller reported in [71] is also one of the similar works to the proposed DABT. It achieved 2.5μW of the power overhead when the power supply for digital circuits is set to 0.375V. Nevertheless, its circuit configuration requires 1.8V of an additional power

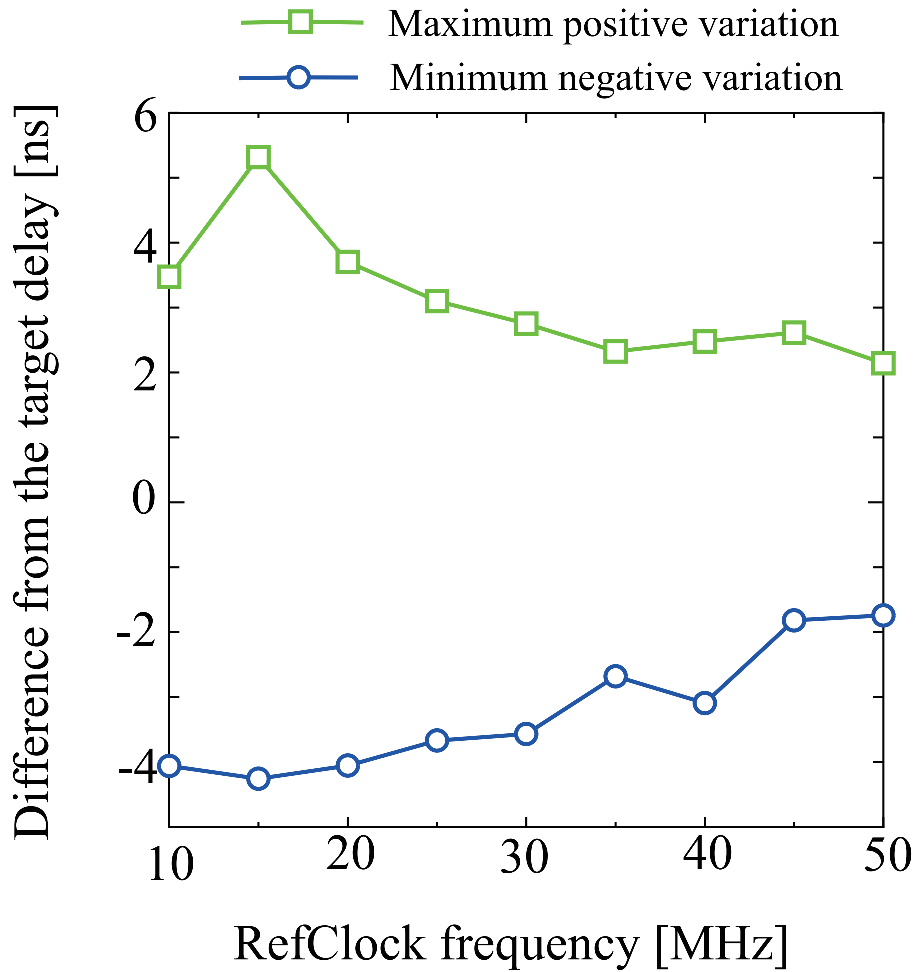


Figure 5.19: Measured frequency deviation of DABT

supply voltage for the charge pump and a part of the controller circuits. Although the bias controller is mainly based on digital circuits, its advantage is not fully exploited.

Table 5.2: Summary and comparison with the other fabricated body bias control systems:
∗The summarized slew rate values are for the body bias transition from the standby mode to the active mode.
†The power consumption is obtained at 0.35V of V_{DD} and 0.1MHz of f.
‡The power consumption is obtained at 0.5V of V_{DD} and 14MHz of f.

Parameter	Proposed DABT	Quelen [71]	Wang [59]	Blagojević [55]	Kamae2014 [57]	Kamae2014 [70]	Miyazaki [54]
Process	65-nm FD-SOI	28-nm FD-SOI	40-nm Bulk	28-nm FD-SOI	65-nm Bulk	65-nm Bulk	0.2μm Bulk
Delay tracking	Yes	Yes	No	Yes	No	No	Yes
Supply voltage	0.35V-0.65V	0.35-1V, 1.8V	1.2V, 2V	1.0V, 1.8V	0.5V-1.2V	0.6V-1.2V	
Another power source	Not required	Required	Required	Required	Not required	Not required	Required
Output	RBB/FBB	RBB/FBB	RBB/FBB	RBB/FBB	RBB/FBB	FBB	RBB/FBB
Circuit area	0.096mm^2	0.0067mm^2	0.1mm^2	0.012mm^2	0.0052mm^2	0.0023mm^2	0.128mm^2
Slew rate* (V_{DD}, load area)	22.5mV/μs (0.5V, 0.1mm^2) 2.31mV/μs (0.5V, 2.56mm^2)		19.2mV/μs (1.2V, 1mm^2)	80mV/ns (1.8V, 1mm^2)	-	50mV/μs (0.6V, 0.1mm^2)	-
BBG power consumption	0.1068μW† - 6.560μW‡	2.5μW	23μW	10μW	600μW	120μW	4000μA (Current)

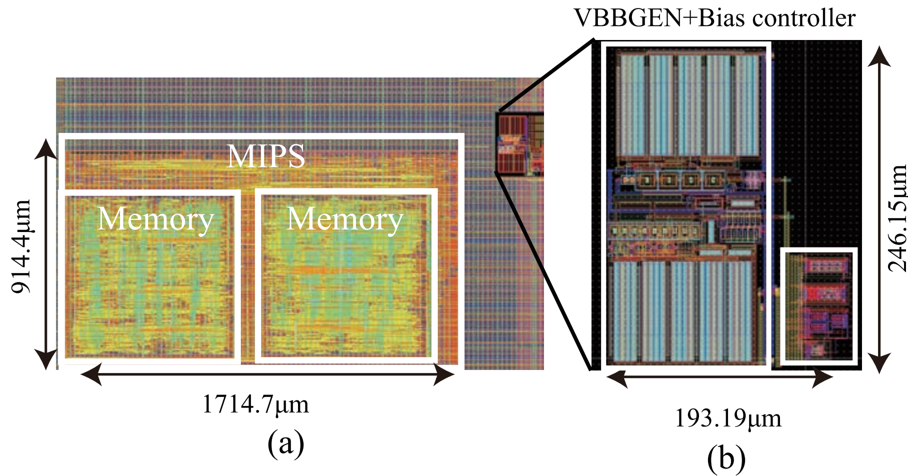


Figure 5.20: Used layout for the simulations: (a) Entire system (b) Bias controller

5.2.3 DABT impact on a processor system

In order to show the DABT efficiency in terms of leakage reduction, HSPICE simulations are carried out where DABT is applied to a processor system. As a case study, a MIPS subset processor is implemented with SOTB 65-nm technology for this discussion. The processor uses MIPS R3000 instruction subset (e.g. ADD, SUB, and some logic calculations), 5-stage standard pipeline and 2KB of Instruction/Data local memory. The used layout for the simulation is depicted in Fig. 5.20. Note that, since the performance emulator is embedded to the MIPS layout, the circuit area for DABT is smaller than that shown in Fig. 5.8. The area overhead at this case is only 3.03% when compared to the implemented MIPS.

For evaluating the delays of the MIPS and the performance emulator, their components are extracted from the netlist, and parasitic RCs are attached to the extracted components. From the obtained simulation results with 0.6V of supply voltage, zero bias and the typical corner, the maximum operating frequencies of the MIPS at 25°C and 70°C are 117.3MHz and 121.2MHz, respectively. When the required frequency is lower than these values, the zero bias state results in excessive body bias voltages.

For the performance emulator, a simple ring oscillator is used as shown in Fig. 5.2. In this implementation, the number of inverters in the emulator can be selected from 15 to 175 in 10-inverters increments. Fig. 5.21 illustrates the delay difference between the performance emulator (105-stage of inverters) and the critical path of MIPS at 0.6V of V_{DD} and room temperature. The number of inverter stages is decided so that the tuned critical path delay by DABT does not violate the timing requirements. At zero bias condition, the difference is 2.22% and it increases to 8.30% at 1.0V of RBB. Although more accurate performance emulators can be selected, the used ring-oscillator is sufficient to observe DABT's efficiency.

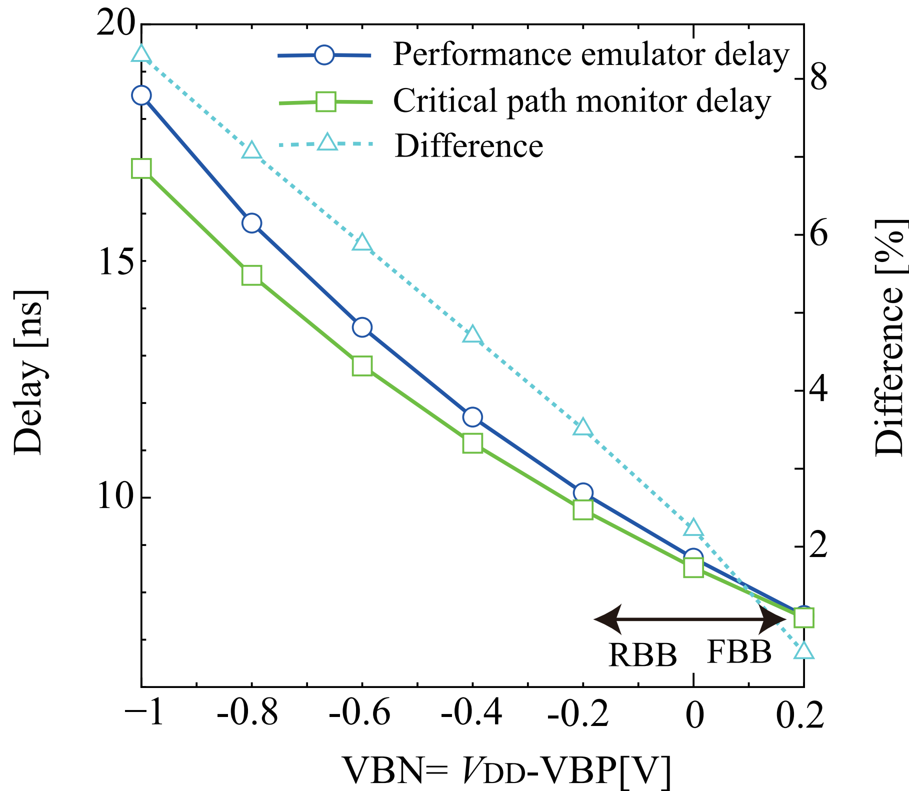


Figure 5.21: Difference of the delay between the performance emulator and MIPS.

Leakage reduction

The leakage simulation is conducted with the netlist extracted from the layout shown in Fig. 5.20. Due to the huge simulation time, the RC extraction for the part of the body bias controller is omitted in this simulation. By using the netlist and the output signal from the performance emulator, we can obtain the body bias voltages at which the critical path delay can be tracked to meet the reference clock period. Then, it is possible to calculate the leakage current consumption of the MIPS. However, this MIPS has numerous flip-flops which might make the simulation unstable at initialization. Hence, the leakage value at zero bias condition is firstly obtained by IC-Compiler, and the MIPS leakage is then scaled by a ratio calculated by the difference of leakage current between zero bias and the obtained body bias with an inverter cell.

Fig. 5.22 shows the simulation results in terms of DABT capability of leakage reduction. The vertical axis is the leakage power of the adopted MIPS which includes the power overhead of DABT. Here, the power supply voltage is set to 0.6V. Since some of the simulated operational frequencies result in excessive body bias voltages at zero bias, DABT can efficiently reduce the leakage current, as illustrated in Fig. 5.22. In fact, 41.82% of power reduction can be obtained at 100MHz of "RefClock" and 25°C. The obtained VBN and VBP voltages at this condition are -0.1307V and 0.8510V, respectively. Moreover, since DABT allows a wide range of input frequencies, it is easy to make it coexist with a

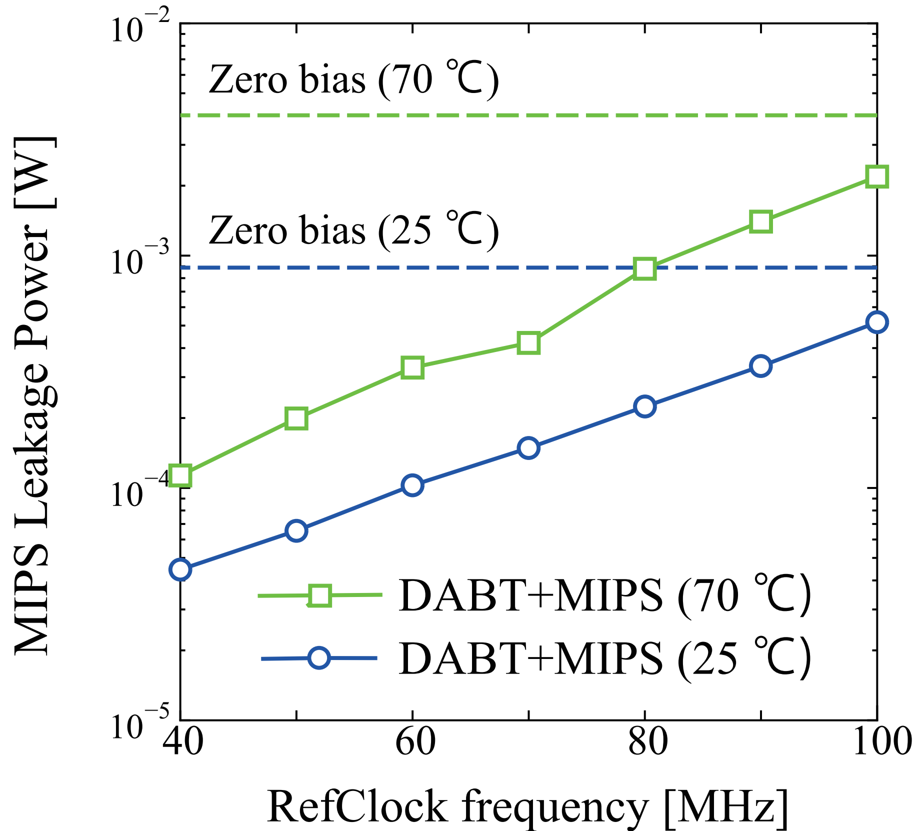


Figure 5.22: Leakage reduction for MIPS processor.

Dynamic Frequency Scaling (DFS). According to this figure, 94.99% of power reduction can be obtained at 40MHz and 25°C. Here, the VBP and VBN voltage are 2.024V and -1.249V, respectively. It is worth mentioning that further stronger RBBs can be supplied for lower "RefClock" frequencies to a certain limit. This limit highly depends on the VBB-GEN output voltages. In fact, VBBGEN can output RBB voltages up to VBP=2.999V and VBN=-2.079V at $V_{DD} = 0.6$V, as shown in Fig. 5.12.

As proved in Fig. 5.15, DABT can properly operate even at high temperatures. Therefore, the leakage reduction can still be achieved at high temperatures. Considering the case of 100MHz, 45.56% of leakage current is reduced with 0.7549V of VBP and -0.2151V of VBN. Also, at 40MHz, 97.18% of leakage reduction is achieved with -1.216V of VBN and 1.864V of VBP.

Process variation

From the results shown above, DABT is immune to voltage and temperature variations. However, digital circuits also suffer from process variations, as previously mentioned. Therefore, the proposed DABT is simulated under different process variation conditions. When the simulation is conducted, the process variation can be categorized as within-die (WID) and Die-to-Die (D2D) variations. For a digital system, like an embedded processor which

Table 5.3: Hspice simulation results of the proposed body bias control at 100MHz of reference frequency. $*$ Since DABT is used for improving the performance at SS corner, the leakage reduction is not applied at this corner.

	Zero bias delay	Adjusted delay	Leakage reduction
FF, 25°C	6.868ns	9.516ns	80.06%
FF, 70°C	6.774ns	9.476ns	78.39%
SS, 25°C	1.014ns (violate)	9.762ns	$*$

has relatively long logic depth, the D2D variation has more significant effects than the WID [56, 85]. For this reason, we only focus on the D2D variation in this simulation. As explained in chapter 2, the corners of the SOTB device model are specified with "F", "T", or "S". FF and SS corner were utilized as case conditions to evaluate the process variation.

The simulated results are listed in Table 5.3. The second and third column represent the critical path delay at the zero bias and after the DABT adjustment states, respectively. The fourth column represents the leakage reduction of DABT from that of the zero bias condition. If a 100MHz operation is required for the MIPS, the zero bias condition at the FF corner is clearly excessive and causes large leakage current. On the other hand, the same condition at SS corner cannot achieve the required 100MHz frequency. Nevertheless, since DABT tunes the body bias voltages based on the system delay information, it is useful for adjusting process variations. For instance, at the FF corner, DABT supplies RBB and achieves 80% of leakage current reduction. At the SS corner, DABT can adjust the delay so as to meet the timing constraints. As a result, the MIPS can properly operate at 100MHz of operational frequency.

5.3 Conclusion of this chapter

In this chapter, a Digitally Assisted automatic Body bias Tuning scheme (DABT) is proposed for near-threshold computing. DABT can generate the adequate body bias voltages capable of achieving a required system speed while reducing the power consumption as much as possible. That is, according to the system clock frequency, it automatically adjusts the bias voltages to meet the timing requirements. On the other hand, when a target system does not have to operate (i.e., standby state), DABT can efficiently supply a strong reverse bias voltage to reduce the leakage current. DABT does not require additional analog power sources, unlike conventional and already proposed body bias control schemes, and can operate at the near-threshold region. Consequently, it can lower the power overhead for body bias control and reduce the system cost caused by additional power sources. According to the evaluations of the fabricated chip with 65-nm SOTB technology, DABT could properly function and deliver the expected benefits, even at 0.35V of supply voltage. Also, the characteristics of DABT at a high temperature condition were measured. These measurements prove that DABT could correctly output the body bias voltage reflecting the ITD effect. In other words, DABT allows a system's delay to be tuned to a target speed, even under the ITD effect.

In order to observe the efficiency of DABT, a MIPS processor is adopted as a case study. At 0.6V of power supply voltage, DABT could achieve up to 80% of leakage reduction while meeting the 100MHz of operational frequency timing requirements. In addition, the evaluation shows that DABT is also useful to compensate the slow corner variations.

6

Conclusion and Future Work

6.1 Conclusion

In this thesis, two power-efficient body bias control methodologies are proposed and evaluated. First, in order to utilize asymmetric body bias conditions, a power optimization is proposed. That is, the proposed optimization can distinguish the body bias for nMOSFET and pMOSFET while the conventional approaches cannot. This approach can improve the BBC control granularity on the condition that discrete body bias voltage sets are given. Second, an ultra-low-power overhead body bias controller DABT is proposed. The proposed DABT adopts the digitally assisted analog circuit technique; thus, it can operate at a near threshold voltage region. DABT was fabricated with the SOTB65-nm FD-SOI technology. Real chip measurements revealed that DABT can achieve the lowest power overhead compared to the other body bias scheme already proposed, to the best of the author's knowledge.

Regarding its characteristics, each of the proposed approaches should be carefully applied to improve the body bias efficiency. For example, since DABT controls the body bias with a frequency, unlike the conventional DAC-based body bias generator, its power overhead is increased when higher power supplies and operational frequencies are used, as explained in the previous chapter. If a delay tracking mechanism is attached to the DACs (e.g. critical path monitors, delay comparators, etc.) like [54], the similar power overhead to DABT is incurred. From these viewpoints, the frequency based body bias control is suitable for low performance applications (several MHz of f). On the other hand, the asymmetric BBC intrinsically assumes a Look Up Table (LUT) based body bias control if it is implemented with an on-chip optimizer. In such cases, once appropriate voltages are obtained, a system performance monitoring scheme does not have to always operate. So, its power overhead can be independent from the target frequencies. Therefore, on the condition that target system frequencies are relatively high, LUT + DAC based designs can have an advantage in terms of the power overhead. These discussions are summarized in Fig. 6.1.

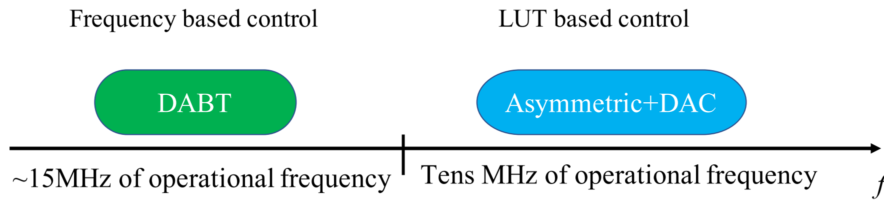


Figure 6.1: Appropriate situations to apply the proposed methods

6.2 Future Work

Despite the good results of the proposed approaches, there is still room for improvement. For example, the current DABT architecture does not assure any body bias balance between nMOS and pMOS. In other words, the current DABT might cause non-optimal body bias balance. Indeed, regarding the real chip measurement results of DABT (Fig.5.15), BBA=VBP+VBN-V_{DD} is equal to 0.5207V at room temperature, and 2MHz of "Ref-Clock". This balance is not always optimal for a target system. Therefore, an additional circuit to control the body bias balance is required. Moreover, although the DABT characteristics are validated with a real chip, the impact of leakage reduction is simulated with HSPICE in this thesis. This is because the current DABT is a prototype and it is designed so that any off-chip digital loads can be connected to DABT after fabrication. Therefore, realizing the co-operation between DABT and a target system with a real chip is still one of the future works. Similarly, the on-chip error adjustment scheme in chapter 4 (Fig. 4.10) is validated with simulations. Therefore, it should also be fabricated with a real chip, and its efficiency should be validated with real chip measurements.

Also, when we discuss the proposed power optimization, the V_{DD} and body bias voltages are considered as discrete values due to limitations from practical voltage generators. However, these voltages can be quasi-continuous values by adopting "voltage dithering". That is, when discrete voltages V1 and V2 are given, intermediate voltages between V1 and V2 can be virtually realized by dithering them [86]. This dithering technique also pursues finer voltage control granularity like the proposed asymmetric BBC. However, when voltage transitions are required, they clearly incur an energy overhead. On the other hand, the asymmetric body bias conditions can improve the voltage control granularity without this energy overhead. Therefore combining the asymmetric BBC and voltage dithering technique might provide a good trade-off between the control granularity and energy overhead. Exploring this trade-off can be an interesting direction and it is one of the future works of this thesis.

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Publications

The works described in this thesis are based on several publications listed below:

Journal Papers

- Hayate Okuhara, Akram Ben Ahmed, Hideharu Amano, Digitally Assisted On-chip Body Bias Tuning Scheme for Ultra Low-power VLSI Systems, IEEE Transactions on Circuits and Systems I: Regular Papers, Vol.xx, No.xx, pp.xx–xx, 2018. (accepted for publication)
- Hayate Okuhara, Akram Ben Ahmed, Johannes Maximilian Kühn, Hideharu Amano, Asymmetric Body Bias Control with Low Power FD-SOI Technologies: Modeling and Power Optimization, IEEE Transactions on Very Large Scale Integration Systems, Vol. 26, No. 7, pp.1254-1267, July 2018.
- Hayate Okuhara, Yu Fujita, Kimiyoshi Usami, Hideharu Amano, Power Optimization Methodology for Ultra Low Power Microcontroller with Silicon on Thin BOX MOSFET, IEEE Transactions on Very Large Scale Integration Systems, Vol. 25, No. 4, pp. 1578-1582, April 2017.

International Conference Papers

- Hayate Okuhara, Akram Ben Ahmed, Hideharu Amano, An Ultra Low-power Automatic Body Bias Tuning Scheme Using SOTB technology, *Proc. of the 2018 IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips 21),*, Poster session, Poster No.11, April 2018.
- Hayate Okuhara, Akram Ben Ahmed, Johannes Maximilian Kühn, Hideharu Amano, Leveraging Asymmetric Body Bias Control for Low Power LSI Design, *Proc. of the 2017 IEEE Symposium on Low-Power and High-Speed Chips (COOL Chips 20),*, pp.1-3, April 2017.
- Hayate Okuhara, Kuniaki Kitamori, Yu Fujita, Kimiyoshi Usami, Hideharu Amano, An Optimal Power Supply And Body Bias Voltage for a Ultra Low Power Micro-Controller with Silicon on Thin BOX MOSFET, *Proc. of the 2015 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pp.207-212, July 2015.

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- Hayate Okuhara, Akram Ben Ahmed, Hideharu Amano, Real chip evaluations of a body bias tuning scheme for ultra-low power processors, *Proc. of the 80th National Convention of IPSJ*, pp.1:15-1:16, March 2018. (In Japanese)
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- Hayate Okuhara, Akram Ben Ahmed, Hideharu Amano, Development and evaluation of on-chip body bias tuning scheme, *IEICE Technical Reports CPSY2016-54*, pp. 35-40, November 2016. (In Japanese)
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- Hayate Okuhara, Yu Fujita, Hideharu Amano, Power optimization methodology based on simple power models for a low power micro controller, *Proc. of the 78th National Convention of IPSJ*, pp.1:185-1:186, March 2016. (In Japanese)
- Hayate Okuhara, Yu Fujita, Kuniaki Kitamori, Kimiyoshi Usami, Hideharu Amano, Power optimization based on a simple power model for a micro-controller, *IEICE Technical Reports CPSY2015-101*, Vol.115, No.374, pp.93–98, December 2015.(In Japanese)