A Thesis for the Degree of Ph.D. in Engineering

Theoretical studies on device structure and material design for high performance graphene nanoribbon devices and interconnects towards future LSI applications

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Chapter 1: Introduction

1.1 Overview of LSI technology

High integration of LSI technology has led to miniaturization or down scaling of the electronic components has given a big impact on the semiconductor technology in this past 40 years. This down scaling trend is very feasible since we are able to achieve not only device with higher performance, but also lower production cost as larger number of transistors can be occupied per chip. This long trend which started since 1970 is called 'Moore's Law', where the number of transistors per chip is estimated to double every year by scaling down the size of transistors [1,2]. However, this trend of downscaling is reaching its limit in both transistors [3,4,5] and interconnects technologies [6]. In conventional silicon devices, as the gate-length becomes too short, problems such as short-channel effects [7, 8, 9] occur. The main problem is that short channel contributes to off-leakage current due to the tunneling behavior of the electrons.

To date, we have a 14 nm node technology by Intel where the physical gate length is actually speculated to be shorter than 14 nm. In regards with the 'technology nodes', it is expected that there will be only another three generations of them after the current 14 nm generation. Expected to be in 2020, when the gate-length is down to 5 nm, marks the limit of CMOS technology where there will be too huge off-leakage current in the entire chip [3].

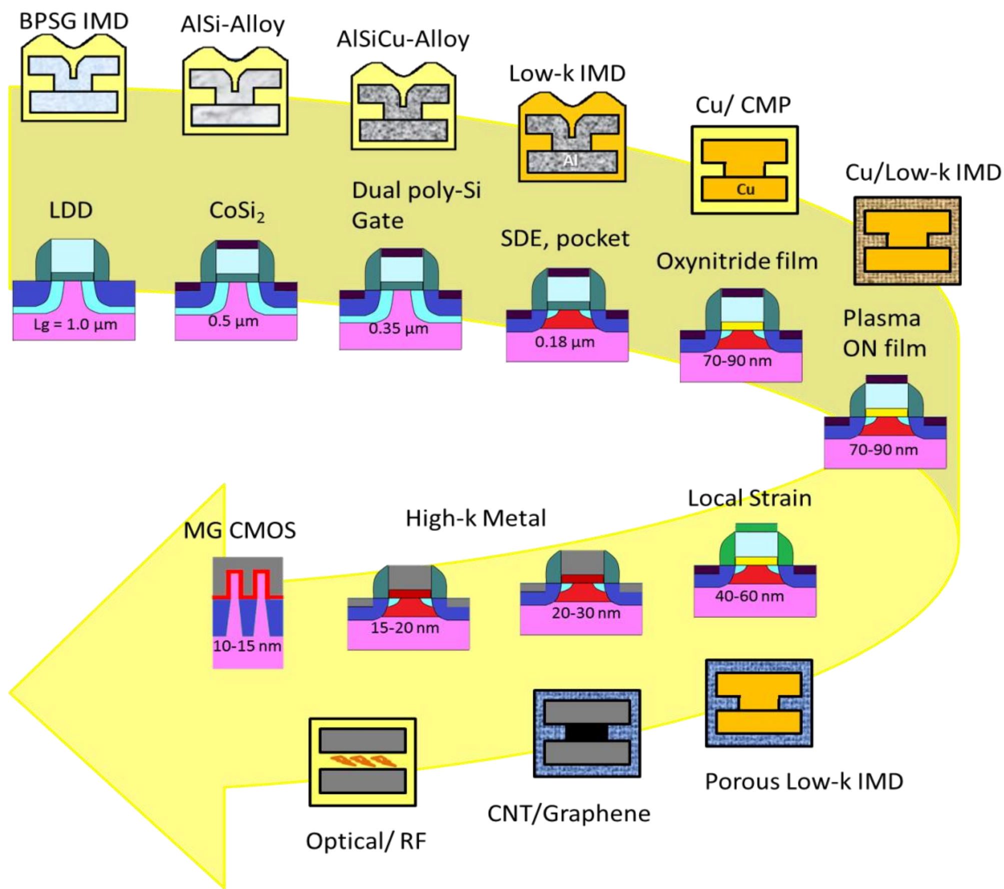


Fig. 1: Scaling down and performance enhancement in LSI technology

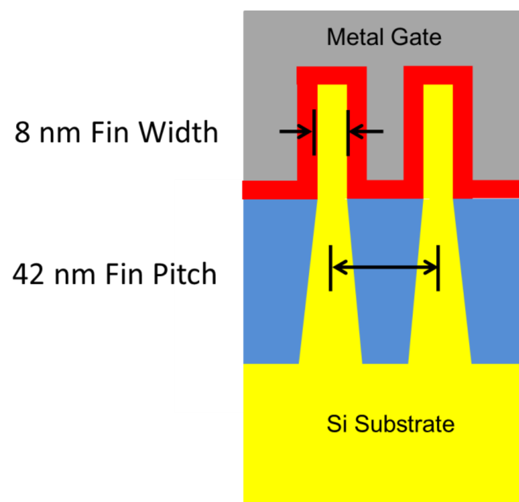


Fig. 2: 14 nm technology node of a Fin-Field Effect Transistor developed by Intel [10]

On the other hand, together with the down scaling of the silicon transistor, conventional copper interconnects is also reaching its limit [6, 7] because of the high integration in LSI technology. By the year 2020, it is predicted that the interconnect wire width will be as narrow as 22 nm while current density reaching 5.8×10^6 A/cm^2 [11]. The current-carrying capability of conventional copper interconnect cannot achieve such high current density due to limiting factors such as carrier scattering at material interface/grain boundaries, thermal induced failure and electromigration [12,13]. Moreover, aggressive scaling of copper interconnects will further increase energy loss through heat dissipation which is governed by higher resistance in narrower interconnects [14]. Although past predictions are not always correct, with the way the trend is continuing right now, we expect the both conventional transistor and interconnect technology will struggle to stay alive in another 10-20 years.

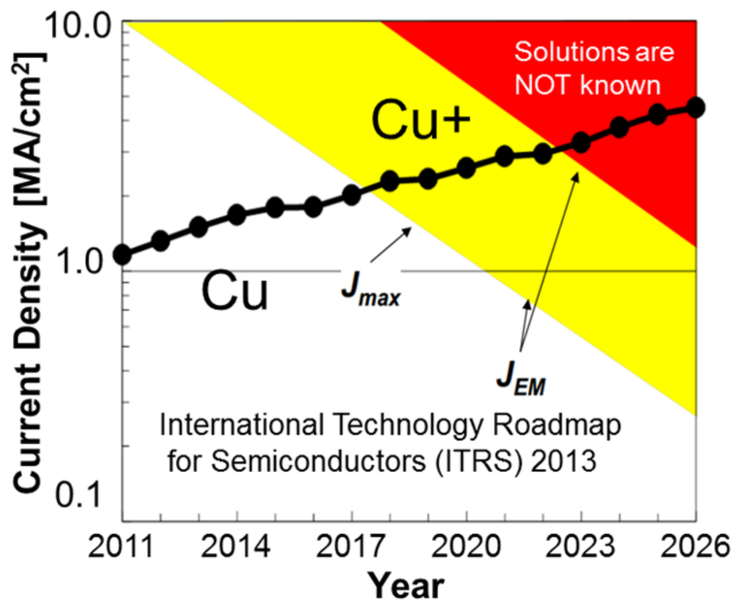


Fig. 3: ITRS roadmap for the current density of Copper (Cu) [15] Reprinted and modified with permission from ITRS 2013 Edition, Interconnect, Figure INTC9

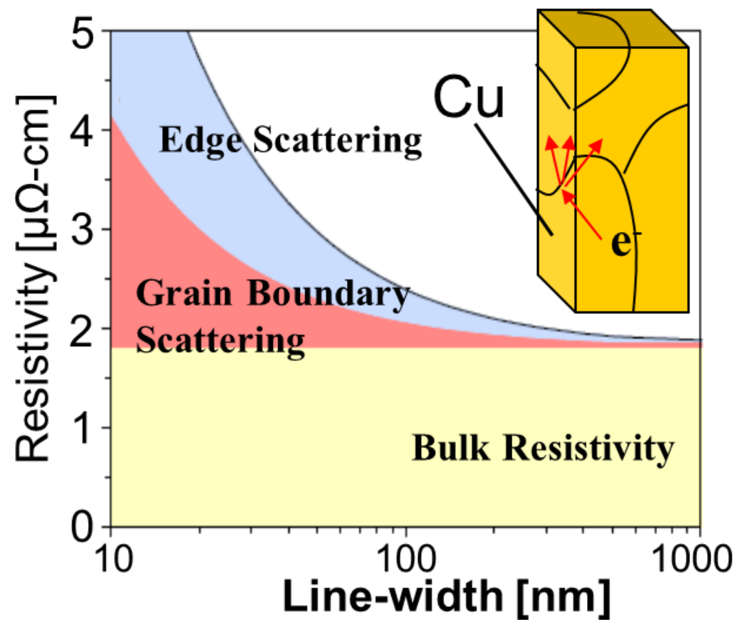


Fig. 4: Increasing resistivity of Cu interconnect with width of <100nm [16]

A solution to this struggle is the adoption of new device structure such as the double gate (DG) [17] or fin-FET [18] type MOSFETs. These devices are excellent in suppressing the off-leakage current. Another application is Si-nanowire [19] MOSFETs which show higher on-current conduction than conventional DG FETs and the fact that they can be adopt for high-density integration is yet really attractive. Despite of these new technologies, the ultimate question is what will come next after reaching the final limit of downsizing? In order to answer this question, some suggest that a new prominent material is needed to replace the conventional silicon channel and copper interconnects technology. Amazingly a single material has the potential to solve these two crucial technologies and is very promising for the future of higher performance electron devices. These new materials are considered as an 'Emerging Material' by the ITRS. In order to keep the Moore's law trend going the advancement in current LSI technology can be generally divided into two major parts. First is the trend of device miniaturization that we discuss earlier, which is called 'More Moore'. The second part is something referred to as 'more than Moore' where intensive works is being carried on to achieve something that exceeds the current trend. 'More Moore' defined by the International Roadmap of Semiconductors (ITRS) indicates something we refer as

‘Beyond CMOS’ This includes researches on new materials, which are commonly addressed as Emerging Research Materials (ERMs) as an alternative channel material for extending CMOS.

These ERMs includes graphene [20], carbon nanotube (CNT) [21] and semiconductor nanowires [22, 23] which are excitingly able to enhance the performance of MOSFETs while possibly reducing the power consumption because of their properties. Higher carrier mobility in III-V, Ge, graphene, carbon nanotube for example can provide higher on currents, I_{on} and lower gate capacitance at constant I_{on}. However issues need to be addressed before such materials can be integrated in the current CMOS technology.

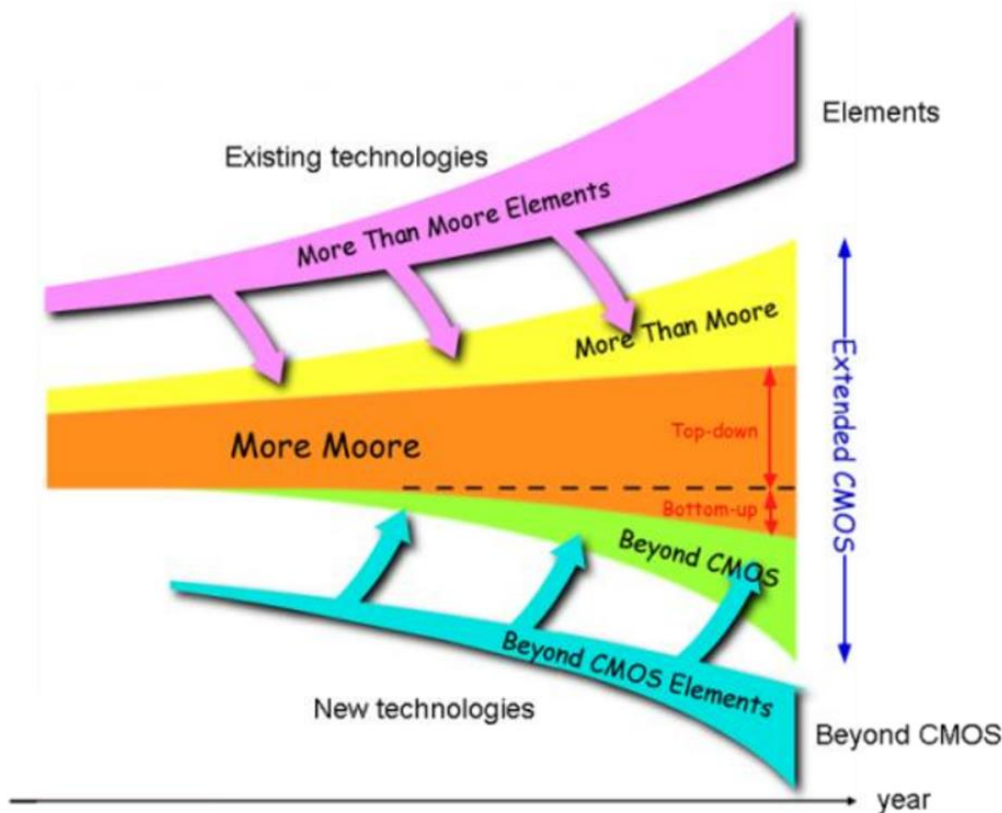


Fig. 5: ITRS roadmap of technological advancement and development [24]. Reprinted with permission from ITRS 2013 Edition, Emerging Research Device, Figure ERD1

1.2 Significance of graphene and its challenges

One of the most promising materials to solve both the issues that we have in transistors and interconnects is graphene. Although graphene has just recently discovered in 2004 and its evaluation is still at early stage, its extraordinary characteristics attract many research works and its discovery was awarded the Noble prize. Graphene is a nanocarbon material where atoms of carbon are being bonded together forming a sheet of honeycomb lattice structure as shown in Fig. 6. It is like an unzipped version of a CNT. 3D-stacking of graphene layers formed the well-known graphite. Although it is considered that 100 layers of a 2D sheet material such as graphene stacked together can be considered as a thin film to a 3D material such as graphite, it has been found that graphene is reaching the 3D limits of graphite at 10 layers [25]. Carbon atoms inside graphene are being bonded to each other by a sp2 bonding, leaving unbounded π-orbitals. These π-electrons can act as high mobility carriers which contribute to amazing properties inside graphene. Among these amazing properties is massless Dirac fermions in graphene which yields a carrier mobility of up to 200 000 cm^2/Vs and a carrier velocity of up to $\sim 10^6$ m/s [26], linear E-k dispersion and ballistic transport. This extraordinary high mobility is 100~1000 times higher than that of silicon in conventional transistor. Owing to these exceptional properties, graphene shows potential for both transistor and interconnect application. Moreover, graphene ambipolar characteristic and its similar p and n carrier velocity make it possible for graphene to serve as both p-channel and n-channel material. Graphene also has a high aspect ratio which makes it immune to short channel effect which is one of the main problems in conventional silicon LSI applications. Despite having these amazing properties, Graphene is however a zero bandgap semiconductor. Thus, this is a very significant issue that is commonly addressed by researchers to be solved before graphene can be used for extended CMOS applications. Nevertheless, ways of creating a bandgap are being previously reported [27, 28, 29].

When graphene was first discovered in 2004, graphene was exfoliated or peeled off from graphite using a scotch tape. This method of producing graphene is called exfoliation method and researchers all over the world initially use this method to produce high quality graphene flakes. The graphene flakes produced defer in specimen

size since it is impossible to control the size of graphene peeled using this exfoliation method. Since the size of graphene cannot be controlled, although high quality graphene can be produced this way, such method is not suitable for mass production in graphene and surely cannot be adopted inside the current LSI fabrication process. Graphene can also be synthesized on Silicon Carbide (SiC) with annealing process where temperature and SiC surface control can produce high quality graphene as well as being able to control the number of graphene layer produce. The major drawbacks of this process is still however not compatible with conventional LSI fabrication process since the annealing temperature is very high (1000 ˚C). Another way to produce graphene is by Chemical Vapor Deposition (CVD) where graphene is grown on Cu films. Graphene with large grain size and high in quality can be grown using this method. However, similar to graphene synthesis on SiC, although graphene can also be grown at low temperature which is compatible with LSI fabrication process (logic application, 400-450 ˚C, flash memory, 650 ˚C), high CVD temperature is needed in order to produce high quality graphene.

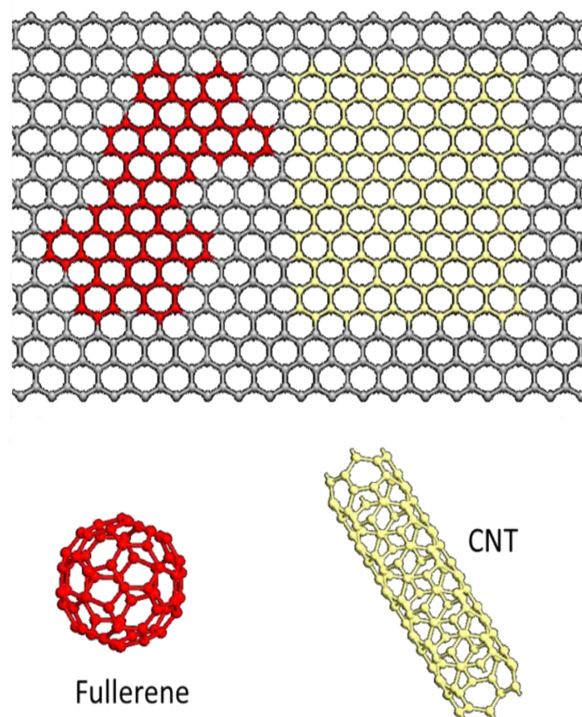


Fig. 6: Graphene structure as a unit that can formed fullerene and CNT. This is modified from[25]

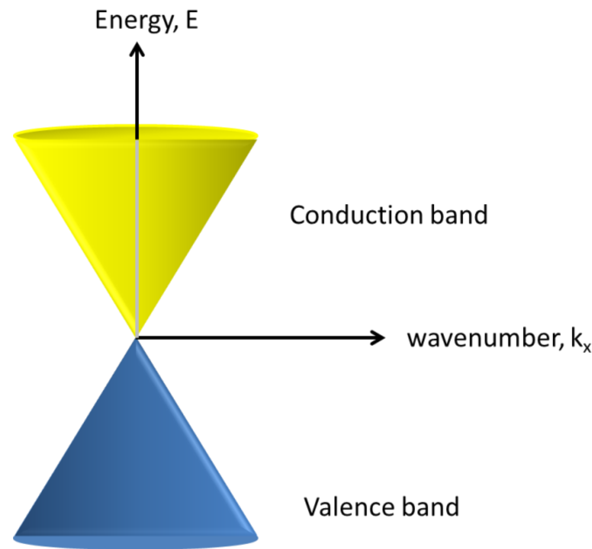


Fig. 7: E-k dispersion of graphene showing zero bandgap

Despite the setbacks in graphene production, developments on graphene electron devices have been very intensive. For example, graphene FETs (GFET) with promising high cut-off frequency have been previously reported. In 2010, Y. M. Lin from IBM group and L. Liao *et al.* both respectively reported a graphene FET (GFET) with a cut-off frequency of 100 GHz [30] and 300 GHz [31]. This value is comparable to of a GaAs high electron mobility transistor with similar gate length. K. Kim *et al.* also reported a GFET with a cutoff frequency of 80 GHz on the same year. Although the GFET report by K. Kim had a lower cutoff frequency and larger gate length, CVD graphene was used for the fabrication process [32]. In 2012, another breakthrough was reported by Y. M. Lin group with a GFET of 350 GHz [33]. L. Leio group however reported the best GFET on the same year with a cutoff frequency of 457 GHz [34]. With this, advancement in GFET fabrication is catching up with the development of high speed III-V semiconductor at a very fast pace. Despite this kind of achievement, the future of graphene electronics is yet still challenging. In most of the reports, where graphene devices were fabricated on a standard silicon wafer with a silicon dioxide insulator layer, the electrical properties of the graphene channel deteriorated showing lower performance in terms of the carrier mobility comparing to their theoretical values. There are suggestions that these findings were caused by parasitic factors such as the

surface scattering of SiO_2 [35] or by damage of graphene flakes during fabrication process. To solve this issue alternate substrates are used replacing silicon substrate such as Boron Nitride (BN) substrate which possesses an identical lattice structure with graphene. In this case the carrier mobility was reported to be enhanced [36]. The feasibility of this BN substrate or layer to be integrated with CMOS technology is however still being evaluated and BN substrate itself is rather costly.

As stated briefly earlier, graphene lacks a very essential property for switching device application; a bandgap. Graphene exhibits a linear E-k dispersion with no bandgap. Nevertheless, ways such as by producing a thin graphene stripe called graphene nanoribbon (GNR) or by applying a perpendicular electric field to a bilayer graphene channel were reported to be able to create a bandgap. Although Bilayer GFET with perpendicular electric field showed an excellent device with high on-off current ratio and a saturated current, the problem with this device is its complex structure that is very difficult to be used as a building block in integrated circuit. In that sense, GNR is a better candidate for graphene-based logic applications. Bandgap opening in GNR is induced by quantum confinements. In this quantum confinement effect, electrons occupy quantum well states which are discrete enabling a quantumly confined bandgaps. This phenomenon is shown in First Principle theory calculation where the size of the bandgap opening inside GNR was found to be inversely proportional to its width [28]. Due to this substantial bandgap opening, FETs with GNR channels show reduced off-leakage current and a larger on-off current ratio with a current saturation. Experimental and theoretical studies both show that GNR-FETs or GNR-tunneling FETs (GNR TFETs) with sub-10 nm GNR channels can produce a substantial band gaps with I_{on}/I_{off} ratios of higher than 10^6 achieved [37]. Another interesting application using GNR is GNR TFET which shows a subthreshold slope of 13 meV/dec [38] and has an advantage over the 60 meV/dec in conventional MOSFET making use of the tunneling effect.

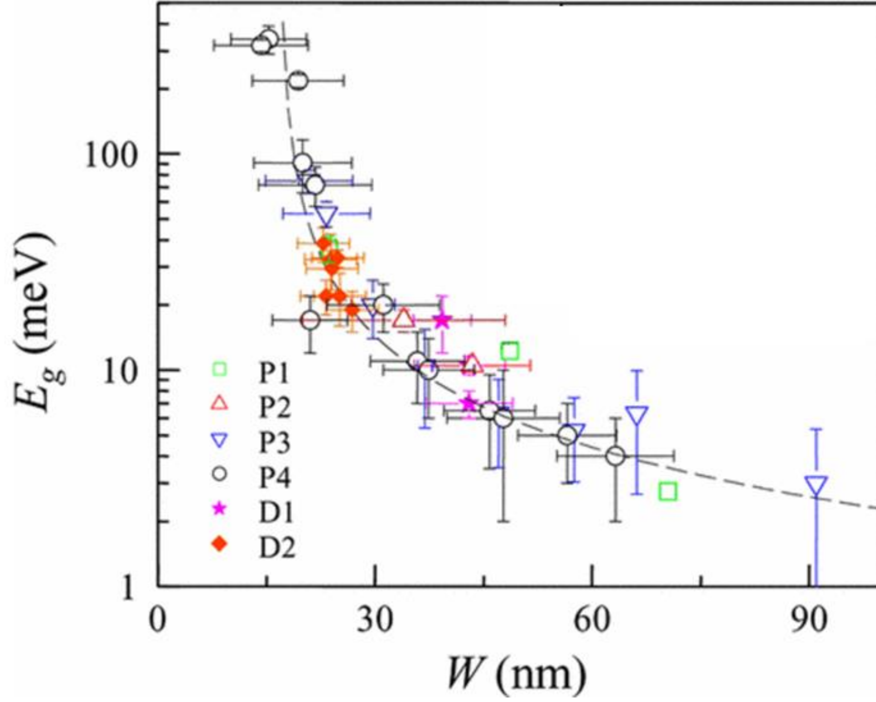


Fig. 8: Bandgap opening, E_g inside GNR. Eg is inversely propotional to GNR width. P1-P4, D1-D2 are different samples measured in this work. Reprinted with permission from [29]. Copyright by the American Physical Society.

However, one of the main challenges with GNR FET is to produce a smooth GNR down to 10 ~ 20 nm channel width where the size of bandgap opening is substantial. Conventional lithography and etching methods have been used to fabricate GNR FET with such channel width from both exfoliated graphene [39] and CVD graphene [40]. In this method, graphene edges cannot be fully controlled and defects or edge disorders have always been inevitable. These parasitic factors undermined the performance of GNR where devices show lower carrier mobility. In such cases, the bandgap opening is suggested to be dominantly arising from transport gap between localized states induced by the disorder instead of the quantumly confined bandgap. Therefore, cutting edge etching and fabrication technology needed to be properly developed to solve such issue in the near future. On the other hand, chemical unzipping of CNT [41, 42] enables production of GNR with smoother edge. When unzipping CNT, different chemicals were used in different previous works to break the bond

between carbon atoms and unzipped CNT into GNR. To prevent oxidation of produced GNR which is common after chemical unzipping process of CNT, 3 steps annealing process in [41] was introduced. Moreover, argon plasma etching had also been used to unzip CNT into GNR [43]. GNR with controlled edge without any disorder can also be synthesized by growing it directly on SiC substrates using ion implantation and laser annealing [44]. Although these bottom-up methods can produce GNR with smoother edges, it is not reproducible and still not compatible with conventional LSI technologies.

It is known that the edge state of GNR largely affects its characteristic. GNR conductivity changes drastically in zigzag or armchair edge as shown in Fig. 8. Generally, it is semiconducting in an armchair GNR (A-GNR) while zigzag edged GNR (Z-GNR) shows metallic properties. Theoretical prediction also shows that A-GNR can also be metallic and Z-GNR can be semiconducting. In the case of A-GNR, the dimer N, number or atoms forming the GNR width affects its characteristic. It is found that the characteristic differs in 3 different ways 3N, 3N+1 and 3N+2 [28]. A-GNRs with 3N and 3N+1 dimer are semiconducting while ones with a dimer of 3N+2 are metallic. Z-GNRs on the order hand show bandgap opening in GNR width of lower than 7 nm due to edge magnetism. This property has been found in both theoretical and experimental studies [45]. While the most stable structure of GNR edge is when it is being terminated with hydrogen atoms, terminations of the edges with other atoms or modulations of the edge states change GNR electronic band structure. Because of such effects, researchers strategically modulate the edge and width in different ways. These methods include applying disorder [46], doping [47], or mechanical strain [48].The main disadvantage of GNRFET is that, the drift current is significantly lower because of the nano-scale dimension of its width [49]. The mobility in GNR FETs are also lower because of the bandgap opening. Mobility and bandgap introduction of graphene and other materials from previous work is being summarized in Fig.10.

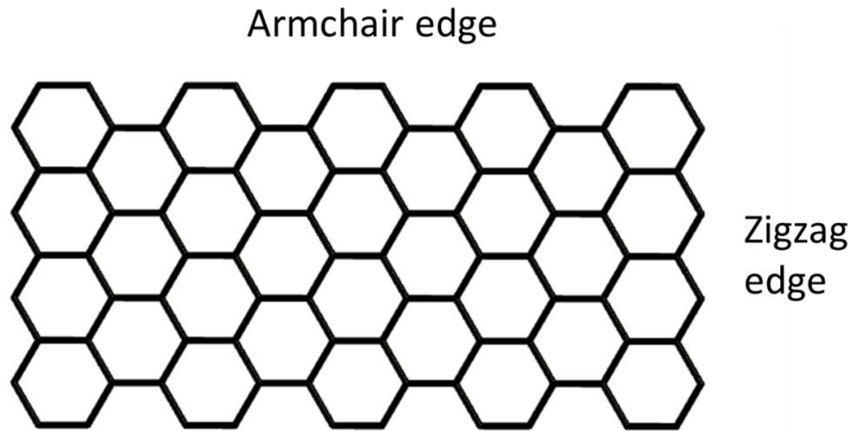


Fig. 9: Armchair and zigzag edge in GNR. The edge states affect the semiconducting and metallic properties in GNR.

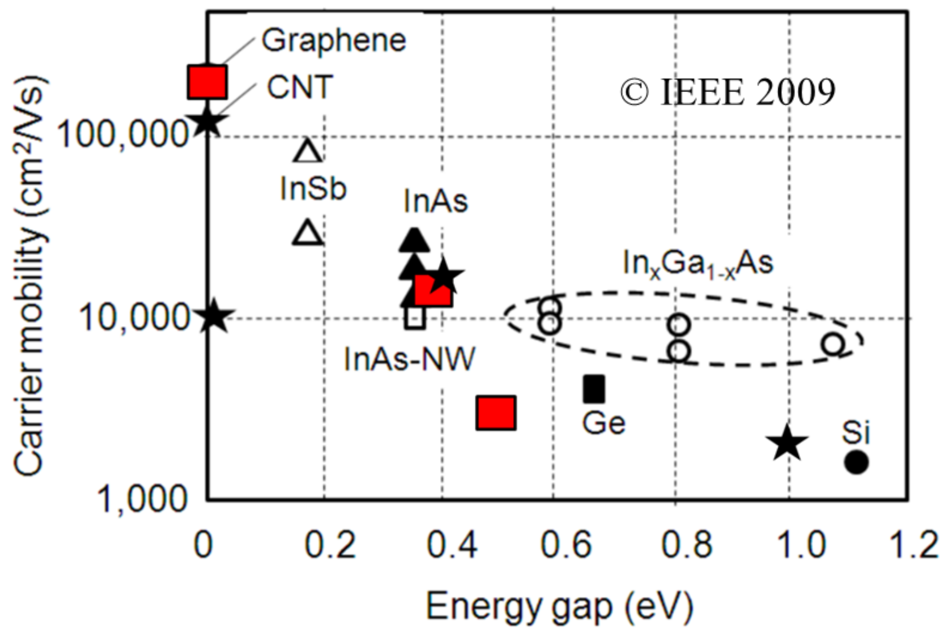


Fig. 10: Performance in terms of carrier mobilitiy (300 K) as a function of energy gap of materials to replace silicon in conventional CMOS [50]. Reprinted with permission from [51]. Copyright by IEEE.

On the other hand, researches on graphene interconnects have also been done intensively. Both wide graphene ribbon [52] (>100 nm) and graphene which is fabricated into narrow-width [53] (<100nm) graphene nanoribbon (GNR) have been systematically studied and compared to conventional copper interconnect. Multilayer graphene is a better candidate for the used in interconnect application due to its lower resistance. It has shown both an interesting temperature coefficient [54] and a theoretical projection that outperforms Cu as in interconnect applications [55]. In width of shorter than 8 nm, the resistance per unit length of GNR is surprisingly lower than that of Cu [56]. Morever, GNR interconnect shows an impressive breakdown current density in graphene wire which was reported by R. Murali *et al.* [54]. Initially, multilayer graphene interconnects are exfoliated from highly oriented pyrolytic graphite (HOPG) and kish graphite which is not suitable for large-scale manufacturing. In 2011, CVD-grown multilayer graphene has also been reported and the resistivity is lower prior to other researches [56]. However, despite all this promising data, the lowest value reported from experimental works for GNRs resistivity is still two and three times higher than copper wires. It is suggested this high resistivity mainly resulted from edge roughness scattering in GNR [54].

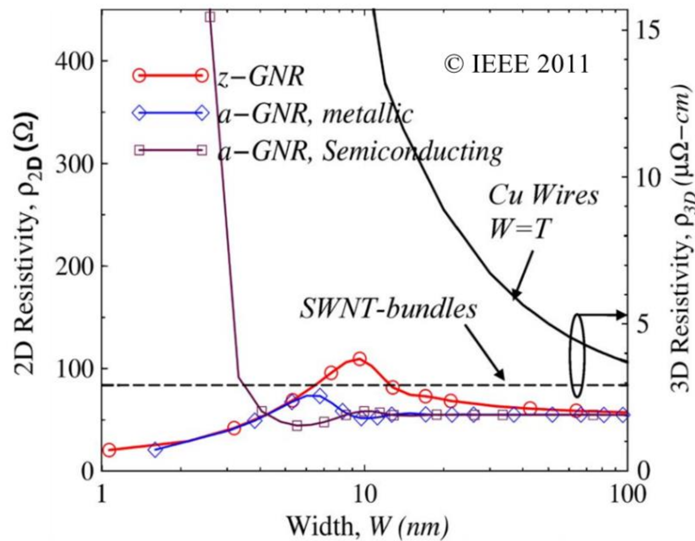


Fig. 11: Simulation result of the resistivity in single-layer GNRs of different edge states (a- armchair, z-zigzag) an MFP of 1 μm compared with those of copper wires and SWNT bundles.[57] Reprinted with permission. Copyright by IEEE.

1.3 Structure and Material Design in Graphene Electron Device

1.3.1 Previous Work on Graphene Device Structure Modification

In order to solve these challenges in the realization of graphene electron devices discussed in the previous sub chapter, some important works tackle these issues by modifying the structure of graphene devices. To suppress surface scattering of SiO_2 for example, a new GFET structure is reported by suspending the graphene channel in a device called suspended GFET. In this structure, the graphene is literally being suspended like a bridge between the source and drain of the channel without being on any SiO_2 surface. In this device, the carrier mobility of the device improved significantly and a similar value with the theoretical value can be obtained [58]. This structure is however mechanically unstable making it vulnerable of being damaged by a slight external force or a high current flow [59].

To deal with the lack of a bandgap an low current coupled with a low carrier mobility in GNR FET, in 2010, by modifying the physical structure of graphene, J Bai *et al.* introduce a new structure called graphene nanomesh (GNM) where bandgap opening is possible [60]. Although device current is usually low in GNR device because of the narrow channel, in GNM transistor, the current is not compromised because of the bandgap opening where a GNM device shows a nearly 100 time higher current than individual GNR device with similar bandgap opening. However, the conductivity of GNM transistor is ~1-2 orders of magnitude lower than of bulk graphene. Apart from physical modification, chemical modification can also open a bandgap in graphene. These modifications include partially oxidizing graphite [61] or by reducing graphene oxide [62], GO until a graphene like behavior is achieved is such cases. Other chemical modifications are hydrogenation of graphene basal plane [63], fluorination [64] and chemical doping [65]. Despite these breakthroughs, graphene-based device conductivity decreases as bandgap is opened up because of the mass is heavier and the E-k dispersion is flatter when the bandgap is enabled.

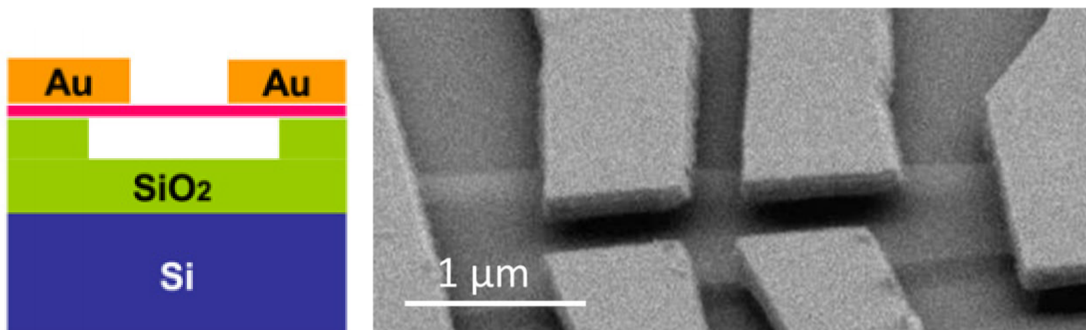


Fig.12: Suspended graphene device which show high carrier mobility since SiO2 surface scattering is absent. Reprinted with permission from [59]. Copyright by Elsevier.

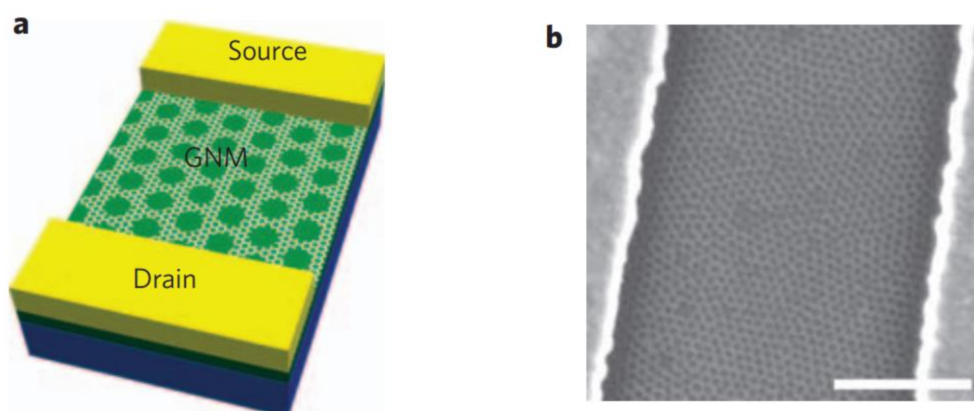


Fig.13: (a) Structure of Graphene Nanomesh (GNM) transistor where mesh are fabricated to induce bandgap inside graphene channel. (b) SEM image of a GNM device made from nanomesh with a periodicity 39 nm and neck width of 10 nm. Scale bar, 500 nm. Reprinted with permission from [61]. Copyright by Nature.

1.3.2 Previous Work on Graphene Interconnect Material Design

As discussed earlier, although graphene has a longer mean free path (MFP) than Cu, the Line Edge Roughness (LER) scattering increase the resistivity of GNR making it larger than Cu. The issue of this LER scattering is becoming more important in narrower GNR that is needed for future LSI applications. A way to reduce the resistivity in GNR is by doping. The motivation is to tailor the electronic properties by shifting the fermi level in GNR as a result of the doping effect. This will later lead to higher carrier density in graphene interconnects and a lower resistivity [66]. In 2010, a group reported that, by doping graphene with $AuCl_3$, they successfully reduced the resistivity of graphene by 77%. Other works also shows that the Fermi level of graphene can be controlled by doping. Depending on the dopant that is used the type of doping is decided whether it is a p-type doping or an n-type doping [67, 68, 69].

However, such that has been actively done to achieve doping effect in graphite to lower its resistivity [70], a better way of doping graphene in order to shift the fermi level without largely reducing the conductivity of graphene is by intercalation as chemical doping that is discussed earlier can affect the structure of graphene lattice by substitution doping [71]. Moreover, intercalation is better since multi-layer graphene can be doped this way. Intercalation is a method where intercalation compounds are inserted between the layers of graphene. The interlayer distance in graphite or graphene will significantly increase depending on the nature of the intercalation compound and this affects the electronic coupling between the layers which will then changing its property. Intercalation is a better way of doping since the structure of an intercalated graphene host is not largely change since intercalation compound does not bond with the carbon atoms in an intercalation process. Since the 1980s, intercalation of atoms such as alkali metals, halogens, oxygens and hydrogens has been reported by several groups and it is shown that resistivity is reduced in intercalated graphite [72, 73, 74]. Recently, several works on few layers and multi-layer graphene intercalations have also been done showing enhance resistivity and doping effect [75, 76].

For interconnect applications, intercalation of GNR wire is inevitable. Although there is a breakthrough of intercalating GNR which show a low resistivity, little is known on the stability of the intercalated GNR structure. In the case of graphite, there are cases where the intercalation compound escapes from the graphene over time

[77] leading to the resistivity of the graphite to increase again. There is also still a need to determine the most feasible candidate to be used as an intercalation compound with regards to its stability. Instability of an intercalated graphene host can also lead to the peeling of graphene flakes [78] which will deteriorate the intercalation structure.

1.4 Motivation of Thesis

The purpose of this research is to propose ways to solve the issues involving Graphene Electron Devices focusing on GFET and graphene interconnect by the approach of redesigning the graphene device structure and material.

To start with, our first objective is to propose a novel GFET structure in order to enhance the high speed property inside graphene channel. This new GFET architecture will make use of the overshoot velocity nature of carrier in graphene channel to enhance the carrier velocity inside the channel achieving faster transit time.

Our second objective is to focus on an extended version of the new design, making use of quantum confinement of GNR in order to achieve a bandgap opening inside our graphene device without comprising the high-speed performance.

Our third objective is to proposed a guideline towards interconnect with lower resistivity by investigating the stability of GNR intercalation. This work will provide an understanding of what is the factors affecting the stability of a GNR intercalation for the first time. This is a crucial guideline for intercalating GNR thus suggesting a way to find the best candidate to be used as an intercalation compound for GNR interconnect applications.

Chapter 2: Theoretical Framework

2.1 Introduction of theoretical method

In this chapter, different modeling tools that have been applied in evaluating the feasibility of the structural modification in our proposed new GFET structure and in intercalated GNR are described. An explanation to the Monte Carlo simulation method, First-principle Theory calculation and Molecular Dynamics simulation that are adopted and support the use of these modeling tools in this research. These simulation methods are used for:

I. Estimation of the transport properties in GFET with local channel modulation using Monte Carlo simulation
II. Bandstructure Calculation of the GNR array inside the modulated region using first principle theory calculation
III. Estimation of the stability in intercalated GNR using Molecular Dynamcis and first principle theory calculation

2.2 Semi Classical Monte Carlo Particle Simulation

There are several simulation methods that can be used to investigate the transport and electrical properties of a graphene transistor such as First Principle Theory, FPT, Tight Binding Model, TBM and Monte Carlo. MC Method. However, in terms of the precision of the calculated model, Monte Carlo (MC) [79, 80] simulation method is recognized as the best simulation method as it adopts a stochastic method where in this simulation model it involves the drift and scattering event of the particles under the presence of high electric field contributed by the terminal voltage of the transistor that cannot be simulated using DFT or TBM. The computational details will be discussed later on. First let us look at whole structure of the device simulation.

Our simulation is done in a program containing series of subroutines with several other functions in them. This series of subroutines and functions mimics the transport and electronic phenomenon inside the device. For examples, in the subroutine Monte Carlo, there are “drift1” and “scattering” functions where carriers will randomly travel without scattering (drift) or carriers will scatter by the scattering function. This whole program continues until the time, t reaches the maximum value that is set to be 1

ps in this simulation with dt being set to 0.2 fs and iteration set to 5000 times.
The time is set to 1 ps while considering the relaxation time of carrier transport which is confirmed after series of simulation with longer time (t = 2ps,4 ps) where the calculation results are similar with when t = 0.1 ps.

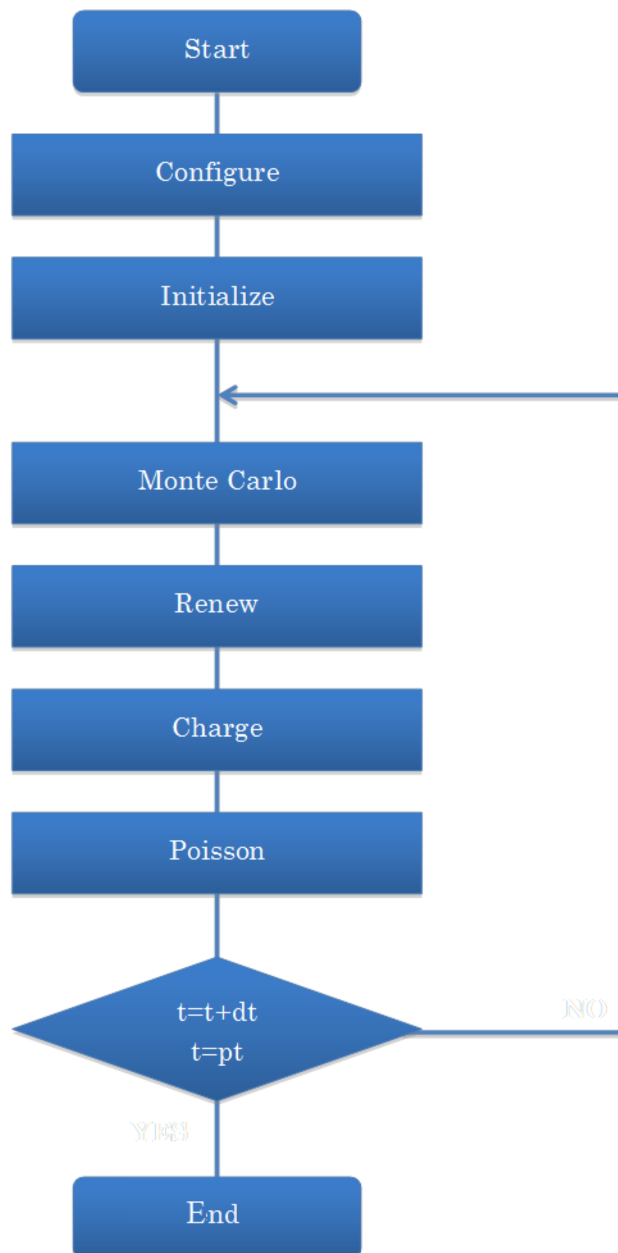


Fig. 14: Monte carlo simulation flow that is ued to estimate the properties of devices in this studies

i. Configure

This is the subroutine where the device structure is defined. Physical properties such as the dimension of the graphene transistor as well as the doping concentration of the graphene channel are defined here. In this theoretical investigation, we modeled a 2-dimensional Graphene Field Effect Transistor, GFET. These 2 dimensions are defined as x-dimension and z-dimension.

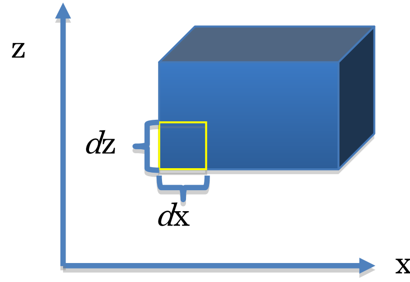


Fig. 15: Device Dimension

The whole structure is constructed with mesh that is *d*x of width and *d*z of height, which are set to be 2.0 nm and 0.5 nm respectively. In addition, this section of the subroutine creates matrices that are essential to solve the Poisson's equation which will be used to calculate the electrical potential inside the simulated device. There are 3 A, B, and C matrices defined here in this subroutine which will be explained in details. First, the 2-Dimensional Poisson's equation is given by:

$$\frac{d^2\emptyset_z}{dz^2} + \frac{d^2\emptyset_x}{dx^2} = -\frac{\rho}{\varepsilon} \qquad (1)$$

To solve this inside computer simulation, this equation will need to be converted into a difference equation. The difference equation is derived by considering the potential difference between a mesh with the meshes surrounding that particular mesh in the graphene channel as shown in Fig. 16.

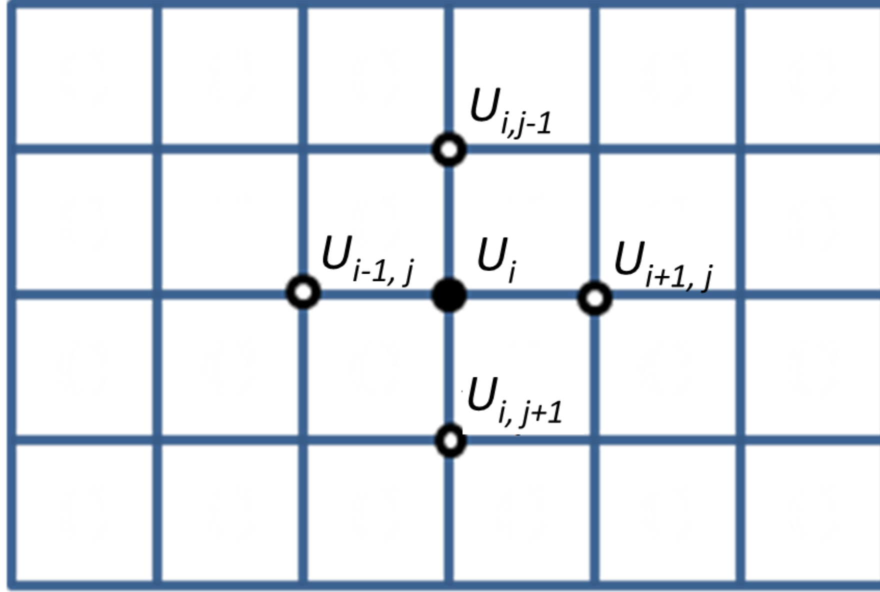


Fig. 16: Potential difference in meshes

From the potential difference shown in Fig. 16 we derive equation (2).

$$\frac{U_{i-1,j} - 2U_{ij} + U_{i+1,j}}{\Delta x^2} + \frac{U_{i,j-1} - 2U_{ij} + U_{i,j+1}}{\Delta z^2} = -\frac{N_{ij}}{\varepsilon}$$

$$U_{i-1,j} - 2U_{ij} + U_{i+1,j} + \frac{\Delta x^2}{\Delta z^2}(U_{i,j-1} - 2U_{ij} + U_{i,j+1}) = -\Delta x^2 \frac{N_{ij}}{\varepsilon}$$

$$U_{i-1,j} + U_{i+1,j} - 2\left(1 + \frac{\Delta x^2}{\Delta z^2}\right) U_{ij} + \frac{\Delta x^2}{\Delta z^2}(U_{i,j-1} + U_{i,j+1}) = -\Delta x^2 \frac{N_{ij}}{\varepsilon}$$

$$U_{i-1,j} + U_{i,j-1} - 2(1 + \varsigma)U_{ij} + \varsigma U_{i,j+1} + U_{i+1,j} = -\Delta x^2 \frac{N_{ij}}{\varepsilon} \qquad (2)$$

Three matrices of A, B, C that correspond to the equation above are created.

ii. Initialize

In this part of the subroutine, all the initial variables are being defined for each and every particle. Each variable holds the characteristic of the particles. These particles represent the carriers inside the GFET channel. There are 8 variables and each one of it is represented by a matric that are defined as PTC. Prior to the initialization of the variables, the number of the particles existing in every mesh is defined.

a) wave vector, x-direction: k_x, represented by PTC 1
b) wave vector, y-direction: k_y, represented by PTC 2
c) wave angle : theta, θ represented by PTC3
d) energy of particle : E_F, represented by PTC4
e) scattering time : T_S, represented by PTC5
f) position, x-dimension : x, represented by PTC6
g) velocity, x-dimension : V_x, represented by PTC7
h) velocity, y-dimension : V_y, represented by PTC8

The initialization subroutine then calculates the initial energy of the particle by using the equation.

$$\log \frac{\exp(r)}{2 - \exp(r)} k_B T \qquad (3)$$

r is a random number generate between 0 and 1. k_B is the boltzman constant while *T* is the temperature and is set to 300 K (room temperature). Using the value of energy, the wave number is calculated using equation (4) while considering that the band dispersion of monolayer graphene is linear.

$$k = \frac{E}{v_g \hbar} \qquad (4)$$

For the case with a bilayer graphene, a file containing the data of the bilayer energy dispersion is referred to when calculating the wave number.
The wave angle, θ, is generated using random number trough equation (5).

$$\theta = \pi(2r - 1) \qquad (5)$$

From this θ, the k_x, k_y and v_x is calculated using equation (6), (7), and (8) respectively.

$$k_x = k\cos\theta \qquad (6)$$
$$k_y = k\sin\theta \qquad (7)$$
$$v_x = v_e\cos\theta \qquad (8)$$

The initial scattering time is defined using next equation. Γ is the total scattering rate.

$$-\frac{\log(1-r)}{\Gamma} \qquad (9)$$

Then, finally, the position of the particles is calculated using 3 different equation considering the position of the particles at the edge part of the device.

Case 1: At the source edge of the FET (x=1)

$$x = 0.5 \cdot dx \cdot r \qquad (10)$$

Case 2: At the drain edge of the FET (x=151)

$$x = x_l - 0.5 \cdot dx \cdot r \qquad (11)$$

Case 3: Inside the device

$$x = dx(i + r - 1.5) \qquad (12)$$

iii. Monte Carlo

Fig. 17 shows the flow chart of the Monte Carlo subroutine. The initial state is first acquired by reading the data in the PTC matrices. The scattering time is then compared with the t + *d*t. If it is larger, then the particle will just drift for *d*t of time without any collision. On the other hand, if the scattering time is smaller, the particle will drift for t_{scat}-(t+*d*t) of time. After that, using random number, the scattering mechanism is selected and a new scattering time is generated. The loop continues until the scattering time is larger than t+*d*t.

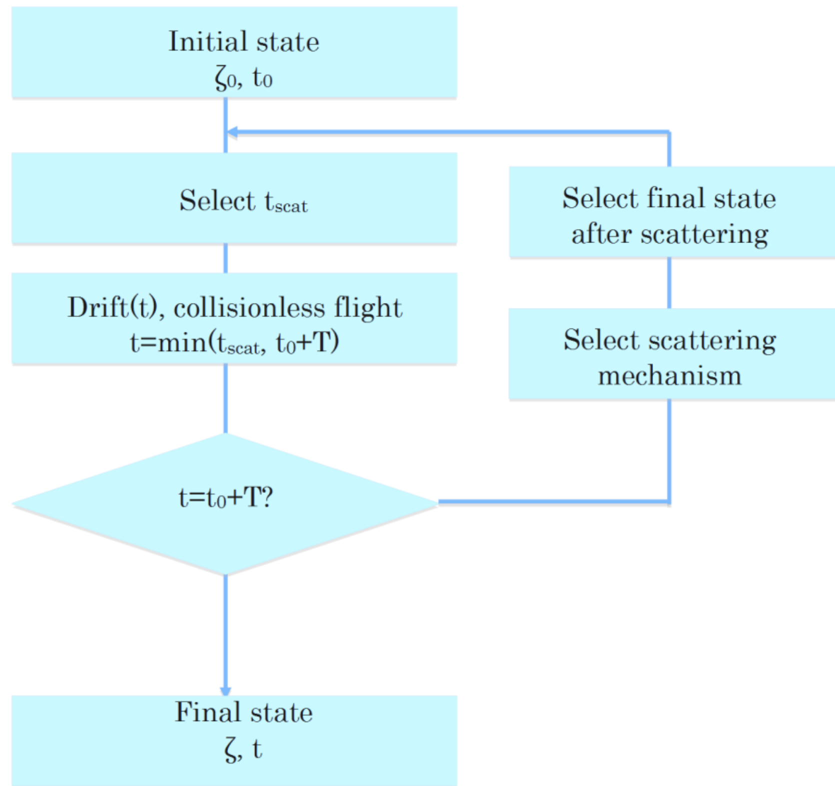


Fig. 17: Monte Carlo Flow Chart which include drift and scattering event of carriers.

At the end the end of the drift function, there is a function call annihilation where particles that come out from the edge of the transistor (x < 1*dx* or x > 151*dx*) are

flagged with a matric called IP and is set equaled to 9. By default, this IP matric return 0 value for each particle and only the particle being flagged returns the value of 9.

iv. Renew

This is the part where the matrices of the particles are newly constructed and all the particles that have gone out from the device are removed from the matrices.

v. Charge

This subroutine is the part where the charge distribution in the channel is calculated. The charge distribution is calculated by determining the number of electron per particle. The number of electron per particle varies with the position of the particle.

vi. Poisson

Poisson's equation that is being solved in this simulation is equation (1) like being discussed in the configure subroutine. In that section, the 3 matrices only represent the left part of equation (2). When the whole equation is converted into matric form, it will look like equation (13) below.

$$([A]+[B]+[C])\begin{pmatrix} U_{00} \\ U_{01} \\ U_{02} \\ . \\ . \\ . \\ . \\ . \\ U_{ij} \end{pmatrix} = -\frac{1}{\varepsilon}\begin{pmatrix} N_{00} \\ N_{01} \\ N_{02} \\ . \\ . \\ . \\ . \\ . \\ N_{ij} \end{pmatrix} \qquad (13)$$

A, B and C represent the three matrices we created in *configure* subroutine. U represents the electric potential while N is the charge distribution. N is defined in equation (14).

$$N = q(n - N_D)\,\Delta x^2 \qquad (14)$$

So, except for the voltage potential, all variables are known. So, using the inverse matrix of [A]+[B]+[C], the voltage potential is determined.

2.2 First-principle theory calculation

Next, first-principle theory calculation will be briefly explained the. Historically computational methods used as a scientific approach to understand the property of materials had started back since 1950. However, it was only in 5-10 years back that much more complex quantum mechanical methods were developed were simulations of molecules and materials can be done in which atomic forces can be obtained by solving the interaction of ions and electrons together [81]. There are many quantum mechanical methods where the level of approximation differs: empirical or semiempirical orthogonal tight-binding methods are the simplest [82]; nonorthogonal tight-binding and nonself-consistent Harris-functional methods are next [83]; and fully self-consistent density functional theory (DFT) methods are the most complex and reliable ones [84].

In this research, DFT is used to calculate the bandstructure of a GNR array inside the modulated region of the new GFET structure in order to later simulate this MC device simulation. In this method, Schrödinger equation is solved to calculate the electronic energy of system using the electron density functional, which is defined in one to one relation with the electronic wave function. The DFT method was previously used to study possible bandgap opening in GNRs [28, 85].

2.2.1 Basic of Quantum mechanics

The basic of Quantum mechanics involve around solving equation the Schrödinger equation. Accordingly, in order to understand the electronic structure of a system, the Schrödinger equation needs to be solved. The fundamental equation in quantum mechanics is given by,

$$\hat{H}\psi = E\psi \qquad (15)$$

where Hamiltonian operator, $\hat{H}$ is used to calculate the total energy of the system when E is applied to the wave function, ψ. The energy can be computed by solving this Schrödinger equation, which in Born-Oppenheimer approximation is;

$$\hat{H}\psi(r_1, r_2, \dots, r_N) = E\psi(r_1, r_2, \dots, r_N) \qquad (16)$$

$\hat{H}$ consists of a sum of three terms; the kinetic energy, the interaction with the external potential (V_{ext}) and the electron-electron interaction (V_{ee}). This can be defined as follows:

$$\hat{H} = -\frac{1}{2}\sum_{i}^{N} \nabla_i^2 + V_{ext} + \sum_{i<j}^{N} \frac{1}{|r_i - r_j|} \qquad (17)$$

External potential in this case is simply the interaction of electrons with the atomic nuclei;

$$V_{ext} = -\sum_{a}^{N_{at}} \frac{Z_a}{|r_i - R_a|} \qquad (18)$$

Here, r_i is the coordinate of electron i and the charge on the nucleus at R_a is Z_a. The equation is solved by:

$$E_i = \int \psi_i \hat{H} \psi_i dr \qquad (19)$$

With the energy of the system derived from eigenvalue E_i which corresponds to the eigenfunction of system i. However, as you can see, to solve this equation there is a need to know the wavefunction ψ_i. ψ_i is given by variables of 3N dimension with N being the number of electron. Therefore, while it maybe is possible to find the wavefunction and solve the equation in smaller system of a few atoms, it is very difficult to be solved in larger systems with a large number of atoms. In conclusion, system sizes that can be treated with wave function based methods is severly limited.

2.2.2 Density Functional Theory [86,87, 88]

In DFT, to solve the Schrödinger equation that we briefly introduce earlier, there is no need to know the 3N dimensional wavefunction. Instead, the Schrödinger equation is reformulated in terms of the electron density where instead of using wavefunction, electron density is used as the central quantity. The advantage of using the electron density over the wave function is the fact that no matter how many electrons there is in the system, the density is always 3 dimensional. The limited number of atoms can be calculated in a system is no more and this enables DFT to be applied to much larger systems, hundreds or even thousands of atoms. Largely because it is computationally cheaper DFT has become the most widely used electronic structure to date.

This fundamental idea is introduced way back in 1972 by Thomas and Fermi [89,90]. However the final version of the modern DFT that is widely used rests on two fundamental theorems provided by Kohn and Hohenberg and a set of equations formulated by Kohn and Sham [91]. The Kohn-Sham equations make it possible to generate the electron density of a non-physical and non-interacting system by defining their orbitals. In its final form, energy E of the ground state can then be expressed as a function of the electron density:

$$E[\rho] = -\frac{1}{2}\sum_{i=1}^{N} \varphi_i^*(r_i)\nabla^2\varphi_i(r_i)dr_i - \sum_{x=1}^{N}\frac{Z_x}{r_{xi}}\rho(r_i)dr_i + \frac{1}{2}\iint \frac{\rho(r_1)\rho(r_2)}{r_{12}}dr_1 dr_2 + E_{XC}[\rho] \quad (20)$$

The first term represents the kinetic energy of the non-interacting electrons, the second term refers for the nuclear-electron attractions, and the third term describes the Coulomb repulsion between the total charge distribution at the point r_1 and r_2 in space. The last term, $E_{xc}[\rho]$, is called the exchange correlation functional and represents the kinetic energy arising from the interaction between the electrons and all the non-classical corrections to the electron-electron energy. By solving this equation, we can solve the Shrodinger equation and understand the electronic structure of a system. In this work, DFT calculation is performed using Quantumwise Atomistix Toolkit which uses the SIESTA (Spanish Initiative for Electron Simulations with Thousands of Atoms)

method [92].

2.3 Molecular Dynamics

In the late 1950s and the early 1960s, intensive works on the dynamics of fluids by Alden and Wainwright and by Rahman has lead to the foundation of Molecular Dynamics (MD). MD is one of the pioneering applications form their research and since then, MD has becoming an indispensible and valuable tool in simulating and estimating the behavior of both chemical and physics system. Boosted by the advancement in the computer technology and algorithm development, since 1970s MD is widely used for such purposes. In this research, classical MD is used to calculate the stability of GNR host which is intercalated with intercalation compound. Although such simulation can be more precisely done using DFT, MD simulation is adopted as it is faster and more computationally cheap since the system that is calculated is large.

MD simulation targets to solve the classical equation of motions with a numerical, step-by-step, calculation. By solving the equation of motion, all the interaction between atoms or molecules inside the system can be simulated and understand. The most notable difference between MD simulation and DFT is that these intercations inside the system are defined before the simulation started. In a classical non bonded interaction the interaction is given by,

$$U_{\text{non-bonded}} = \sum_i u(r_i) + \sum_i \sum_{j>i} v(r_i, r_j) + \cdots \quad (21)$$

This potential energy Unon-bonded need to be solved to calculate the forces inside a system which then can be used to solve the classical equation of motion. In this equation, $u(r)$ term represents an externally applied potential field such as the effects of the container walls. The pair potential $v(r_i, r_j) = v(r_{ij})$ is usually focused and three-body (and higher order) interactions are neglected. Therefore, the way the potential is being modeled is very important and give the idea of what approxiamtion has been given to the simulation of the system. The method of how these potentials are determined experimentally, or modelled theoretically are extensively done [93, 94] .

In this research, the pair potentials are derived from other theoretical literature. One of the most common pair potential that is being used is the continuous, differentiable Lennard-Jones pair potential (LJ potential). LJ potential is given by:

$$v^{\mathrm{LJ}}(r) = 4\varepsilon\left[\left(\frac{\sigma}{r}\right)^{12} - \left(\frac{\sigma}{r}\right)^{6}\right] \quad (22)$$

This form of Lennard-Jones potential is the most commonly usedwith two parameters: σ, the diameter, and ε, the well depth.

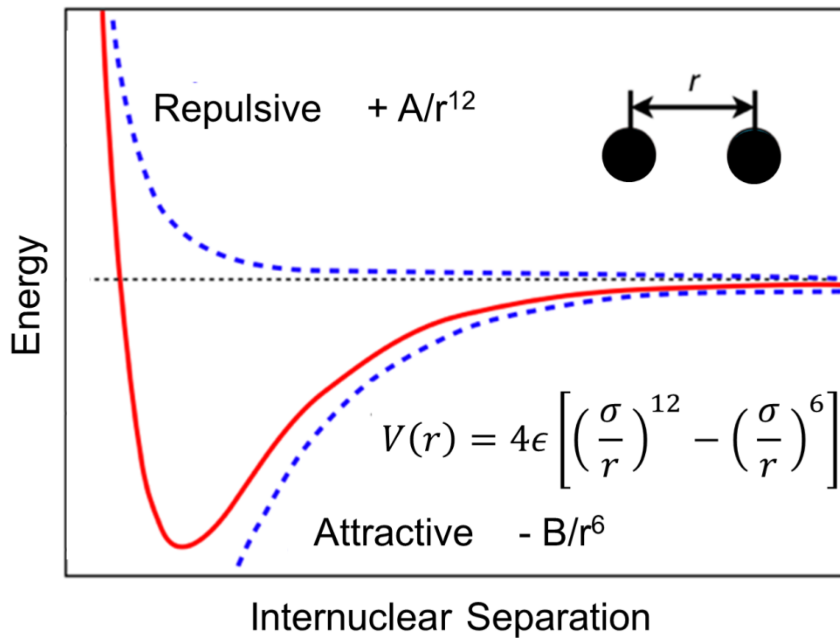


Fig. 18: LJ pair potential that make use of the repulsive and attractive interaction between 2 atoms or molecules

If electrostatic charges are present, we add the appropriate Coulomb potentials:

$$v_{Coulomb}(r) = \frac{Q_1 Q_2}{4\pi\epsilon_0 r} \qquad (23)$$

where Q_1, Q_2 are the charges and ϵ_0 is the permittivity of free space. Another common pair potential which is used in our MD simulation is Morse pair potential. Morse potential is also simple and widely used to define interatomic interactions. Morse potential is given by:

$$V(r) = D_e\left(e^{-2a(r-r_e)} - 2e^{-1(r-r_e)}\right) \qquad (24)$$

where r is the distance between the atoms, r_e is the equilibrium bond distance, D_e is the well depth (defined relative to the dissociated atoms), and a controls the 'width' of the potential (the smaller a is, the larger the well).

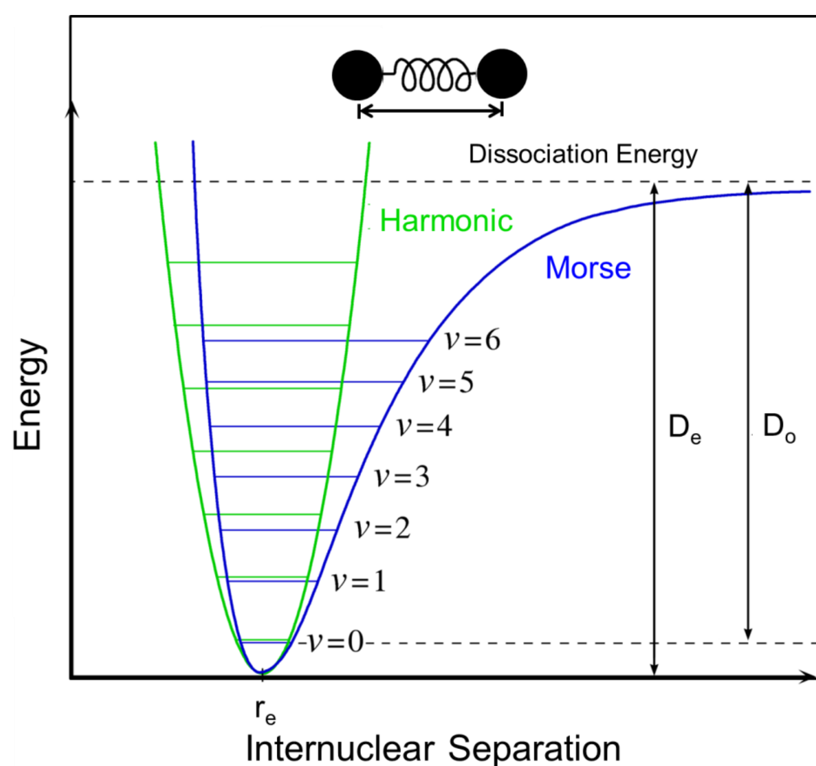


Fig. 19: Morse potential includes the disassociation energy between two atoms

Chapter 3: High Speed Properties in Modulation Channel Width (MCW) GFET

3.1 Introduction of Chapter 3

As discussed in the first chapter, there is still a dire need to improve the performance of graphene transistor that is being researched and proposed to date since there is no research that has been able to systematically solve the most critical issue of enhancing graphene device's high speed transport property while introducing a bandgap inside the graphene channel at the same time. In this chapter, the first part of the issue is focused, where a new GFET structure is proposed to enhance the high speed property of carriers inside the graphene channel. Monte Carlo device simulation is used to estimate the transport and electrical property of this device. This device is called a Modulated Channel Width Graphene Field Effect Transistor (MCW-GFET). To evaluate the transport properties in MCW-GFET, the mean velocity profile of simulated devices are focused on. From the profile, transit time, τ is extrapolated and evaluated. The high-speed performance enhancement is determined by a faster transit time. Although the newly proposed structure might be complex to be fabricated with any other semiconducting materials, the two-dimensional physics of graphene makes such fabrication possible. Advanced etching technology such as focused He-ion beam milling can be used to fabricate graphene nano device with the capability of sub-10 nm [95].

3.2 Overshoot velocity effect in short-channel FET

It was found that the carrier velocity was higher than its saturation velocity in a short-channel FET where the carrier velocity peaked before saturated [96]. This is called an overshoot velocity effect were the carriers in semiconductors response time-dependently to the electric field and if the electric field is high enough, the carrier stay in an overshoot final velocity for a several picoseconds [97]. The overshoot velocity phenomenon occurs due to two reasons [98]. First, when the momentum relaxation rate is larger than the energy relaxation rate. Second, there is a heavier mass conduction valley at low enough energy where the electrons significantly populate at steady state. So, by increasing the electric field along the graphene channel, we can accelerate the carriers in the GFET to achieve a higher overshoot velocity. It is suggested that

overshoot velocity in graphene is due to the first factor where overshoot velocity occurs because of larger momentum relaxation time compared to energy relaxation rate. This carrier acceleration will enhance the high-frequency and high-speed performance, such as a faster transit time, especially when taking place at the source side of the channel [99, 100].

In that case, it is considered that introduction of a high electric field at especially the source side of the channel is crucial in order to shorten the transit time in transistors. There are several methods to do so. Methods such as increasing the doping concentration or changing the thickness of the source and drain regime can introduce this high electric field. However these methods will consequently change the threshold voltage of the transistor.

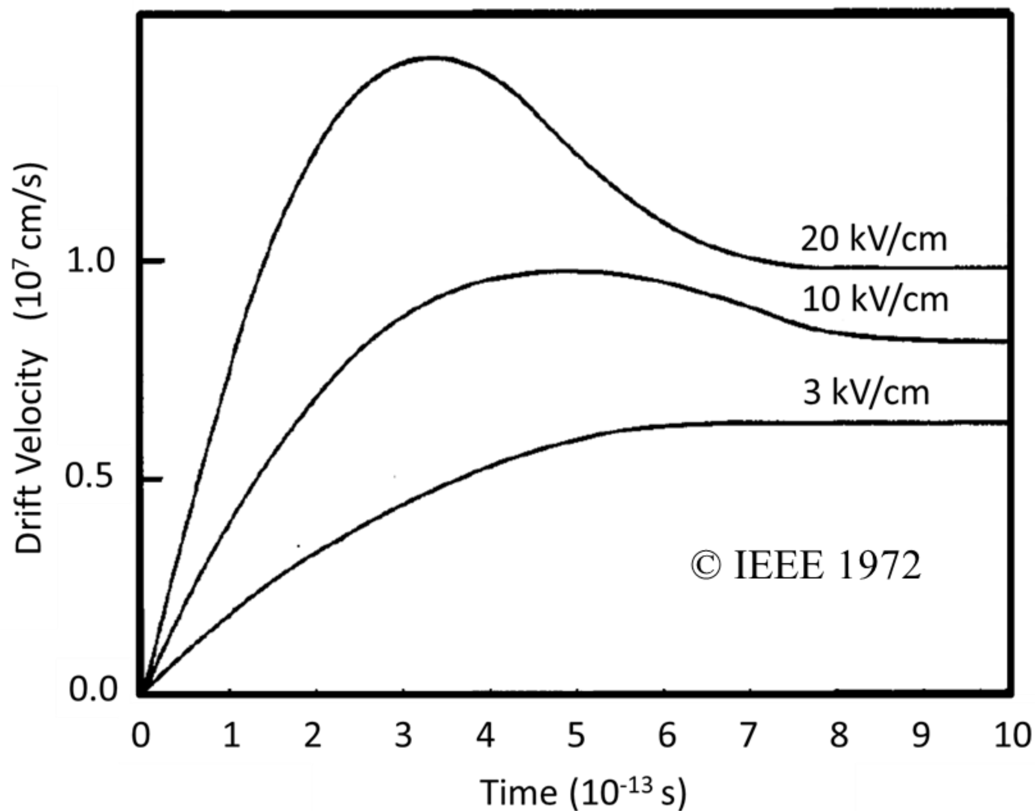


Fig. 20: Velocity overshoots effect in Silicon. Reprinted with permission from [98]. Copyright by IEEE.

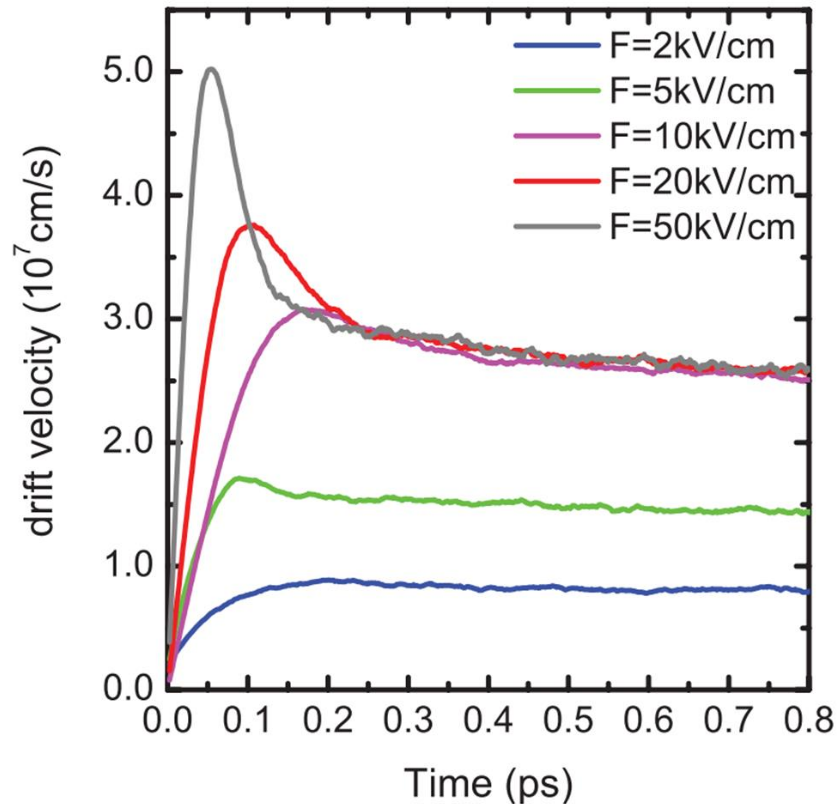


Fig. 21: Velocity overshoots effect in Graphene FET. Reprinted with permission from [101].

In a previous theoretical study by Awano *et al.* [102], it was reported that the carrier mean velocity increased significantly (30%) in a HEMT with a nonuniformed channel. It was speculated that this result is due to introduction of a high electric field at the source side of the channel without changing the threshold voltage. This high electric field was yields by the nonuniformed structure of the HEMT.

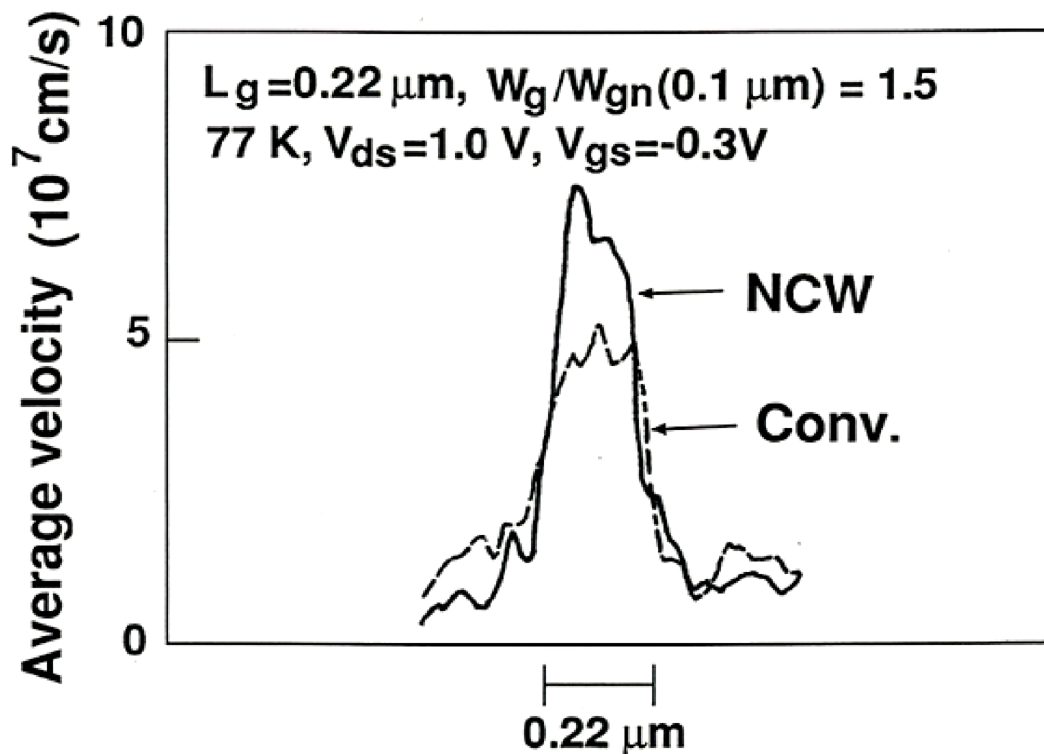


Fig. 22: HEMT with nonuniformed channel structure. Average velocity of the transistor in such channel increased.

3.3 Design Principle of MCW-GFET

The new GFET structure introduces a local modulation of the channel width and is called a Modulation Channel Width (MCW) GFET. In this novel structure, the modulation of the width involved locally narrowing the channel width specifically at the source side of the channel. The motivation behind this channel modulation is to achieve a strong electric field at the modulated region that will accelerate the carrier's velocity inside the channel. This will lead to a higher performance FET in terms of the high speed velocity. The theory is that the strong electric field can be induced at modulation region since there is higher density of electrical flux in that region as a result of the narrowed channel width. This carrier acceleration by the strong electric field will then translate into a faster carrier transit time. It is worth noting that since this channel modulation is done at its width, no change in the threshold voltage can be expected. This is how the overshoot velocity effect is adopted.

3.4 Simulation Model of MCW-GFET for High Speed Enhancement

3.4.1 Simulated Device Structure

The general structure of the device considered in this simulation is shown in Fig. 23. Insulators are formed on both the top and bottom parts of the graphene channel forming a sandwich device structure. The thickness of both insulators is 10 nm with a dielectric constant of $2.4\varepsilon_0$. The graphene channel is doped n+($1x10^{18}$ cm^{-3}) -n($1x10^{16}$ cm^{-3}) - n+($1x10^{18}$ cm^{-3}). The lengths of the n+-layer source, n+-layer drain, and n-layer channel are all 100 nm in length, making the device dimension 300 nm long. The initial number of particles is 20 000 and the lattice temperature is set to 300 K.

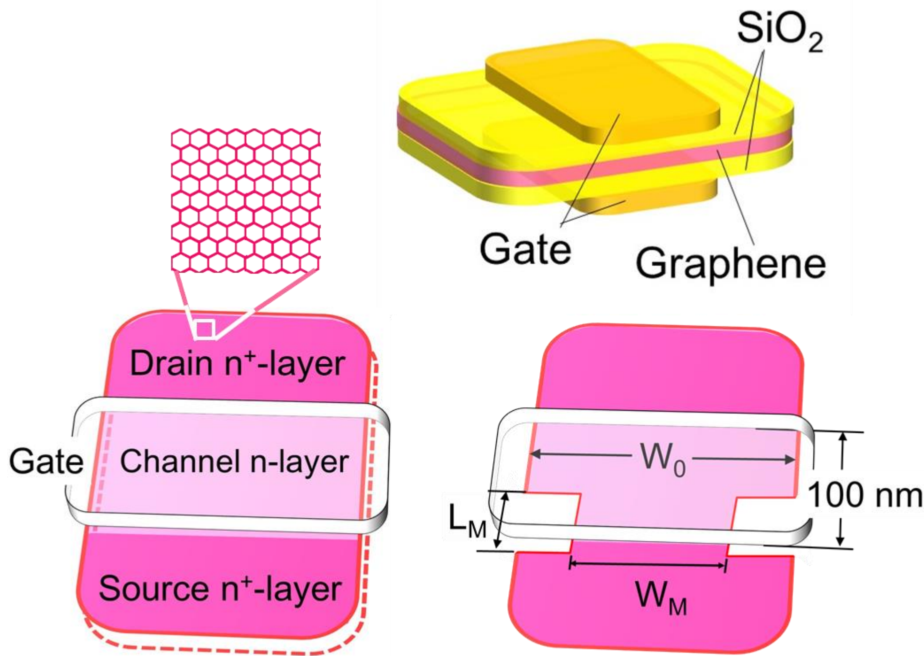


Fig. 23: Modeled device structure

The scattering mechanisms being considered in this simulation are acoustic phonon elastic scattering and inelastic optical phonon emission. The scattering rates for elastic scattering and inelastic phonon emission are 1.0×10^{13} and 1.0×10^{12} respectively. It is assumed that the scattering rate is independent of energy, electron density, and

spatial distribution. Such approximation is considered as it is shown that an average of only 4% difference was found when comparing the velocity profiles in devices with an energy dependent model and the constant model as reported by N. Harada *et al.* using the same scattering rate value [104]. The optical phonon energy is 0.155 eV. We perform the Monte Carlo motion simulation at the x-axis while solving Poisson's equation at the x-z plane [103]. In order to achieve the MCW GFET structure, we adjust the width ratio, W of the graphene channel all along the device, creating notches at the source and gate region. W is given by channel dimension (W_M the number of stripes) /W_0, as shown in Fig. 23.

3.4.2 Quasi 3D Poisson solver

Since this generates a nonuniform channel in the y-direction of the device, the Poisson's equation is modified to include W as a new parameter in the 2D x-z plane Poisson's solver, and with that, a quasi-3D Poisson's equation is achieved.

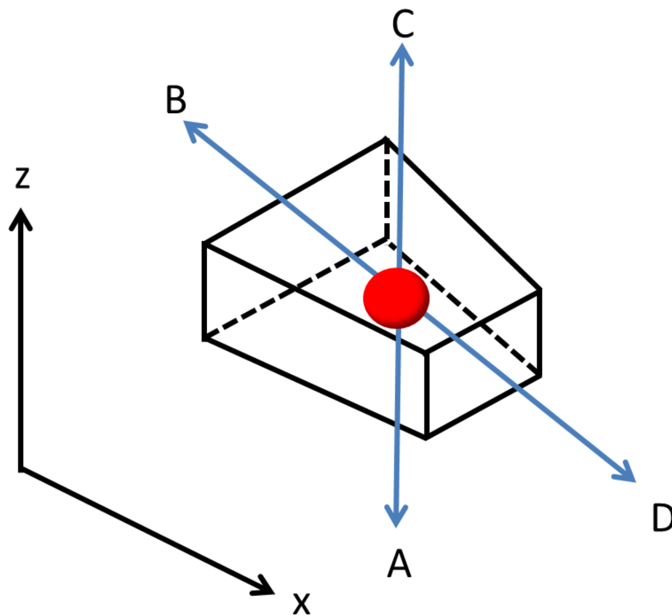


Fig. 24: Charge confined in a nonuniform cubic

2D Poisson's equation:

$$U_{i-1,j} + \zeta U_{i,j-1} - 2(1+\zeta)U_{ij} + \zeta U_{i,j+1} + U_{i+1,j} = -\frac{\Delta x^2 N_{i,j}}{\varepsilon} \quad (26)$$

$$\text{where } \zeta = \frac{\Delta x^2}{\Delta z^2}$$

Quasi-3D Poisson's equation:

$$U_{i-1,j} \cdot \min(W_i, W_{i-1}) + \zeta U_{i,j-1} \cdot W_i - [2\zeta W_i + \min(W_i, W_{i-1}) + \min(W_{i+1}, W_i)]U_{ij} + \zeta U_{i,j+1} \cdot W_i + U_{i+1,j} \cdot \min(W_{i+1}, W_i) = -\frac{\Delta x^2 N_{i,j}}{\varepsilon} \quad (27)$$

This quasi-3D Poisson's equation is derived using Gauss's Law by considering a situation wherein an electric charge is confined in a nonuniformly shaped cubic as shown in Fig.20. The total charge$Q$ over ε, enclosed within the cubic can be defined by:

$$\frac{Q}{\varepsilon} = \oiint_S \boldsymbol{E} d\boldsymbol{A} \qquad (28)$$

The surface integral of electric field then can be defined using the given component E_A, E_B, $E_C$and $E_D$as:

$$\oiint_S \boldsymbol{E} d\boldsymbol{A} = E_A \cdot \Delta x \cdot W_i + E_B \cdot \Delta z \cdot \min\left(W_{i,} W_{i-1}\right) + E_C \cdot \Delta x \cdot W_i + E_D \cdot \Delta z \cdot \min\left(W_{i+1,} W_i\right) \qquad (29)$$

Since,

$$E_A = \left(-\frac{U_{i,j-1} - U_{ij}}{\Delta z}\right) \qquad (30)$$

$$E_B = \left(-\frac{U_{i-1,j} - U_{ij}}{\Delta x}\right) \qquad (31)$$

$$E_C = \left(-\frac{U_{i,j+1} - U_{ij}}{\Delta z}\right) \qquad (32)$$

$$E_D = \left(-\frac{U_{i+1,j} - U_{ij}}{\Delta x}\right) \qquad (33)$$

Equation (29) can be expanded to:

$$\left(\frac{U_{i,j-1} - U_{ij}}{\Delta z}\right) \cdot \Delta x \cdot W_i + \left(\frac{U_{i-1,j} - U_{ij}}{\Delta x}\right) \cdot \Delta z \cdot \min(W_{i,} W_{i-1}) +$$

$$\left(\frac{U_{i,j+1} - U_{ij}}{\Delta z}\right) \cdot \Delta x \cdot W_i + \left(\frac{U_{i+1,j} - U_{ij}}{\Delta x}\right) \cdot \Delta z \cdot \min(W_{i+1,} W_i) = \frac{Q}{\varepsilon}$$

$$\frac{\Delta x}{\Delta z} \cdot W_i(U_{i,j-1} - 2U_{ij} + U_{i,j+1}) + \frac{\Delta z}{\Delta x}[(U_{i-1,j} - U_{ij}) \cdot \min(W_{i,} W_{i-1})$$

$$+(U_{i+1,j} - U_{ij}) \cdot \min(W_{i+1,} W_i)] = \frac{Q}{\varepsilon} \qquad (34)$$

By replacing $Q = \Delta x \Delta z W_i \cdot q \cdot N_{ij}$ which represents electric charge in device, (q is the charge per electron and N_{ij} is the carrier density)

$$U_{i-1,j} \cdot \min(W_i, W_{i-1}) + \frac{\Delta x^2}{\Delta z^2} U_{i,j-1} \cdot W_i - [2\frac{\Delta x^2}{\Delta z^2} W_i + \min(W_i, W_{i-1})$$

$$+\min(W_{i+1}, W_i)]U_{ij} + \frac{\Delta x^2}{\Delta z^2} U_{i,j+1} \cdot W_i + U_{i+1,j} \cdot \min(W_{i+1}, W_i) = -\frac{\Delta x^2 N_{i,j}}{\varepsilon} \qquad (35)$$

By replacing $\zeta = \frac{\Delta x^2}{\Delta z^2}$, equation (27) is derived.

The value of W is adjusted along the devices such that it defines the narrowed or modulated channel region.

3.5 Result and Discussion

3.5.1 Electric Field Profile (MCW-GFET W= 0.1, W= 0.3)

Performance estimation is started by evaluating the electric field profile specifically at the modulation region near the source side of the channel (Position, X= 100-150 nm). From the result shown in Fig. 25 and Fig. 26, we find out that strong electric field are induced in both MCW-GFET devices with a monolayer and a bilayer channel. The strongest electric field is up to 2×10^4 and 1.68×10^4 V/cm in monolayer and bilayer MCW-GFET devices respectively when W=0.1 in both cases. This result shows that introduction of local strong electric field is achieved at the modulated region as can be seen when observing the electric field inside the whole channel of the device in Fig. 27.

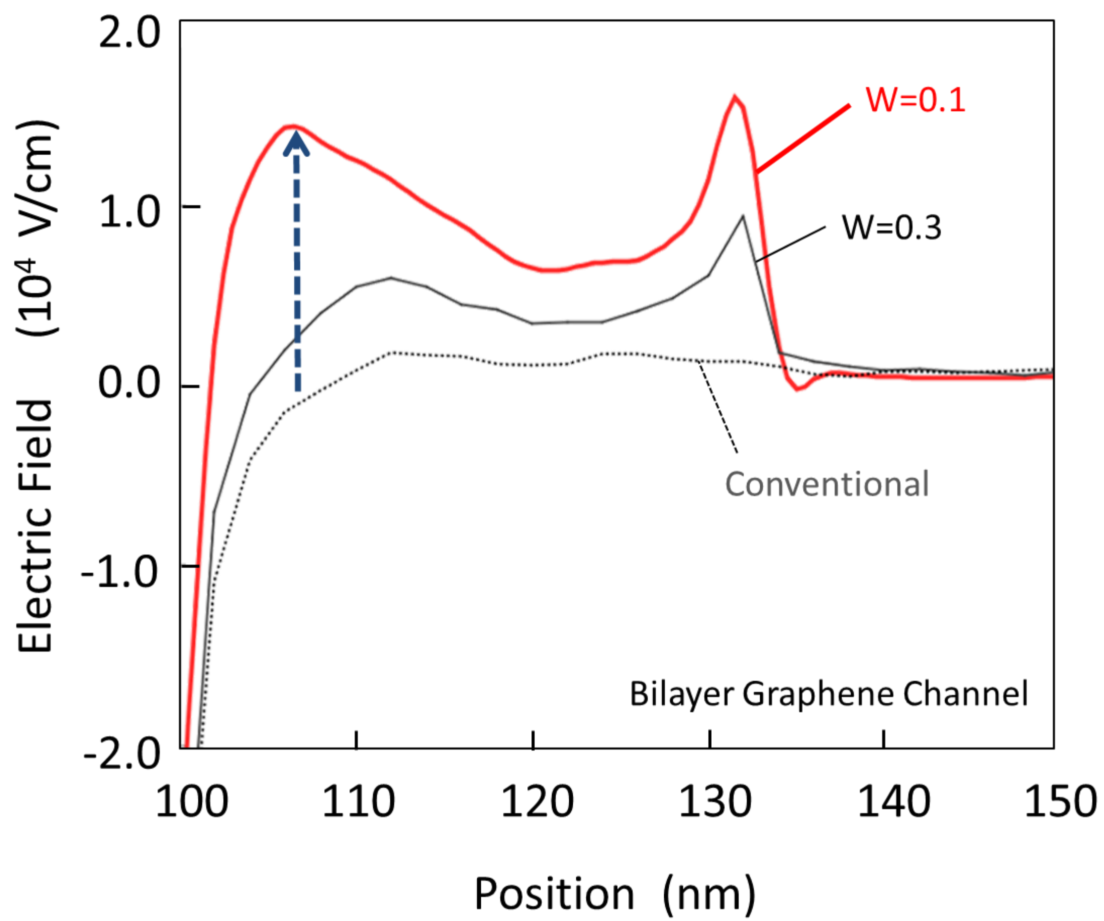


Fig. 25: Electric Field in MCW-GFET with a bilayer graphene channel

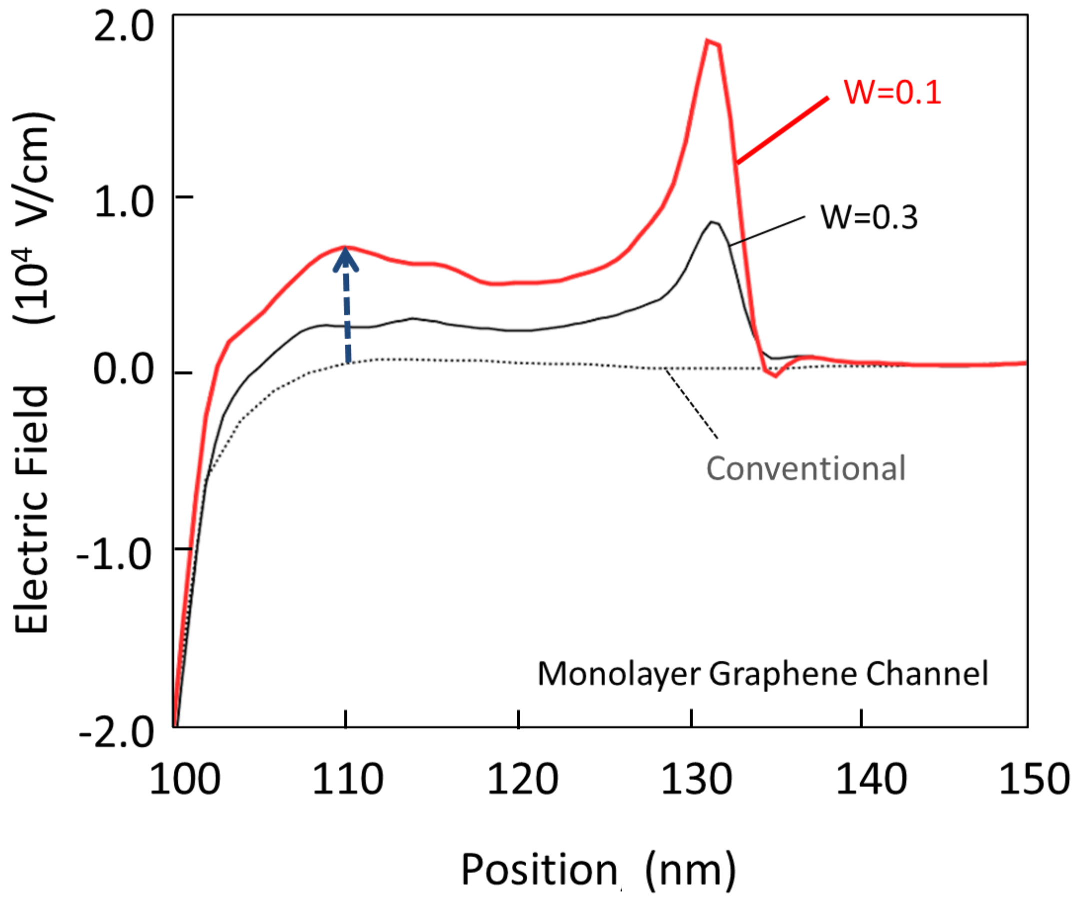


Fig. 26: Electric Field in MCW-GFET with a monolayer graphene channel

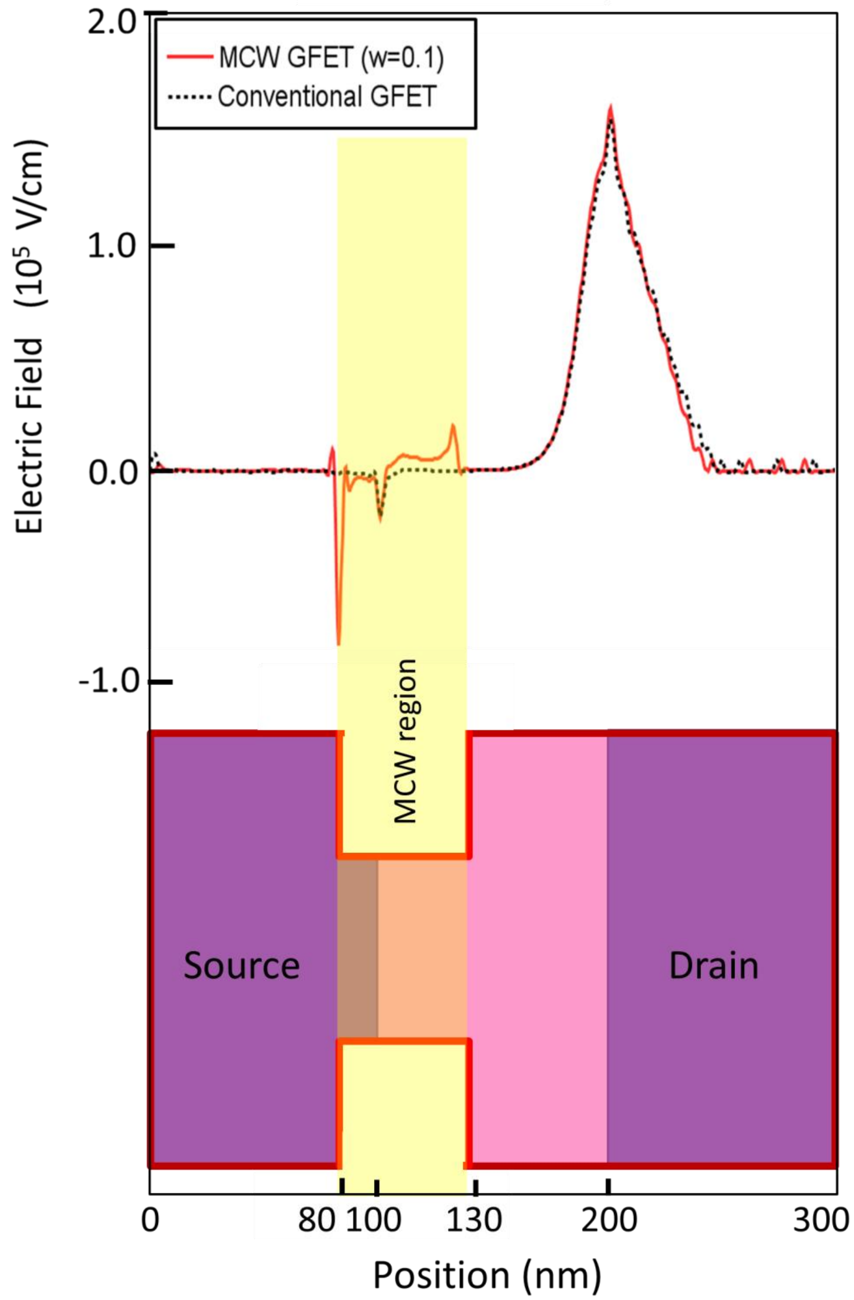


Fig. 27: Full Electric Field profile in MCW-GFET and Conventional GFET with a monolayer graphene channel. Local stronger electric filed is introduced at the modulated region.

3.5.2 Mean Carrier Velocity (MCW-GFET W= 0.1, W= 0.3)

Next, we further observed the mean carrier velocity in both devices to see the effect of stronger electric field. It was evident from the results in both MCW-GFETs with bilayer and monolayer graphene channel that stronger electric fields had an effect on mean carrier velocity shown in Fig. 28 and Fig. 29. The mean carrier velocity increased in both cases when W=0.3 and W= 0.1. When clearly observed, in the case of device with bilayer graphene channel, the highest increase in the mean velocity (W= 0.1) was observed near the source region, 22nm from the source edge inside the channel region. It is a 52% increase from 1.67×10^5 to 3.93×10^5 m/s.

When taking the transit time τ of the particles into account, the time needed for the carriers to travel along the channel from the source to the drain region of the MCW-GFET, it shortened greatly by 38% from 0.38 to 0.24 ps. Since the intrinsic high-frequency high-velocity performance is frequently determined by looking at the transit time near source region in the n channel, the transit time at a particular region (X = 80 to 130 nm), where the notches are introduced are also observed. This modulated region transit time is denoted as τ^*. Surprisingly, the MCW-GFET showed $\tau^*$of 0.23 ps, while the conventional GFET possessed $\tau^*$of 0.5 ps, which simply indicates that the modulated region transit time had shortened by 54%, more than half in the MCW-GFET. The device with W= 0.3, on the other hand, showed a similar increase in velocity of up to 42% near the source region. The local mean velocity increased from 1.67×10^5 to 2.86×10^5 m/s. In such device, τ^*shortened by 36% from 0.5 to 0.32 ps.

On the other hand, in the case of monolayer graphene, the maximum increase in the mean velocity (W=0.1) was observed 8 nm from the source edge inside the channel region where X = 92 nm. The mean velocity increases up to 64%, from 8.58×10^4 to 2.39×10^5 m/s. The transit time is however only shortened by 13% from 0.15 to 0.13ps. τ^*on the other hand shortened by 30% from 0.14 to 0.1 ps. Device with W= 0.3 showed 8% faster transit time and 9% faster modulated region transit time.

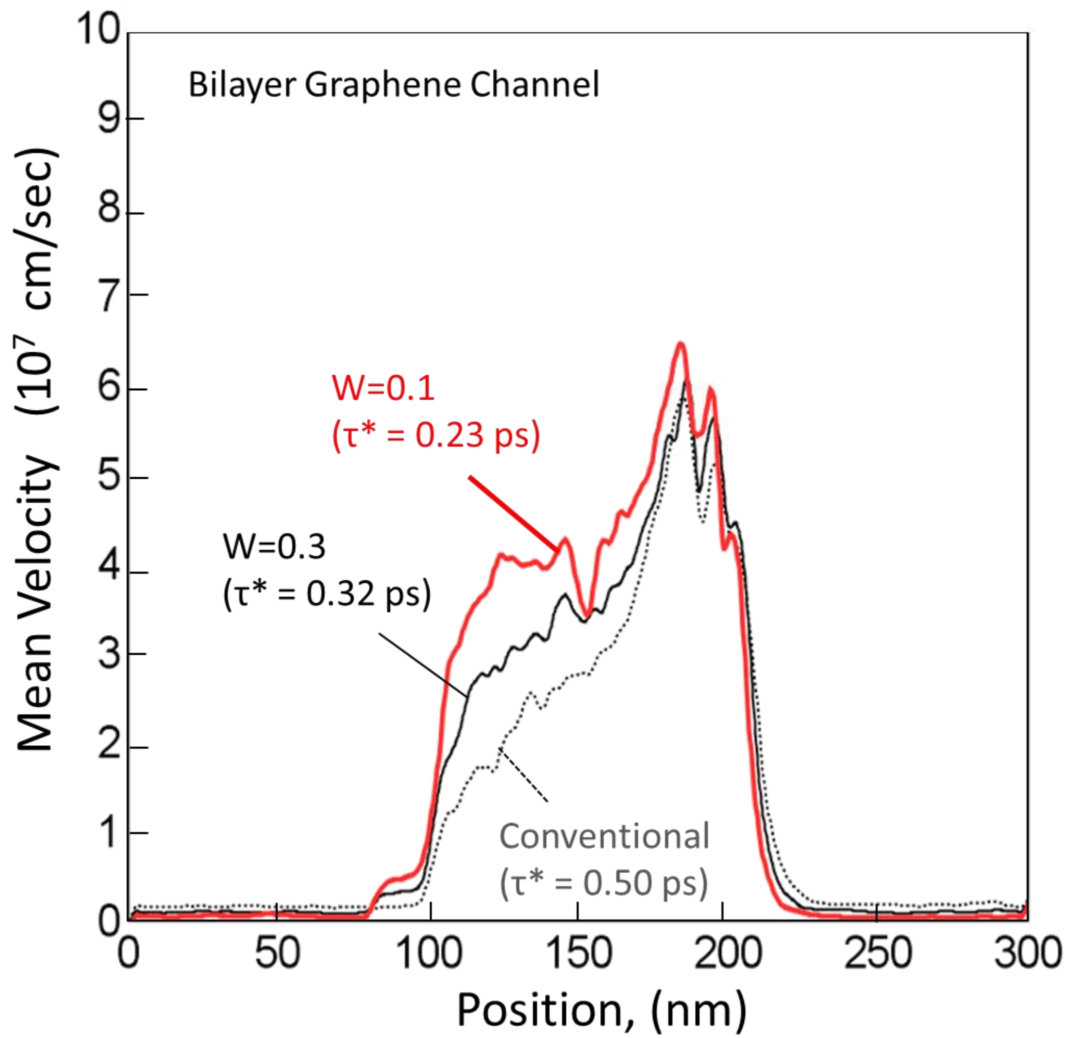


Fig. 28: Mean carrier velocity in MCW-GFET with bilayer graphene channel. Modulated region transit time, τ^* is the transit time at the source side of the channel.

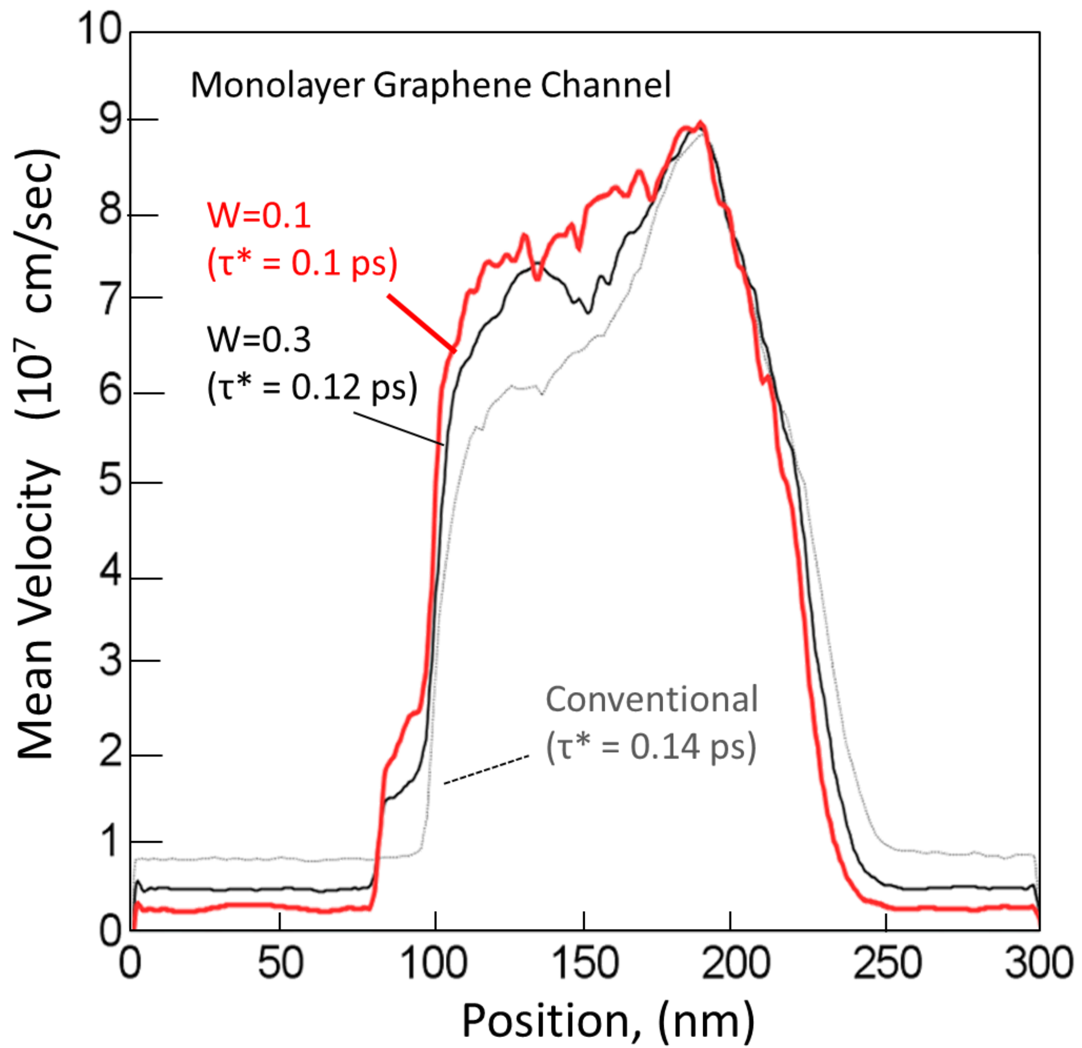


Fig. 29: Mean carrier velocity in MCW-GFET with monolayer graphene channel. Modulated region transit time, τ^* is the transit time at the source side of the channel.

3.5.3 MCW Effect in Monolayer and Bilayer Graphene Channel

It has been shown that the MCW structure introduce a sharp electric field increase at the source side at the channel and the enhancement of the high speed property which is translate as a faster transit time inside both monolayer and bilayer graphene channel. Although faster transit time can be found in both MCW-GFET with monolayer and bilayer graphene channel, it can be seen from the results that the MCW effect is more significant in MCW-GFET with a bilayer graphene channel. Although the mechanism of the MCW effect will later be discussed in chapter 4, here the why there is a more significant enhancement in terms of carrier velocity of MCW-GFET with a bilayer channel over of a monolayer graphene channel is discussed.

It is suggested that this different effect of the MCW structure correlates with the nature of the bandstructure inside bilayer and monolayer graphene. It is clear that stronger electric field shift the carrier distribution to higher energy region, which is shown in carrier mean energy profile of Fig. 30 and Fig. 31. In the region where the notches were placed (X= 100-150 nm), the energy significantly increased in MCW-GFETs. The highest increased was at X= 132 nm where the mean energy doubled from 0.0273 to 0.0576 eV.

The nature of the E-k dispersion in bilayer graphene is parabolic while is linear in monolayer graphene such that the maximum velocity calculated from the slope of the dispersion does not change in monolayer graphene even in higher energy regions. This maximum velocity does change in bilayer graphene because of the parabolic dipersion. Therefore, shift of the carrier distribution to higher energy region is more significant in contributing to the velocity enhancement in the case of bilayer graphene channel.

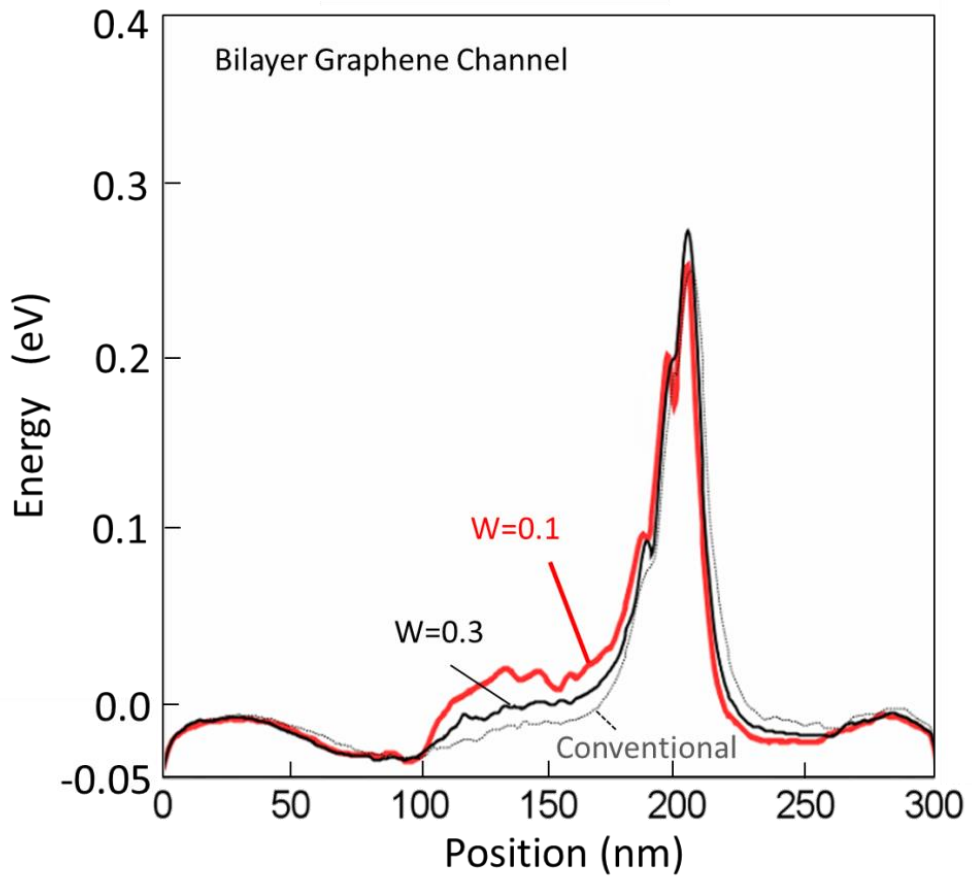


Fig. 30: Energy profile in MCW-GFET with bilayer graphene channel

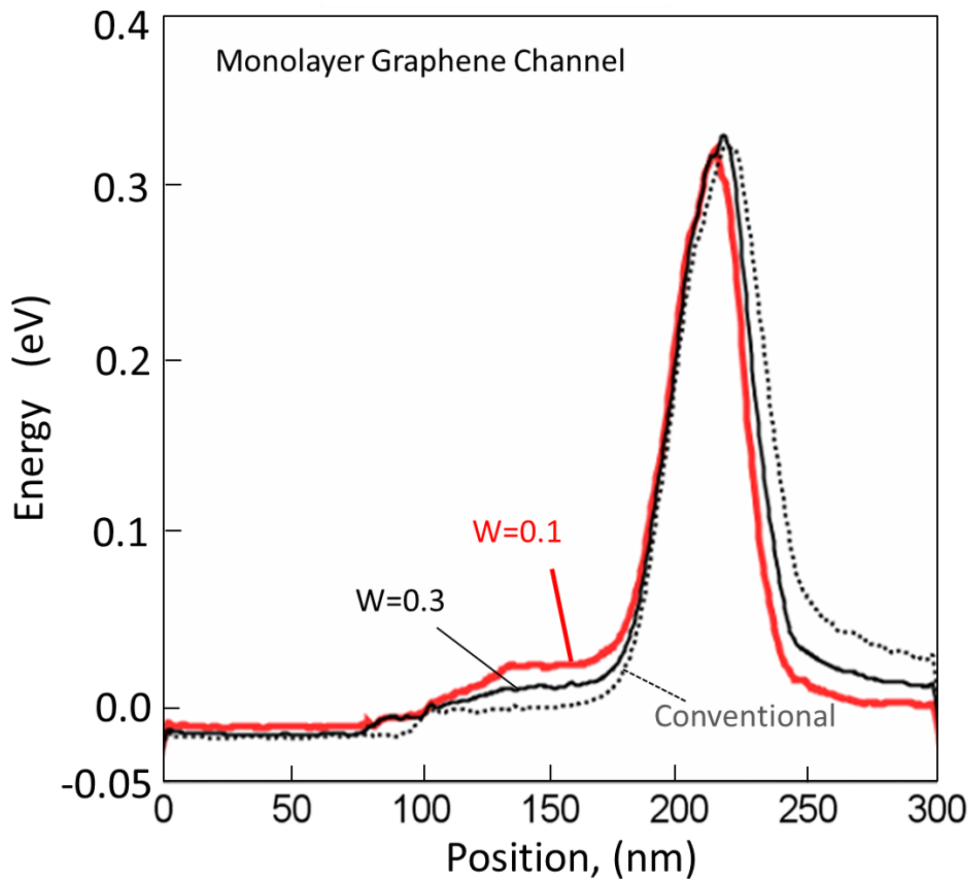


Fig. 31: Energy profile in MCW-GFET with monolayer graphene channel

3.6 Conclusion of Chapter 3

In conclusion, the feasibility of a new MCW-GFET with its channel width being locally modulated is being demonstrated. With dimension optimization, a 54% faster modulated region transit time was achieved in such device. It has been found that local modulation of the channel width introduces a high acceleration electric field near the notch structure but will not change the threshold voltage Vth of the FET. The nature of the parabolic band dispersion in bilayer graphene makes the MCW effect more significant is such compared to a monolayer graphene. These findings open a new dimension for fabricating high-speed high-frequency transistors with structural design.

Chapter 4: Bandgap Opening in Modulated Channel Width (MCW) GFET

4.1 Introduction of Chapter 4

It was demonstrated in the previous chapter that such local modulation of the channel width at the source side of the channel enhanced the high frequency& high-speed performance with almost no changing the threshold voltage of the transistor. In this chapter, the MCW structure is extended to not only enhance the high speed property of carriers but to open a bandgap inside the graphene channel. The electrical and transport properties of MCW-GFET, where a GNR array is created at the modulation area as shown in Fig. 32 is explored. The feasibility of this structure in terms of high speed carrier transport and bandgap creation in the channel is investigated for the first time, by using a semi classical Monte Carlo particle method for simulating electron transport combined with an ab-initio method for calculating band structures of GNR. The bandstructure of GNR array structure is evaluate focusing on two important values which are the bandgap and the slope of the energy dispersion. These two values are crucial to determine the performance of the device in terms of the high-speed performance which is influenced by the slope and switching characteristic which is determined by the value of the bandgap.

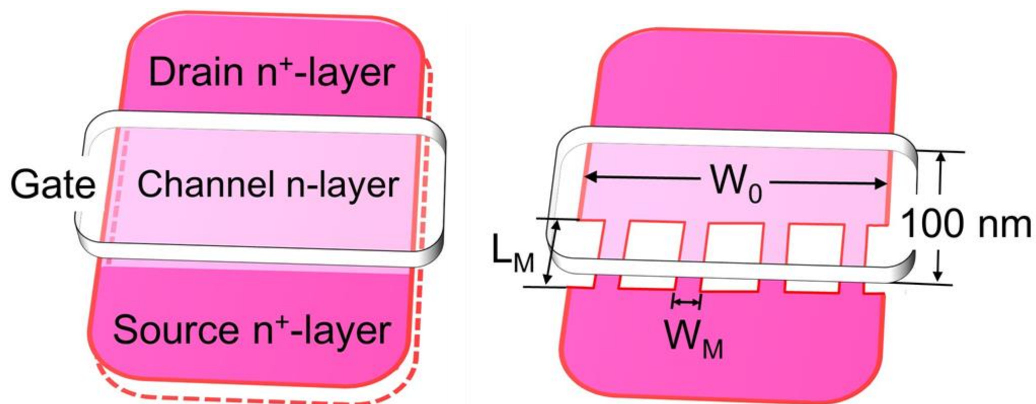


Fig. 32: GNR array introduced in the modulated region of the graphene channel

4.2 Graphene Nanoribbon (GNR)

It has been known that quantum confinement in thin graphene ribbon or more well-known as graphene nanoribbon (GNR) creates a bandgap in graphene channel [104, 105]. The bandgap opening can be controlled by tuning the width and edge state of the GNR [106, 107]. The edge state of the GNR in particular is very sensitive to the bandgap opening. An armchair or a zig-zag edge is reported to sensitively determine whether the GNR will be semiconducting or metallic [108, 109, 110]. In addition, the nature of the bandgap is reported to be inversely proportional with the GNR width [28]. To yield a significant bandgap of >100 meV, a GNR with a width of <10 nm should be considered. The problem with GNR device as a solution to a GFET with no bandgap is the fact that GNR-FET exhibits a low carrier velocity and a low driving current as discuss briefly earlier in the first chapter.

4.3 Bandgap Calculation (10 nm GNR, Bilayer Graphene)

Since calculation is performed while considering periodicity in Y-direction, the band structure of GNR stripes is assumed to be similar to a single stripe of 10 nm-wide nanoribbon calculated using the unit cell in Fig. 33. The GNR arm-chair edges are terminated by hydrogen atoms while Fig. 34 shows the structure of bilayer graphene channel that is also being calculated with a perpendicular electric field applied in order to open a bandgap. The geometry in both cases of GNR and Bilayer Graphene is optimized until the force tolerance is 0.01 meV/A. The Monkhorst-Pack grid k point sampling is set to be $1\times16\times16$ in GNR and $11\times11\times1$ in Bilayer Graphene. The most general exchange correlation, Local Density Approximation (LDA) is used in this calculation.

The bandstructures of both GNR and bilayer graphene with a perpendicular electric field are shown in Fig. 35 and Fig. 36 respectively. A 100 meV bandgap openings is obtained in the GNR structure and this agree well previous works [111]. In order to compare the performance of devices with the same bandgap opening, the perpendicularly applied electric field of bilayer graphene channel is controlled and tuned to achieve a 100 meV bandgap. It is found that a 1.2 V/nm electric field yield a 100 nm in such case and agree considerably well with past literature [112].

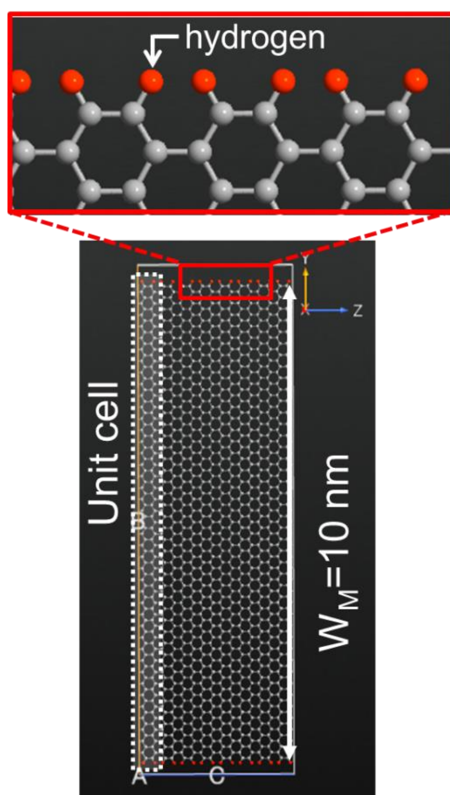


Fig. 33: Unit cell of GNR

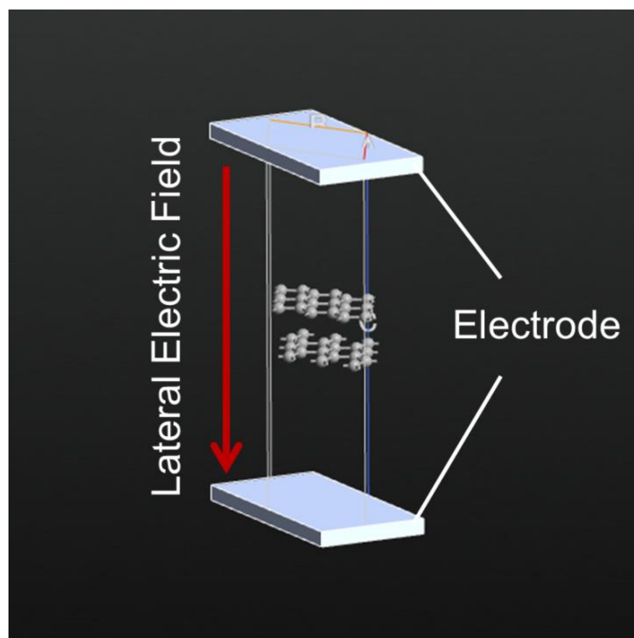


Fig. 34: Unit cell of Bilayer Graphene with a perpendicular electric field being applied

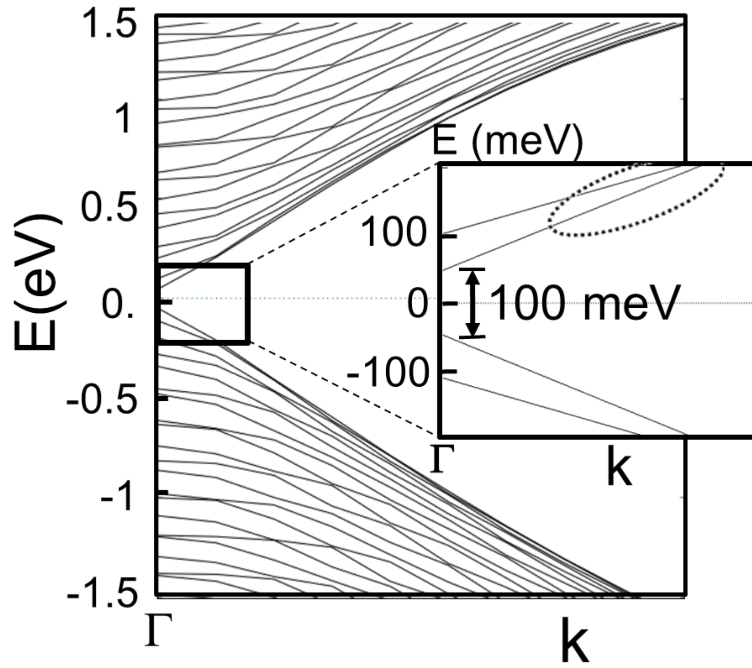


Fig. 35: Bandstructure of a 10 nm GNR

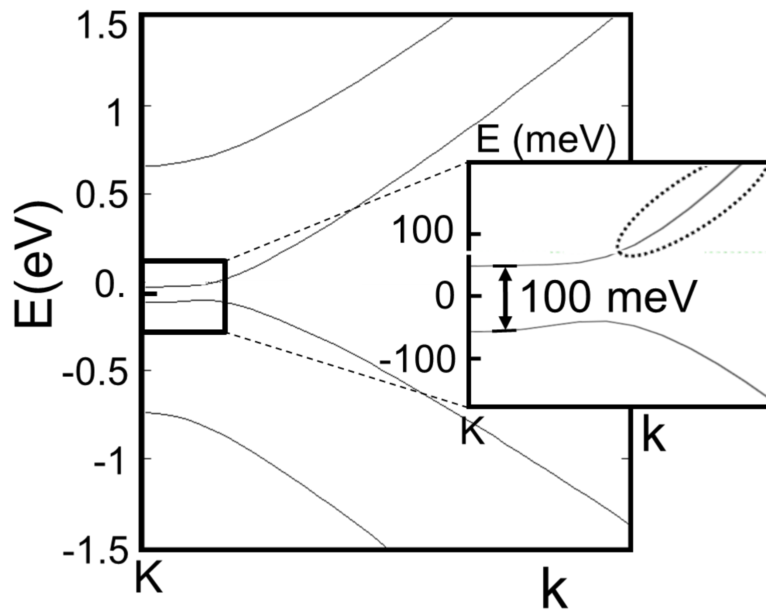


Fig. 36: Bandstructure of a Bilayer Graphene with a 1.2 V/nm electric field being applied perpendicularly

4.4 Result and Discussion

4.4.1 Mean Velocity Profile (MCW-GFET, Bilayer GFET, GNR FET)

Using the bandstructure that is calculated using DFT, the transport properties of a few different kinds of GFETs are simulated. These devices are shown in Fig. 37. Fig. 38 shows carrier mean velocity profiles in MCW-GFET (W_M=10 nm, W=0.3), GNR-FET and Bilayer GFET. All these devices have an equivalent bandgap of about 100 meV inside the channel. The carrier mean velocity profile under a conventional GFET channel is also shown for reference. The source-to-drain voltage V_{ds} and the gate-to-source voltage V_{gs} were 0.5 V and 0 V, respectively. Since V_{DS} is of a low value of 0.5V, no temperature dependency is being considered when estimating the transport properties in this calculation. The edge of the 10 nm GNR array inside the modulated region calculated here is considered perfectly smooth with GNR having a perfect armchair edge without any defects. It has been calculated elsewhere where it is found that the mobility in GNRs which is parasitically affected by edge roughness scattering did not decrease rapidly in GNRs with a fewer defect perfect edge [113]. As shown in this Fig. 38, the MCW-GFET shows a significantly higher mean velocity over its two counterparts even while having the same value of bandgap opening. The width ratio, W of the MCW-GFET that is demonstrated in this velocity profile is 0.33. It is worth noting that there is a rapid increase of carrier velocity at the source side of the channel, which is due to the high acceleration field at that place by the MCW effect. This high acceleration field also contributes to the increase in velocity even after the carrier exits the modulation area as you can see in Fig. 38.

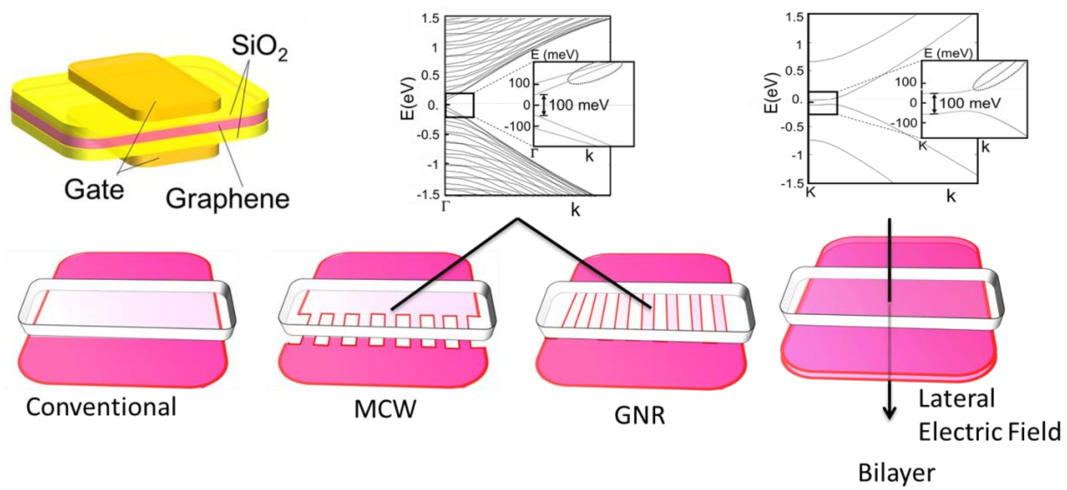


Fig. 37: Transport characteristic of 4 Different devices is being estimated which each devices having a bandgap of 100 meV except for in Conventional GFET

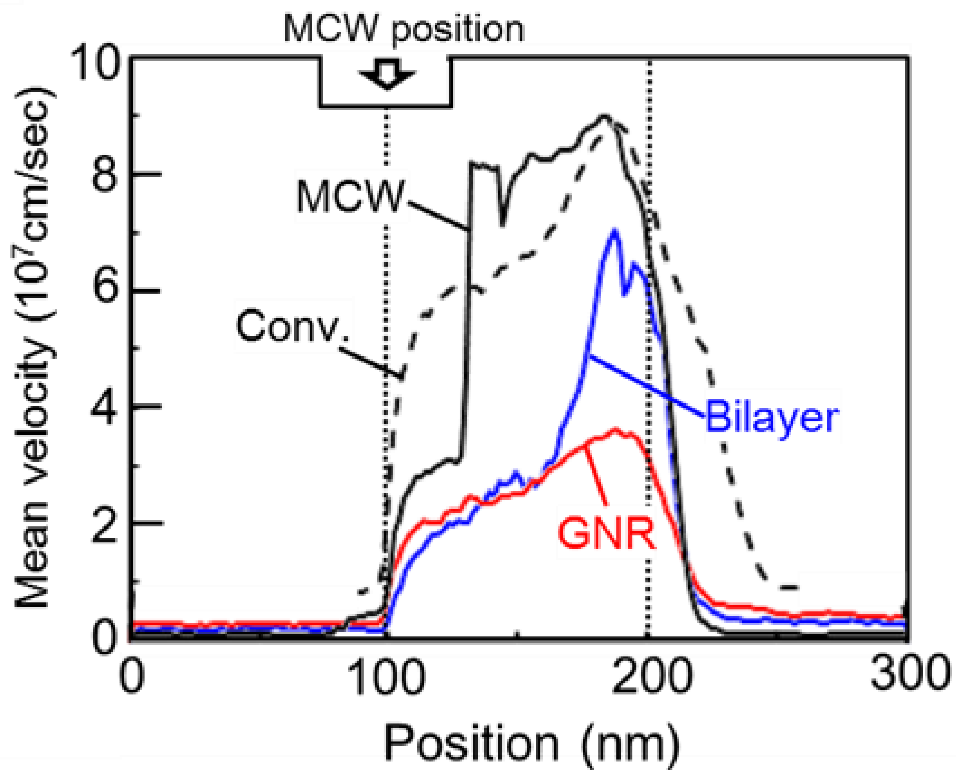


Fig. 38: Velocity profile in MCW, Bilayer, GNR, and Conventional GFET

4.4.2 MCW Effect inside the Device Channel

To discuss this, firstly, note that the velocity of the carrier in this device is given by V_x and V_y velocity component. V_x is parallel to the electric field. From the spatial velocity distribution in Fig. 39, it shows that the V_x and V_y are broadly distributed inside the channel. In the case of conventional GFET, once the carrier is injected into the channel, the electric field gradually align velocity component into the x-direction resulting gradual increase of the mean velocity until it reaches the maximum velocity peak. This alignment of the velocity component is indicated by narrower distribution of the carrier. In the case of MCW-GFET, high acceleration field instantly align the velocity into the x-direction rapidly increasing the mean velocity until it reach the maximum velocity peak as shown in the spatial distribution of a conventional GFET. This alignment of the velocity at x-direction is kept after the carrier exits the modulation area.

Since the bandstructure is of a 10 nm GNR in the modulation area and of a graphene in the rest of the channel, higher maximum velocity due to the linear dispersion graphene bandstructure rapidly increase the velocity of the carrier exiting from the modulation area. Smaller carrier density after exiting the modulation area is due to the fact that current is kept constant throughout the channel. Thus, this narrow distribution of the carrier at high velocity region is represented by the sharp increase of the mean velocity as shown in the mean velocity profile of MCW-GFET.

If you compare the GNR with the Bilayer GFET, the carrier accelerations at the source side of channel are similar to each other. However, there is a marked contrast between the two profiles at the drain side, which can be attributable to a difference in group velocity at higher energy. This is evident when comparing the gradient of the E-k dispersion of Bilayer graphene and GNR shown in Fig. 35, 36. At lower energy region, the gradients are similar but the E-k dispersion is sharper at higher energy region in the case of bilayer graphene. When calculating velocity from the E-k dispersion, it is found out that velocity inside GNR maintains in the range of 3.55×10^7 cm/s ~ 4.34×10^7 cm/s while in Bilayer graphene velocity is lowest at 7.05×10^6 cm/s in lower energy region and highest at 8.05×10^7 cm/s in high energy region respectively.

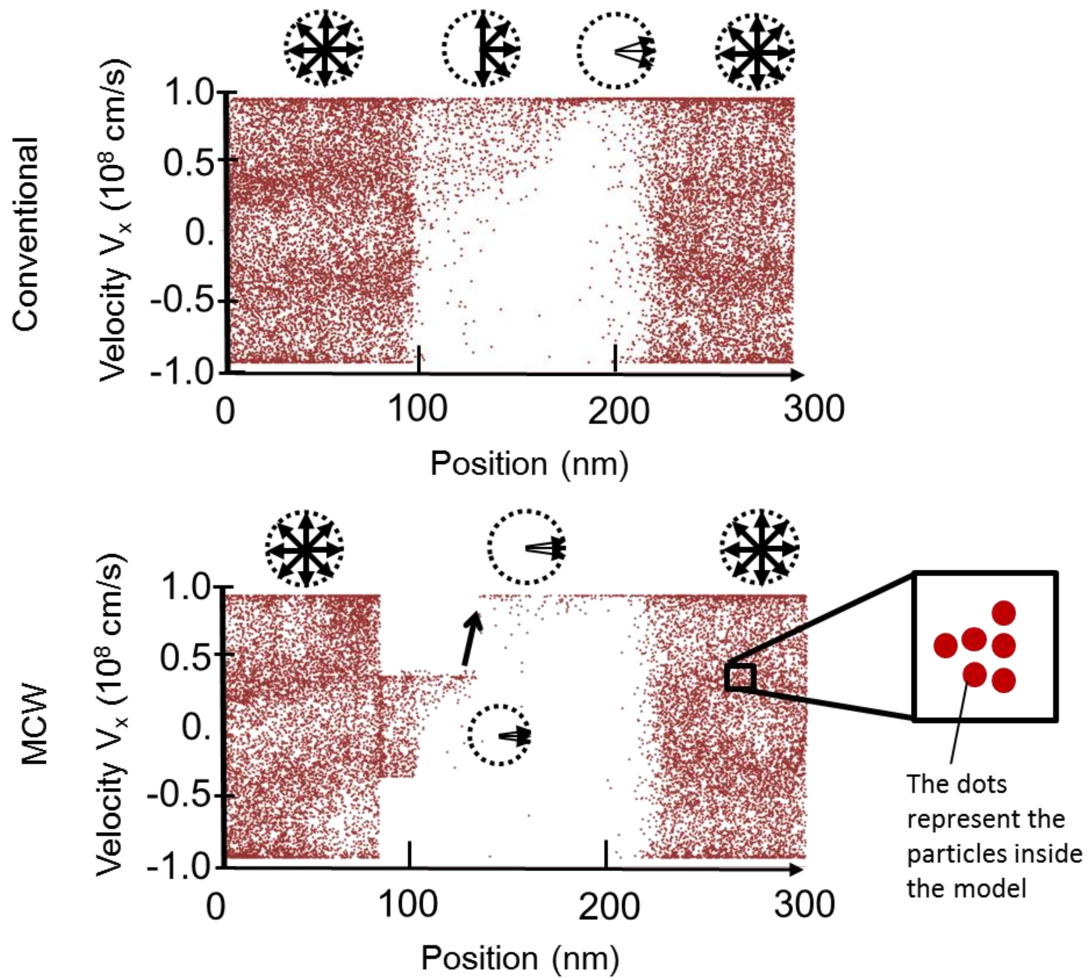


Fig. 39: Spatial distribution of the velocity of the carrier inside the devices. The dots represent carriers inside the device. The circle and the arrow illustrate the velocity vector inside the channel.

The schematic of the band structure and the working principle in Conventional GFET, MCW-GFET and GNR FET is illustrated in Fig. 40. Please note that the source-channel-gate is n+-n-n+. Although the potential in this illustration may be steeper than in the simulated device, this figure is simplified for better understanding. In conventional GFET, since there is no bandgap, the flow of the carriers from the source into the channel cannot be entirely suppressed. On the other hand, in MCW-GFET, the introduction of the bandgap partly inside the channel enable the flow of the carriers injected into the channel at off state be suppressed while high electric field at the modulated region enables acceleration of the carrier velocity injected into the channel at

on state. Although the off-state current is similarly suppressed in GNR FET, carrier acceleration cannot be achieved in GNR FET as illustrate in the figure. This is evident when observing Fig. 38 where there is no velocity enhancement in GNR FET.

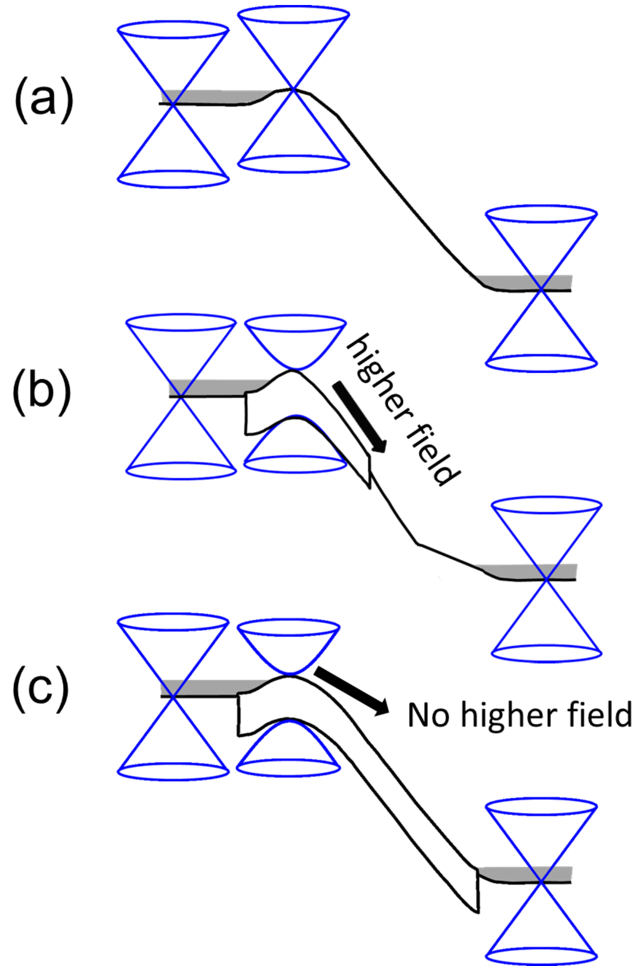


Fig. 40: Schematics of band structures and working principles of (a) conventional GFET (b) MCW-GFET (c) GNR-FET. The arrow represents the electric field at the source side of the graphene channel.

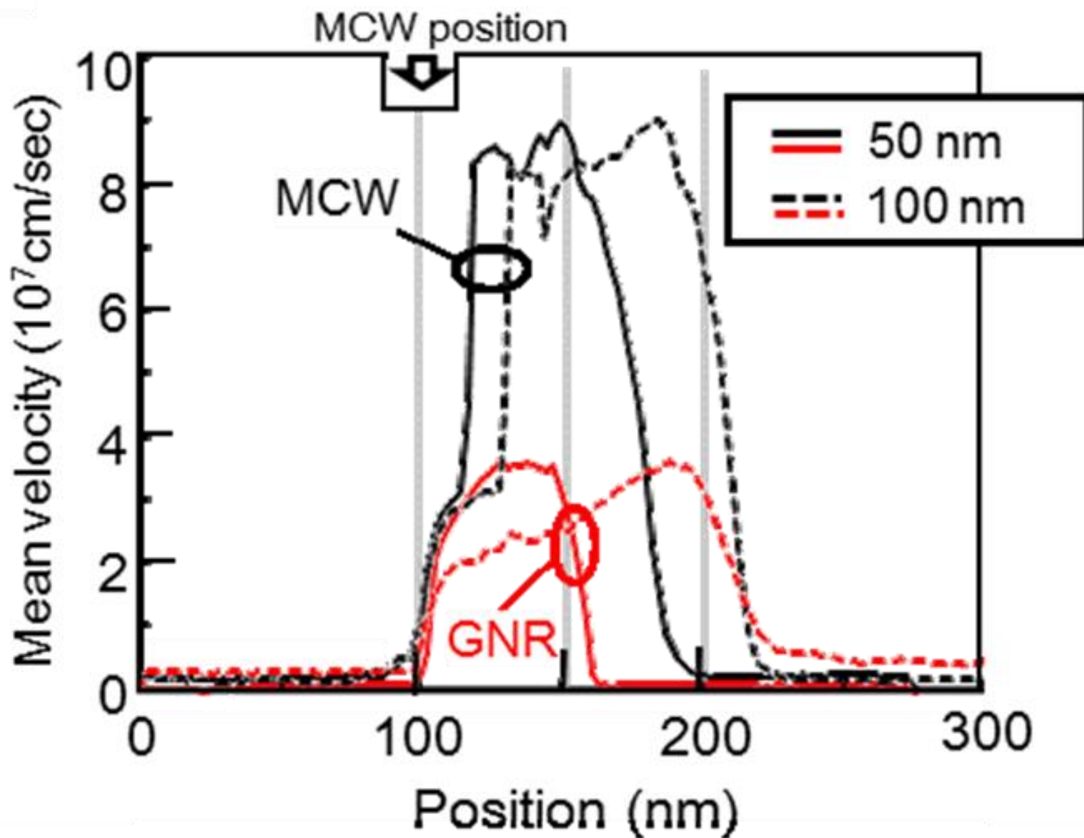


Fig. 41: Profiles of average lateral components of carrier velocity (v_x) of modulation channel width graphene FETs (MCW-GFETs) and parallel graphene nanoribbon FETs (GNR-FETs) with 50-nm and 100-nm channels

When scaling down the FETs by shrinking the channel length to 50 nm, more carriers travel ballistically in the channel. Subsequently, the mean velocity profile of the GNR-FET increases more rapidly and tends to saturate in the channel, as shown in Fig. 41. The mean velocity profile shows significantly higher mean velocity in the MCW-GFET.

Fig. 42 shows the intrinsic transit time τ_d as a function of channel length for graphene FETs. Experimental extrinsic values of τ_d for InP-based high electron mobility transistors (HEMTs) [114, 115, 116, 117, 118, 119] are also plotted for comparison. All of the graphene FETs simulated here exhibit shorter transit times comparing to InP HEMTs having the same channel length. In particular, the transit time in 100 nm-

MCW-GFET reaches 0.15 ps, which is 60% shorter than of the GNR-FET and 49% shorter than that of the Bilayer-GFET. This implies that MCW-GFET is a better candidate in terms of faster transit time while having a bandgap opening of the same value if compared to a GNR-FET and Bilayer GFET with a perpendicular electric field. When scaling down the GFETs by shrinking the channel length to 50 nm and the modulation length to 24 nm, the velocity enhancement effects in the device remains. The 50 nm-MCW-GFET shows a 59% faster transit time of 0.08 ps compared to 0.17 ps of GNR-FET. Comparing devices with a minimum size feature of approximately 20 nm, our 50 nm channel with a 24 nm modulation length MCW-GFET is superior with a 3 times faster transit time to of InP HEMT with a 20 nm channel length and a transit time of 0.24 ps.

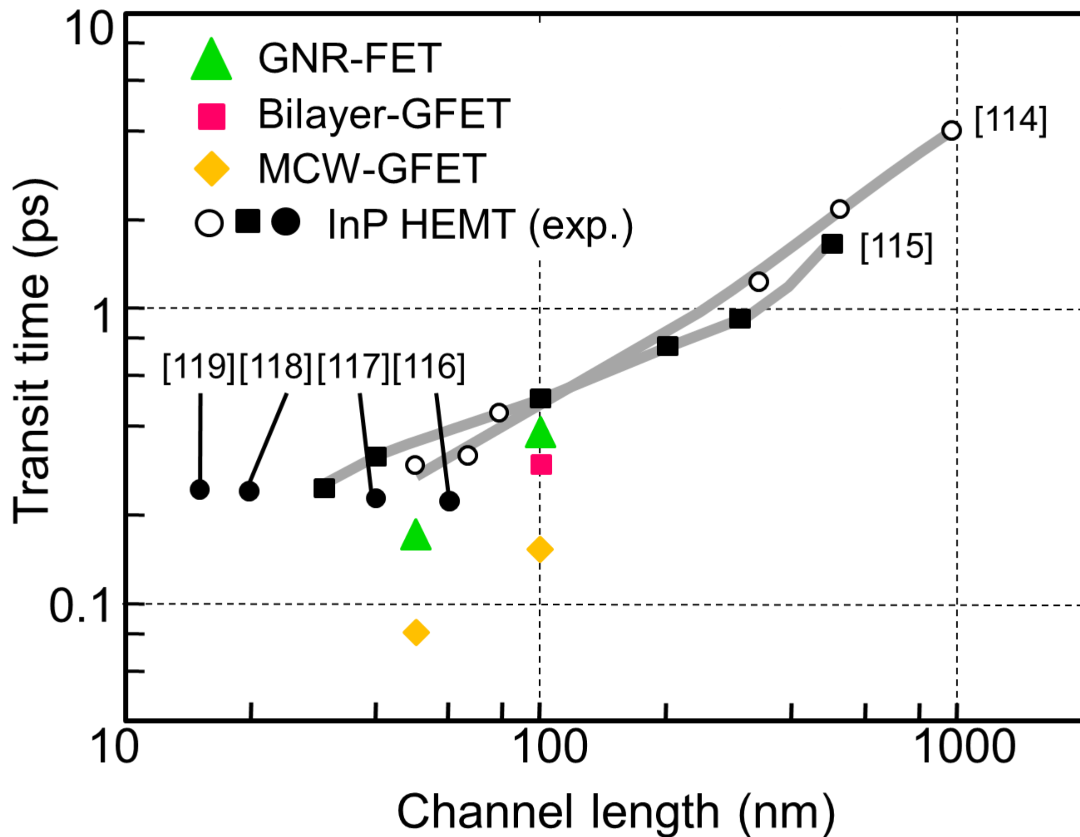


Fig. 42: Transit time of devices calculated in this work compared with previous work on InP HEMT (experimental)

4.5 Conclusion of Chapter 4

In conclusion, GFET structure with a channel width locally modulated in order to introduce a high acceleration electric field and bandgap in the modulated region is propesed. Even though the bandgap creation leads to a smaller carrier group velocity, the electric field modulation makes the transit time in MCW-GFET comparable to conventional GFETs and significantly shorter than those of reported InP-based HEMTs. Comparing with InP-based HEMTs, a carrier transit time that is about one third shorter is obtained for a 100 nm-channel (gate) MCW-GFET. These findings open a new dimension for fabricating GFETs with a bandgap without compromising the high speed performance.

Chapter 5: Stability of Intercalated GNR

5.1 Introduction of Chapter 5

Although much research has been carried out into graphene intercalation, little is known about a stable and suitable intercalation compound to be used in GNRs for LSI interconnects since the development is still at the early stage. On the other hand, one of the most critical issues that had been discussed in graphite intercalation is the stability of the intercalation structure. Stability of different intercalation compound was investigated to find the most stable candidate. In this chapter, both Molecular Dynamics and First Princple Theory calculations are used to estimate on the stability of an intercalated GNR structure while investigating a highly stable intercalation compound. There is no previous report on how an intercalation is affected by the width of the graphene host since intercalation is usually done on a graphite host or on a wide graphene wire. Since the stability of a readily intercalated structure is being simulated, the staging phenomenon inside the simulated intercalated structure need to be considered. Staging or stage number is defined by the number of graphene layers in between of intercalated layer. For example in Fig. 43, the stage number is 2 since there are 2 layers of graphene between the layers that intercalated layer. The stage number depends on the intercalation compound and the intercalation ratio (intercalation compound %)

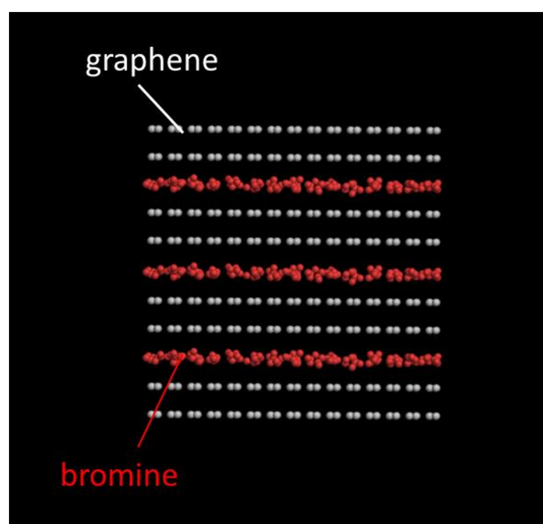


Fig. 43: Staging phenomenon in graphene intercalated with bromine.The same model is used with fewer number of Br and graphene layers

5.2 DFT Simulation Model (GNR width N=10, N=20, Br 3%, 9%)

The binding energy of a graphene host before and after intercalation is calculated as it directly translates the stability of the structure. Since it is very computational costly to calculate very large model, the binding energy of bilayer GNR is calculated. The width is express by the term N, which accounts to the number of atoms at the edge of the GNR. GNR with a width of N= 10 (~ 1 nm) and N=20 (~2 nm) are considered. The unit cell that is being calculated is shown in Fig. 42. Energy optimization is done until the force tolerance is 0.01 eV/A. The Monkhorst-Pack grid k is set to 1×1×34 as the unit cell is periodic only in the Z direction. The simulation is started by calculating the binding energy of N=10, N=20 width bilayer GNR. The binding energy that we get for N=10 and N=20 without any intercalation are 87 meV/carbon atom, C and 86 meV/C respectively. Due to the lack of other literature on the calculation of binding energy of bilayer GNR, this result cannot be compared to find any agreement in other works. However, since the most important aspect of this investigation is to find any change in the binding energy of bilayer GNR before and after intercalation, the value is relevant as an approximation.

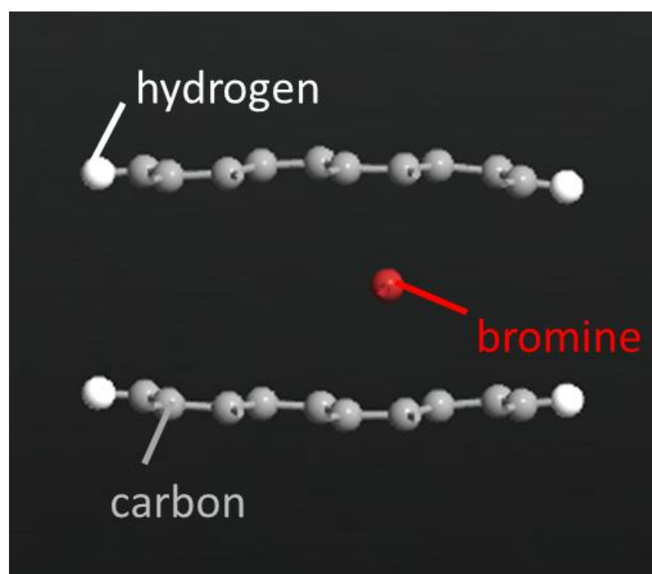


Fig. 44: Simulated model of a single bromine (red) in bilayer GNR (3 nm width)

When intercalating the bilayer GNR with 3% of Br, the binding energy of the intercalated bilayer GNR decrease to 45 meV/C in N=20 and 29meV/C in N=10. These

results suggest that there is a GNR hosts width dependence to the intercalation affect where binding energy between carbon layers in GNR change differently in GNR with different width even though when intercalated with the same intercalation ratio.

Using the same unit cell as in Fig. 44 and the same parameter, the binding energy of a bilayer GNR with a width of N=10 and being intercalated with Br of 9% are calculated. It is found out that the binding energy increase with increasing intercalation ratio of Br. The binding energy increases from 29 meV/C in intercalation ratio of 3% to 83 meV/C in the case of 9% Br. This suggests that the intercalation compound, which Br in this case plays an important role in contributing to the binding energy between carbon layers. It is also being reported elsewhere by previous ab initio theoretical works where the found out that intercalation of the interlayer space between a single layer graphene and a substrate is more stable in higher intercalation ratio with a higher binding energy[120].

Charge transfer between Br atoms and bilayer GNR host is also being calculated. This is done by calculating the density of state (DOS) of GNR host before and after intercalation of GNR structure. From the DOS profile, the Fermi level shift is calculated. In the case where bilayer GNR with a width of N=10 and Br intercalation ratio of 9%, it is found that the Fermi level shift by 0.18 eV. This shows that the charge transfer of one bromine atom is 0.06 eV/atom. Therefore, to achieve a fermi level shift of 1 eV [71] where.the reduction of the resistivity in GNR interconnects is substantial, a GNR host with 50% intercalation ratio of Br is needed.

5.3 MD Simulation Model (GNR width 3nm, 10 nm, Br 15%, 30%)

Molecular dynamics calculation was done using Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPS) simulation package from Sandia National Laboratories [121] to study the interaction between multilayer graphene and intercalation compound in order investigate the stability of the intercalation structure. The MD system features a 4 layers graphene sheet intercalated with bromine (Br) atoms as shown in Fig. 45. Note that bromine is placed between the second and third layer of graphene from above. This is due to the staging phenomenon inside the intercalation structure as discussed in the introduction section and this is a stage 2 intercalation structure which is usually found in bromine intercalated graphite. Interaction between carbon atoms in graphene is modeled using Tersoff potential [122] with Van der Waals being additionally modeled using LJ potential with parameters from previous literature [123]. Br-Br and Br-Carbon I interaction are modeled using the LJ potential and Morse Potential with parameters derived from [124] and [125] respectively. A cutoff of 10 A is imposed on the LJ and Morse interactions. 2 sets of simulation are performed. In the first case, the stability of the intercalation structure is studied in dependence of graphene width (3 nm, 10 nm) while maintaining the atomic percentage (atomic %) of Br at 15%. In the second case, the width of the GNR host is constant (3 nm) while changing the intercalation ratio of the intercalation compound of 15% and 30% to find if there is a optimum intercalation ratio that can stabilize the whole intercalated structure.

Following energy minimization, 0.1 ns simulation are run at 300 K and maintained at 1 atm pressure. The stability of the structure is observed by evaluating the displacement of graphene layers before and after the intercalation. The position of the intercalation compound is also evaluated to determine if the interlayer space in graphene can contain the intercalation compound or not.

In the first case where 10 nm width and 3 nm width GNR are intercalated with the same intercalation ratio of Br, 10 nm GNR is stable while the structure in 3 nm width intercalated GNR deteroriate showing instability in such case. This can be seen from series of post simulation structure by timestep in Fig. 45 where the intercalated structure started to crumble at time = 9 ps. In the stable structure shown in Fig. 46, the interlayer distance of the intercalated region is found to be 0.67 nm which agrees with

experimental findings[126].This result suggests that there is a width dependency between the stability of an intercalation structure and the width of its graphene host. This stability analysis also suggests that a the stability of an intercalated structure is different in GNR host with different width.

In the second case where 3 nm width GNR is intercalated with 30% of Br, the intercalated structure suprisingly stabilized as shown in Fig. 47. When comparing the Fig. 45 and Fig. 47 at time frame 5 ps, it can be seen that in the case of 15% Br graphene structure started to crumble at the middle part of the structure where Br is either absent or only a few. On the other hand, in the case with 30% Br, the intercalated Br form a 2D layer that in return holds the graphene layers together. It can be suggested that Br can also contribute to binds the two layers of graphene together and there is an optimum percentage of Br to form a stable intercalation structure.

(i) GNR width 3nm, Br 15%

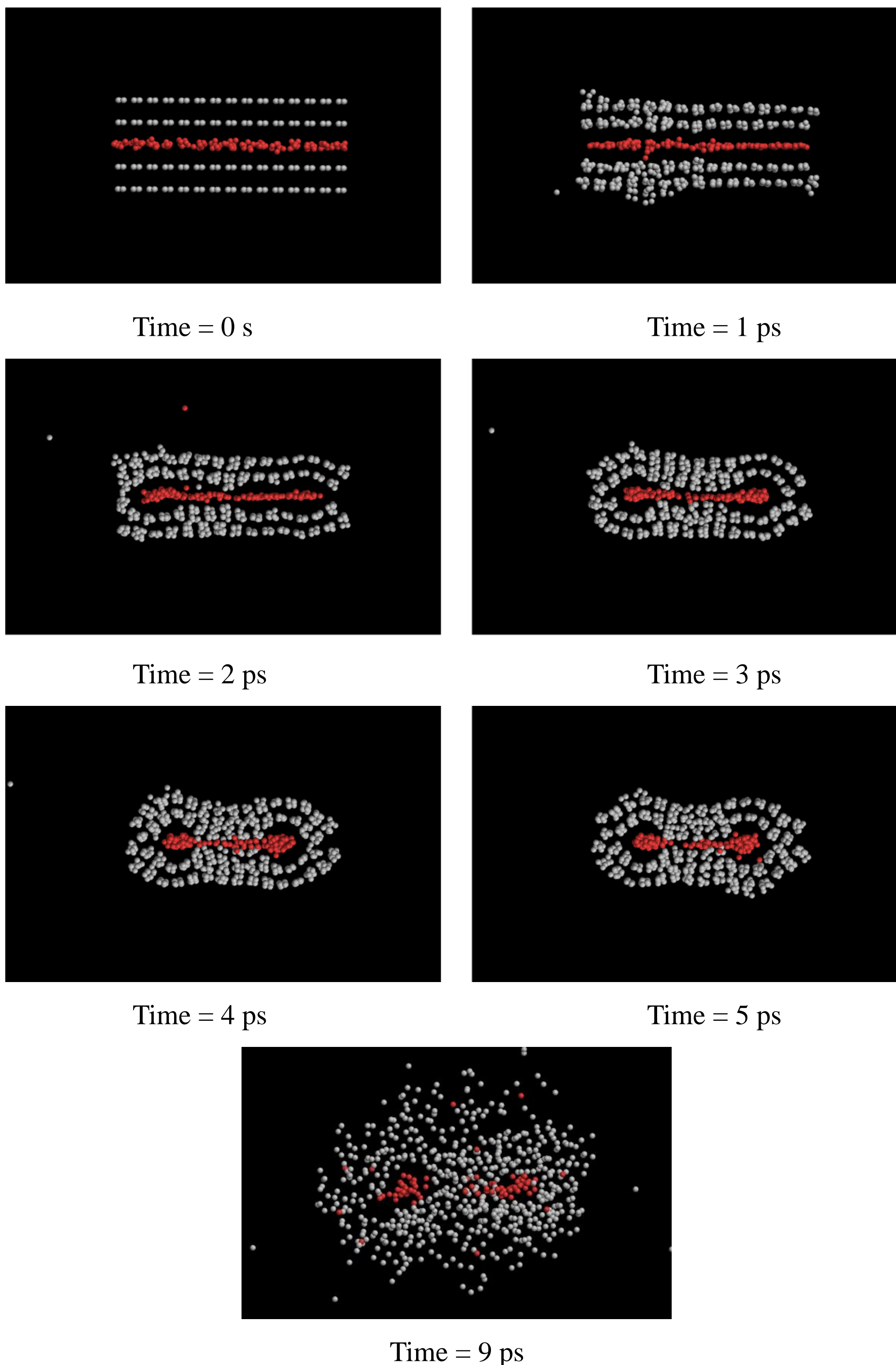


Fig. 45: Post simulation structure of 3 nm width GNR with 15% Br intercalation

(ii) GNR width 10 nm, Br 15%

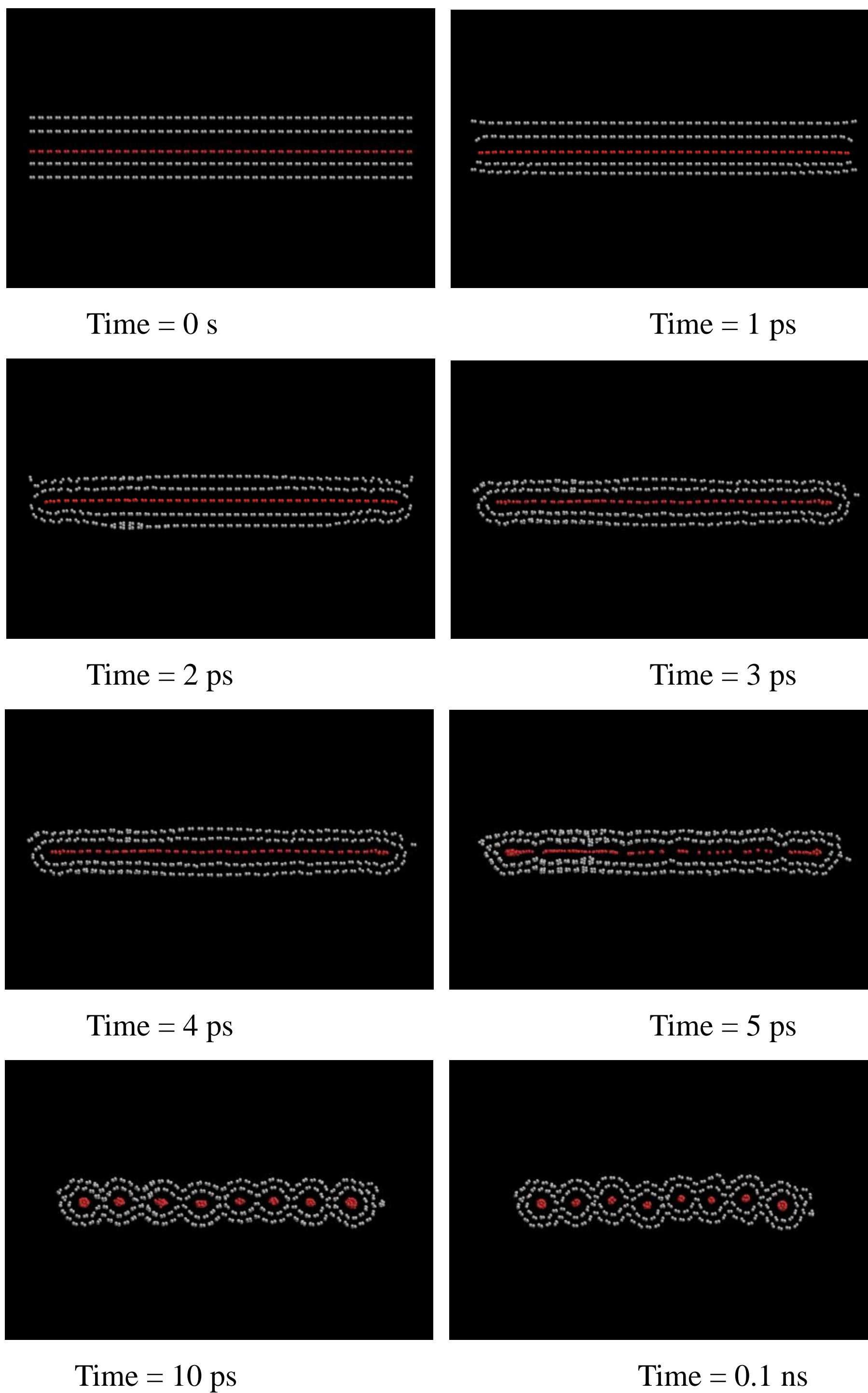


Fig. 46: Post simulation structure of 10 nm width GNR with 15% Br intercalation

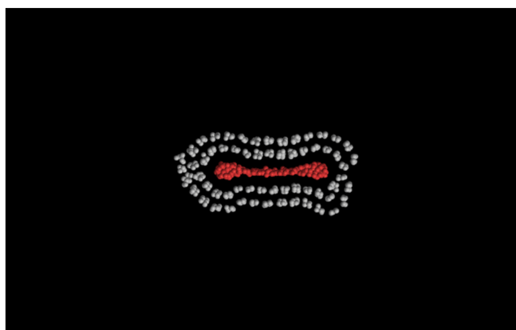
(i) GNR width 3nm, Br 30%

Time = 0 s

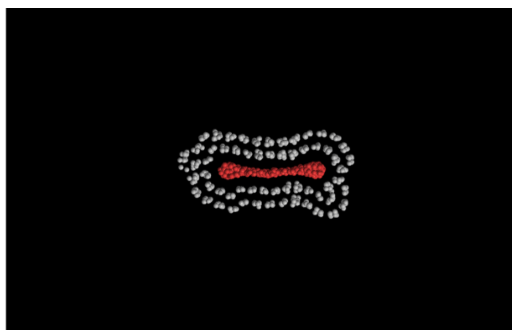
Time = 1 ps

Time = 2 ps

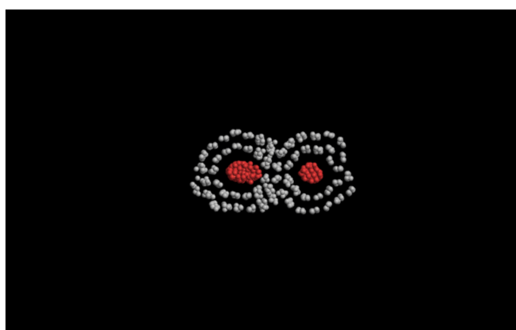
Time = 3 ps



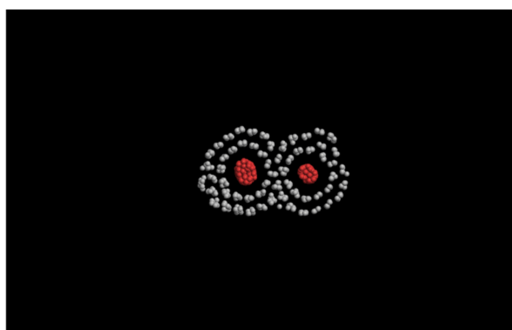
Time = 4 ps



Time = 5 ps



Time = 10 ps



Time = 0.1 ns

Fig. 47: Post simulation structure of 3 nm width GNR with 15% Br intercalation

It is found out that the stable intercalated structures in these MD simulation are similar, showing intercalated compound islands formed inside the graphene host. Since there is no experimental data of a stable intercalated GNR/graphite structure to be compared to these findings, the stable intercalated structure in this MD simulation cannot be evaluated to previous experimental datas. However, in discussing the stability of the intercalated structure in graphite, two well-known models are available which are Daumus-Hêrold model and Rüdorff model. These models are shown in Fig. 48 where stage 1-4 refers to the staging phenomenon in the intercalation structure. Staging phenomenon in intercalation structure depends on the type and quantity of intercalation compound. Experimental results shows that intercalation of bromine varies from stage-2 and stage-3 intercalation structure [71]. When comparing the stable structure in this work to these models, it is found out that the structure is similar to Daumus-Hêrold model in case of stage-2 and stage-3 intercalation. This suggests that the findings in this work agree well with previous intercalation structure model where island of intercalated structure is formed in stage-2 and stage-3 intercalated stucture.

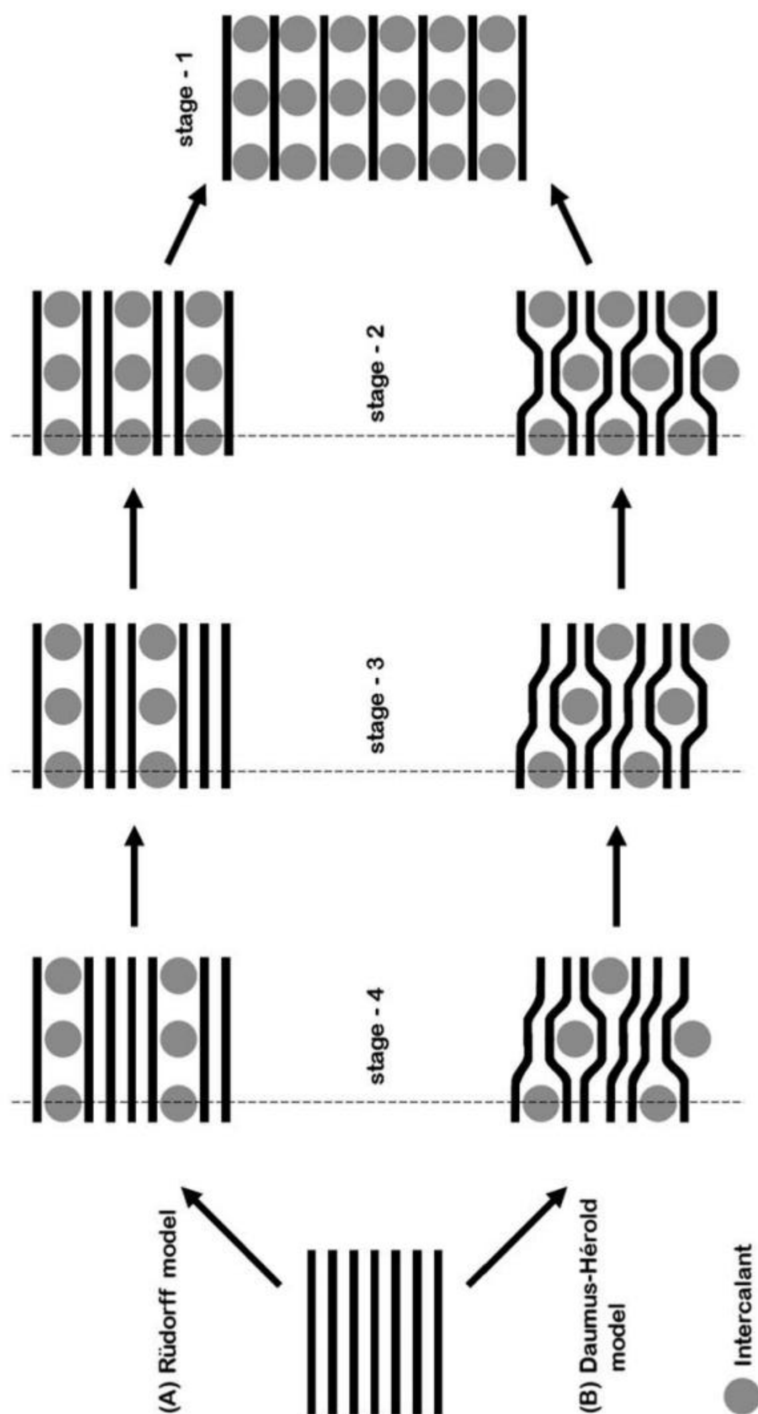


Fig. 48: Intercalated structure models in graphite intercalation. Stage 1-4 depends on the type and quantity of the intercalation compound [127]. Published by The Royal Society of Chemistry (RSC) on behalf of the Centre National de la Recherche Scientifique (CNRS) and the RSC

5.4 Conclusion of Chapter 5

In this chapter, the stability of intercalated GNR with regards to its dependency on the GNR width and the intercalation ratio is investigated. The results are being concluded in Table 5-1 and Table 5-2.

Multilayer Graphene Width	Post MD Simulation Structure		
	Br 15%	Br 30%	No intercalation
3 nm	Not Stable [Fig. 45]	Stable [Fig. 47]	Stable
10 nm	Stable [Fig. 46]	Not simulated	Stable

Table 5-1: Summary of MD simulation

Bilayer Graphene Width	Binding Energy (meV/C)		
	Br 3%	Br 9%	No intercalation
N=10 (~ 1 nm)	29	83	87
N=20 (~ 2 nm)	45	Not simulated	86

Table 5-2: Summary of DFT simulation

From the MD and DFT simulation results, it is found out that there is a dependency between the stability of the intercalated structure and the GNR width. It is also found out from MD and DFT simulation that an optimum % of intercalation compound can help to stabilize the structure by contributing to the binding energy between graphene layers. The calculation results in this chapter are concluded in Fig.49.

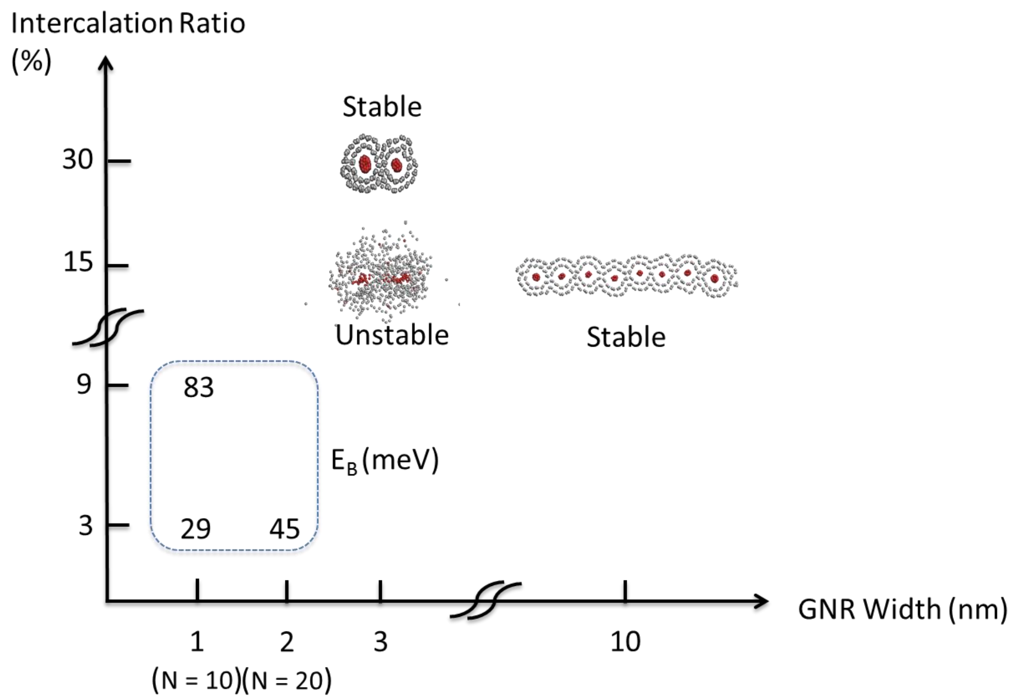


Fig. 49: Stability of calculated intercalation structure in both ab-initio and MD calculation

Chapter 6: Thesis Conclusion

6.1 Thesis contribution

In this research the most critical issue regarding the high-speed performance and zero bandgap in graphene device is being tackled by proposing a new GFET structure that can possibly solve both problems. This device is called a Modulated Channel Width, MCW-GFET. Making use of the overshoot velocity effect of carrier at the source side of the channel by introduction of high electric field in a narrowed width channel, a high speed enhancement is achieved. On the other hand, the readily quantum confinement effect in graphene nanoribbon (GNR) is considered in the design principle to introduce a bandgap opening inside the channel. When estimating the transport properties of the proposed structure, Monte Carlo simulation method is adopted while calculation on the bandstructure of the designated graphene channel is done using First-principle Density Functional Theory calculation. In MCW-GFET without a GNR array, where the channel is simply be narrowed, a high speed enhancement is achieved where the modulated region transit time can shorten to up to 54% without changing the threshold voltage. GFET for high frequency device such as RF applications can benefit from such structure.

In the extended version of MCW-GFET where both bandgap opening and velocity enhancement are enabled, the electric field induced by the modulation makes the transit time in MCW-GFET comparable to conventional GFETs and significantly shorter than those of reported InP-based HEMTs despite lower carrier velocity as a result of the bandgap opening. These estimations is equally important to realize fast GFETs with a bandgap that is suitable for logic circuit applications.

In investigating the stability of intercalated GNR interconnects, it is found out that the GNR width is an important factor in determining the stability of the intercalated structure. Although graphite intercalation works can be used as the guideline in finding the right candidate for a feasible intercalation compound, this findings is equally important as it suggests a totally different perspective in considering and evaluating the stability of an intercalated structure. This theoretical studies show findings that can contribute to the realization of low power and high frequency LSI applications that is very crucial for the next generation electronic advancement.

6.2 Future works

6.2.1 MCW-GFET

Although it is proven theoretically that the high speed performance can be enhanced in this device, fabrication of MCW-GFET and experimental evaluation of its transport properties need to be done to further to understand the feasibility of our theory. One of the main challenges when fabricating MCW-GFET is to reduce the edge disorder or defect along the GNR array. However, it is worth noting that since the lower carrier velocity caused by the edge roughness scattering will be compensated by the high electrical field acceleration, early development of device fabrication even without a perfect edge GNR array will also give a huge impact in terms of its enhanced speed property. To fabricate this device, it is suggested that and advanced etching technology for example the He-ion beam milling discussed in [96] to be used because of its precision and ability to narrowly pattern graphene to sub 10 nm width.

Along with device fabrication, further simulation parameter and approximation need to be optimized and add to provide a better understanding of the transport properties in this device. This includes:

I. Scattering rates which are dependent to temperature and energy since this calculation consider these rates to be independent of temperature and energy.
II. Carrier mobility dependency to different edge roughness scattering rates particularly in MCW-GFET with a GNR array
III. In regards with the metal electrode/graphene contact, the general mechanism that is being considered in this calculation is truly ohmic contact with resistance inside the device is considered at the boundary of the n+ layer and n layer between the FET channel and the source and drain. No contact resistance arising from the difference in work functions between metal/graphene being considered. There is a need to consider the contact resistance arising from the metal/graphene junction in future works. Details of the contact resistance can be refered in several other literatures. [128,129]

The bandgap need to be further enhanced as the bandgap opening in the MCW-

GFET is not high enough for a usual integrated circuit. Further investigations on scaling down of the width of GNR are expected; ab-initio calculation by previous studies reported that a GNR with a width of 4.4 nm can yield an approximately 310 meV bandgap [130]. Moreover, edge states modulation by doping or other methods which are discussed in chapter 1 can be used to enhance the bandgap opening in modulated region.

It is equally exciting if the fundamentals and design principle of this new structure can be further extended to improve and remove the limitations in any other devices with different material. That being said, the proposed structure should open a new outlook on how simple designs making use of phenomenon such as the overshoot velocity to enhance transport properties in devices.

6.2.2 GNR Intercalation

In terms of the intercalation of interconnect, the same theoretical method can be done on other intercalation compound to compare and evaluate the most stable compound. However, ab-initio calculation with wider GNR width need to be done to better understand the mechanism behind the stability of intercalated GNR other than binding energy. The bonding between the intercalation compound that gives rise to the binding energy between the GNR layers need to be further investigated and discussed. On the other hand, to further optimized the MD simulation, other potentials such as AIREBO potential [131] that defines the interaction between carbon atoms inside graphene more precisely need to be considered. In addition, force field and potential from other experimental and theoretical studies need to be used to better understand how to create stable intercalation structure. In further determining the stability of the intercalated structure, other condition such as an ambient atmosphere or in other realistic device environment need to also be considered since the chemical reaction with water or oxygen in air will most probably affect the stability of this structure.

Along with determining a stable intercalated structure, to search for the most suitable and promising candidate as an intercalation compound in GNR interconnects, charge transfer that contributed to the Fermi level shift inside GNR host need to be considered. This means that intercalation compound that transfer higher amount of charges to GNR host is more feasible to be used as an intercalation compound. It is not possible to use an intercalation compound that is stable inside the GNR host but is not

able to transfer a minimal charge to shift the Fermi level. The best candidate satisfies both being stable and being able to shift the Fermi level of GNR interconnects to 1.0 eV.

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APPENDIX

A-1. Structure Optimization (*W*, Modulation Region, Modulation Length)

Further investigation on the dependence of transit time and the width ratio, *W*, Modulation Region, X_N and modulation length L_M to optimize the device performance in the bilayer MCW-GFET is done. From the results shown in Fig. A1, it is found out that it is best by placing the notch slightly inside the source region as the result suggested that stronger electric field outside the source region (inside channel region) only gave little impact to the carrier acceleration. The result also suggests that there ss an optimum modulation length for the MCW structure. This is due to the fact that there is no stronger electric field in longer modulated channel. In the MCW-GFETs that are demonstrated here, the best result is achieved when the modulation length is half of the channel length, which is 50 nm. When varying the width ratio W = 0.1~1.0. it is found that the transit time is fastest at W= 0.1. There is almost no change in the transit time when the width ratio is larger than 0.4, indicated by the w of 0.4, 0.5 and 0.6 results in Fig. A2.

To explain this, when observing the electric field profile of those cases, it is found out that there is stronger local electric field introduced in those structures. However, the electric field is not high enough to shifts the electron distribution to larger k and higher energy region. Since the carrier distribution in those cases stay in the low energy region where the dispersion is almost flat, the saturation velocity is almost identical, resulting a similar transit time. Hence, there is a minimum value of the electric field that depends on the width ratio in order to shift the carrier distribution to region with higher maximum group velocity.

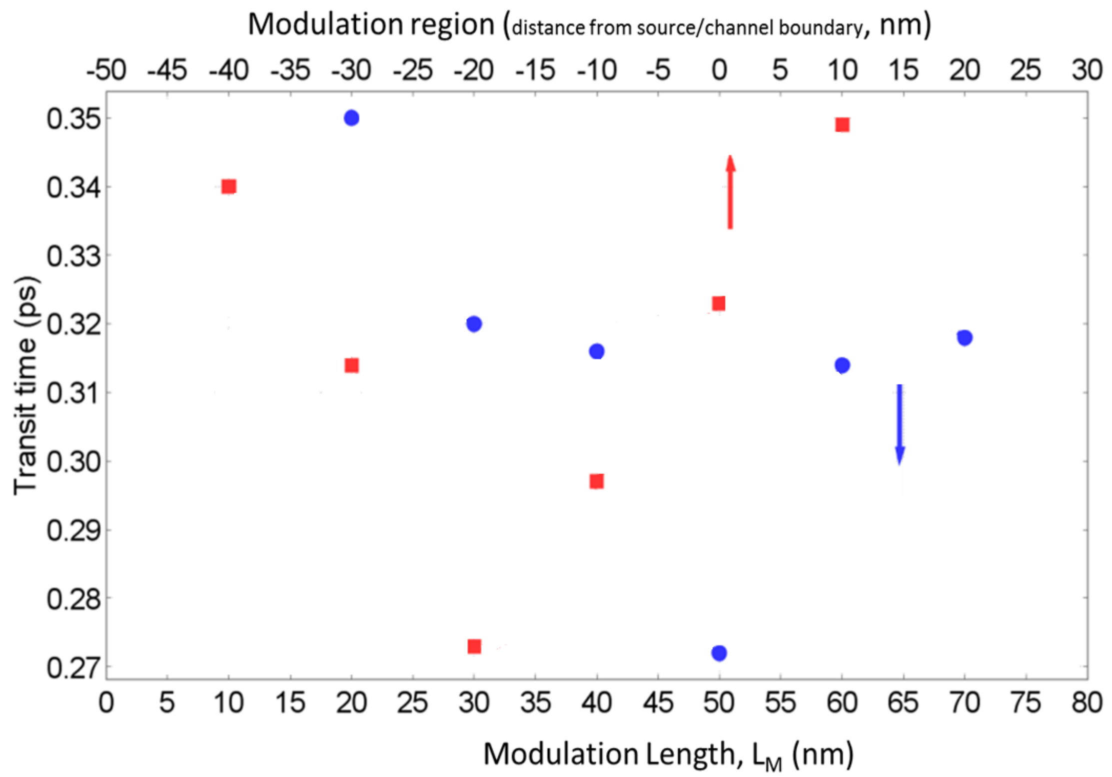

Fig. A1: Transit time of Bilayer MCW-GFET with various modulation region and length

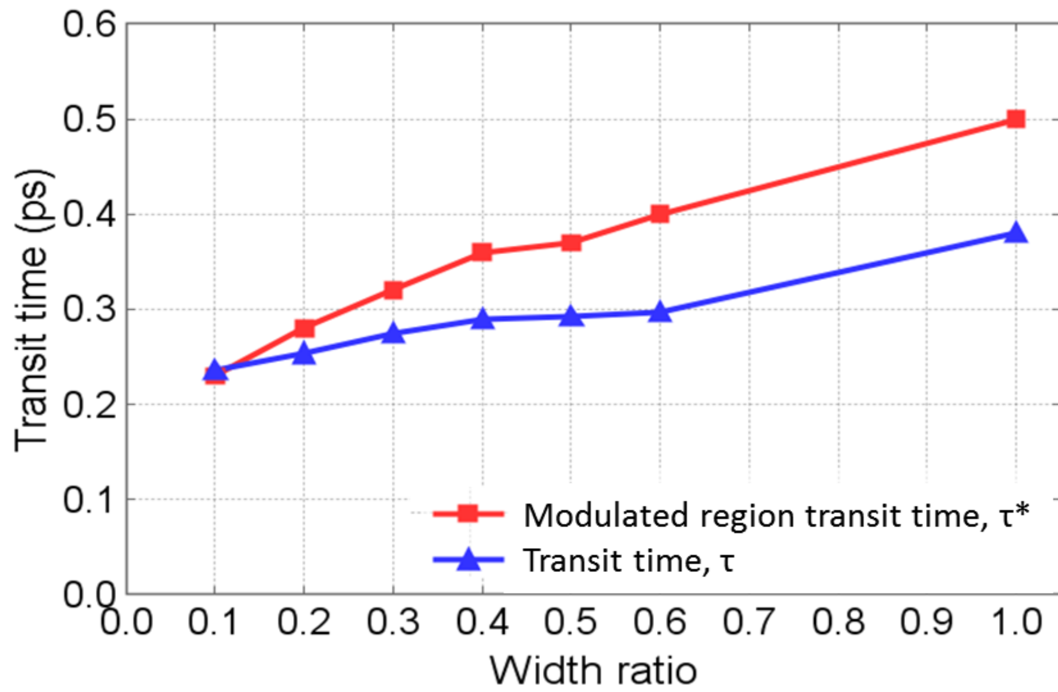

Fig. A2: Transit time in MCW-GFET with various W (bilayer channel). Transit time, τ is the travelling time of the carrier from source to drain (X =100 nm~200 nm). Modulated transit time, τ* is the travelling time of the carrier from the starting point of the modulated region (X = 80 nm) until the carrier exit the end of the modulated region at (X = 130 nm)

A-2. Channel design to reduce quantum reflectance effect

Since the effect of quantum reflectance on the carriers which occurs at the boundary between graphene with a wide width and and the narrow MCW region channel width is not considered in this calculation, it is important that the transit time in modulated channel region with a gradual modulation where the effect of quantum reflectance can be neglected is also calculated. Therefore, MCW regions with abrupt channel width modulation and gradual modulation are calculated as shown in Fig. A3. The result suggested that although the abrupt modulation is favorable with design (a) showing the fastest transit time, gradual modulation which is considered in design (e) also shows enhanced transit time which is second best to the abrupt modulation (a). Therefore, this suggests that the MCW effect can also be seen in gradual modulation where quantum reflectance can be neglected.

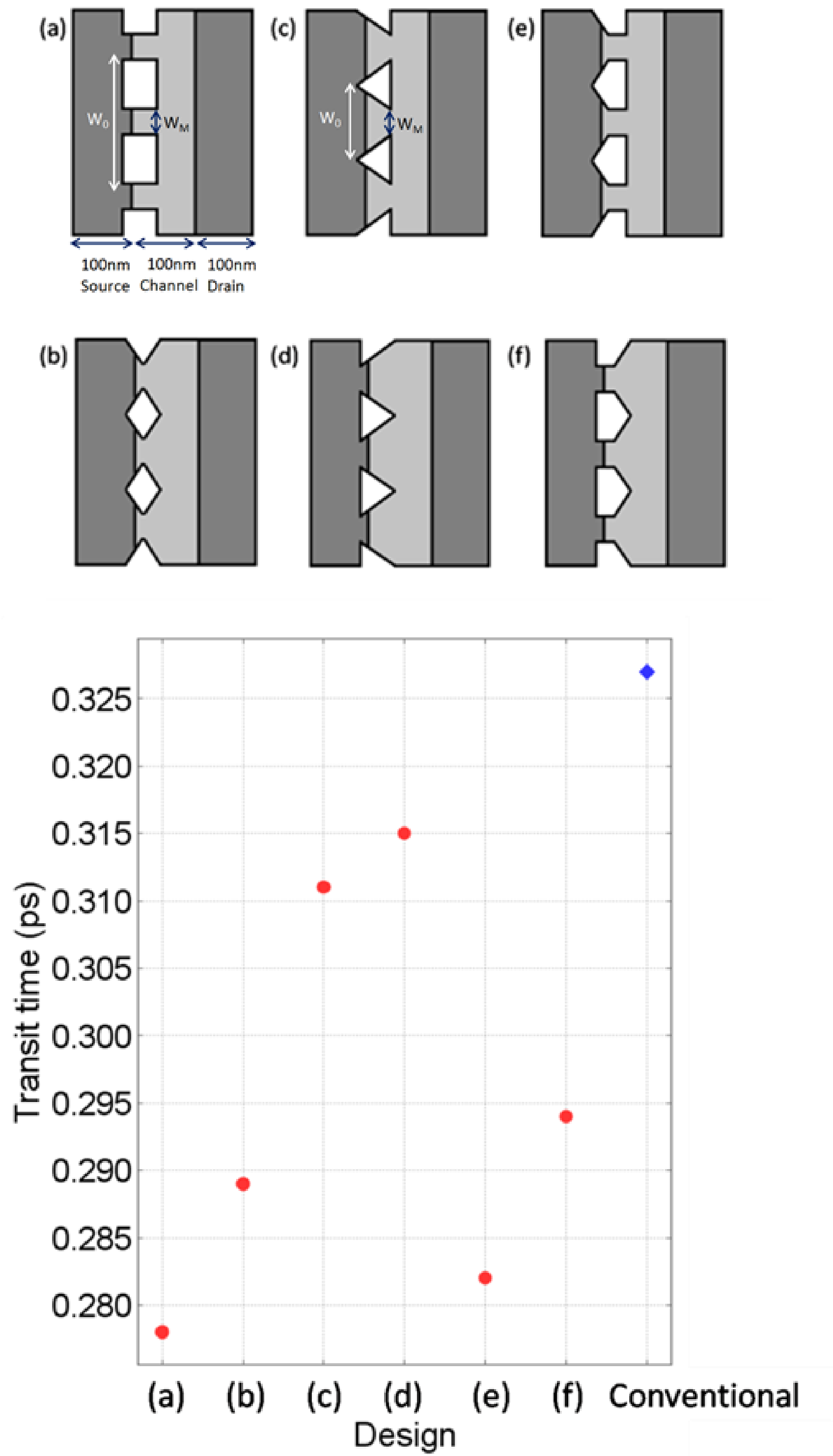

Fig. A3: Transit time in MCW-GFETs with different design where gradual design is being considered to lower the effect of quantum reflectance

A-3. Current and Voltage characteristic inside MCW-GFET

Other than evaluating the transit time inside this MCW-GFET device, the drain current and top-gate voltage is also calculated and compared to a conventional GFET. The result is shown in Fig. A4. In this calculation the top-gate voltage, V_{TG} is being varied form 0 to 0.5 V with drain source voltage, V_{DS} is set to be 0.5 V. From the result it is found out that the current ratio, $I_{VTG=0.5}/I_{VTG=0}$ in MCW-GFET is 21 while is 10 in conventional graphene. This shows that the ratio is improved in MCW-GFET when considering the region where gate voltage is limited to 0~0.5 V. This is due to suppressed $I_{VTG=0}$ in MCW-GFET since it has a 100 meV which is absent in conventional GFET. Since the channel width is being narrowed forming GNR arrays in MCW-GFET, $I_{VTG=0.5}$ is 6 times lower than in conventional GFET. $I_{VTG=0.5}$ in MCW-GFET is 9.4 mA while is 54.3 mA in conventional GFET. This lower current will be compensate by larger 2 times larger ratio and faster carrier velocity inside MCW-GFET.

Although a more general way of evaluating the current ratio inside FETs is by calculating the on-off current ratio and subthreshold slope, this evaluation of current ratio (V_{TG} = 0~0.5 V) is done while considering that the off current cannot be simulated precisely in Monte Carlo calculation. There is a limitation to precisely simulate the current-voltage characteristic at subthreshold regime where noise signal is apparent due to the stochastic nature of Monte Carlo method [132]. An advanced version of a more complex Monte Carlo Simulation need to be considered in order to calculate the precise on-off current ratio and subthreshold voltage.

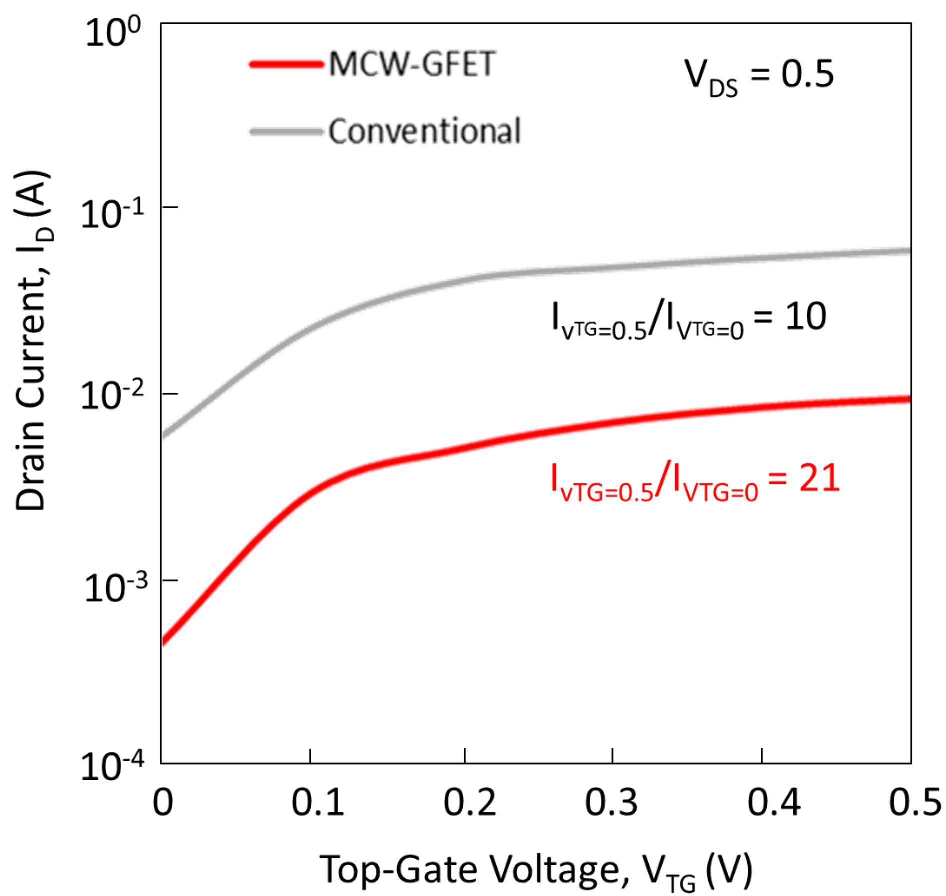

Fig. A4: Drain current vs topgate voltage in MCW-GFET and conventional GFET