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Keio University

Thesis Abstract

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Thesis Title

Theoretical studies on device structure and material design for high performance graphene nanoribbon devices and interconnects towards future LSI applications

Thesis Summary

Recently found in 2004, graphene is a two-dimensional material consisting of carbon atoms being bonded in a honeycomb lattice structure. Its exceptional electrical and thermal properties such as high carrier mobility and high breakdown current make graphene a highly promising candidate to replace silicon and cupper for future electronics application including in electron device and interconnect technologies in LSIs. Although there are advancements in the development of graphene devices and interconnects, there are critical issues that need to be solved in order to realize such applications. To date no solution is being realized to solve the issue of graphene device having no bandgap without having to compromise the high speed performance of the device. In interconnects, edge scattering leads to high resistivity graphene nanoribbon (GNR) wire while doping such as by intercalation can reduce its resistivity. However the stability of intercalated GNR interconnects has not been studied systematically. Accordingly, the main objective of this thesis is to provide solution to these crucial issues by theoretically studying the feasibility of graphene structural modification both in graphene electron devices and interconnects. A novel Graphene Field Effect Transistor (GFET) structure is proposed in which high velocity property enhancement and bandgap opening are possible. The feasibility of intercalated GNR interconnects is also investigated by simulating its stability for the first time. The estimation can provide a guideline to achieve stable intercalated GNR structures for low resistivity interconnect applications.

Chapter 1 provides the general background of current LSI technologies and summarizes the issues of conventional silicon FETs and copper interconnects, and the objectives of this study.

Chapter 2 describes the theoretical framework that is used in this study which consists of Monte Carlo, ab-initio and molecular dynamics simulation methods.

In Chapter 3, in order to enhance the high speed performance of GFET, a new structure of GFET, a Modulation Channel Width-GFET (MCW-GFET), is proposed where the channel is locally modulated by narrowing the width. A Monte Carlo device simulation method is used to simulate electron transport and electrical properties of MCW-GFETs. The electron mean velocity profile shows an abrupt increase near the source side of the channel where the electric field becomes very high, which is because the channel width is narrowed. This leads to a 54% and 30% faster local transit time in bilayer and monolayer graphene channel, respectively.

In Chapter 4, an advanced structure of MCW-GFET is proposed by introducing GNR stripes at the modulated region in order to enable a bandgap opening and enhance its high speed properties. The bandgap opening in GNR is calculated using ab-initio method while device simulation is run using Monte Carlo device simulation. The velocity of the MCW-GFET is comparable to of a conventional GFET despite having a 100 meV bandgap opening. When compared to of an InP-based High Electron Mobility Transistors with the same channel length, a 100-nm-long channel MCW-GFET has approximately 1/3 shorter transit time.

Chapter 5 describes the study of intercalated GNR interconnect stability. Calculation is done using ab-initio and molecular dynamics methods. In both calculations, it is found that there is a width dependency to the stability of the GNR. The results also suggest that there is an optimum intercalation ratio.

Chapter 6 is the conclusion and the future perspectives of this thesis.