A Thesis for the Degree of Ph.D. in Engineering

Design Automation and Optimization of Inductive Coupling Interface

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Thesis Abstract

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Thesis Title

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Thesis Summary

As manufacturing cost in keeping up with the Moore's Law grows exponentially, the idea of three-dimensional (3-D) integrated circuit (IC) technologies become promising solutions in facing the ultimate physical challenges. In recent years, the ThruChip interface (TCI) becomes one of emerging 3-D stacking technologies. TCI is a wireless interface for stacking chips vertically. Due to its wireless nature, TCI can integrate IC products with low fabrication cost in comparing to wiring solution while offering good communication reliability and high data bandwidth. Although TCI has been researched in diverse applications for years, the TCI design automation and influences of physical structures, such as power mesh and dummy metal fill, have not been explored. Without this information, designers may design TCI too conservatively and CAD engineers are unable to realize design automation. As a result, in order to enrich TCI design methodologies, this thesis focuses on discussing TCI extensive design automation and optimization topics in physical design guidelines, inductive coupling coil, and 3-D FPGA system.

Chapter 1 introduces the background of challenges in modern semiconductor industry, the potential solutions in wiring/wireless 3-D IC integration technology, the basic concept of TCI, and the scope of this thesis.

Chapter 2 presents TCI physical design guideline experiments in exploring the dependence between power consumption and D/Z ratio, power mesh impact, and dummy metal impact. The experiment results show that keeping the TCI coil diameter (D) and communication distance (Z) ratio to three is the optimal ratio and enlarging D/Z to six can further reduce total power by 20%. The eddy current on power mesh can cause TCI to fail. Creating a minimum space chop on power mesh can effectively recover TCI communication from eddy current impact with only additional 0.6% voltage drop. Dummy metal fill structure has no impact on TCI.

Chapter 3 introduces an analytical TCI inductive coupling coil design optimization methodology. The optimization results show that the proposed flow can improve mutual inductance value by 17% on average in comparing to baseline cases in chapter 2 and save the design time from days to minutes.

Chapter 4 presents the novel TCI based 3-D field programmable gate array (FPGA) architecture exploration framework. This chapter gives an overview of placement, routing, timing optimization, and noise avoidance design flow in TCI based 3-D FPGA system and raises issues that the architecture may encounter while adopting TCI. The experimental results show the proposed 3-D FPGA architecture can reduce delay by 25% on average over 2-D FPGA. Although the performance of TCI based 3-D FPGA architecture is 8% worse than through-silicon-via (TSV) based 3-D FPGA on average, TCI based architecture can reduce active area consumed by vertical communication channels by 42% on average and thus lead to better area and delay product.

Chapter 5 summarizes this thesis and revisits the objectives of this study. An overview of future work is also given.