A Study on Power Saving and Latency Reduction Methods for Wireless 3D Network on Chips

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Thesis Abstract

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Thesis Summary

By the development of semiconductor technology, we can combine various IP cores such as processors, caches, and I/O modules on a chip. To connect a large number of cores, Network-on-Chip (NoC) that introduces a packet switched network has been widely studied. NoCs have been utilized in cost-effective embedded devices. Such applications often demand very tight design constraints in terms of cost and performance; thus the silicon budget available for their on-chip network should be modest.

Due to the increasing design cost of custom System-on-Chips (SoCs) in recent process technologies, System-in-Packages (SiPs) or 3D ICs that can select and stack necessary known-good-dies in response to given application requirements have become one of hopeful design choices. The three-dimensional Network-on-Chip (3D NoC) also becomes an emerging research topic. The 3D NoC architecture has been extensively studied in terms of its network topology, router architecture, and routing strategy.

We pay more attention to inductive coupling among variety 3D interconnection technology, because we believe it provides the flexibility to build the target 3D ICs by adding, removing, and swapping chips in a package after the chips have been fabricated, like building blocks.

However, two issues emerge: considerable huge power consumption and routing scheme for topology-agnostic characteristic. Only a few inductors can be embedded on the chip, because the total power consumption will be unacceptable. This issue effects the scale of wireless 3D NoC. For the routing scheme, the previous works never involve this issue for inductive coupling based wireless 3D NoC. The above problems must be solved, otherwise the inductive coupling based wireless 3D NoC will not be competitive.

For the above aim, this thesis explores an effective low power technology for ring and irregular based networks, respectively. The vertical links can be dynamically shut down according to the run-time vertical link utilization. Two suitable routing schemes for topology-agnostic wireless 3D NoC are also proposed that enable the chip could be replaced or removed after fabrication. The first one collects topology information at the chip boot stage. The topology will be considered as irregular topology. The Up*/Down* routing is used for transferring packets; Then second one identifies mesh topology from the whole network which is considered as irregular topology by the first routing scheme, automatically. It uses dimension ordered routing in the extracted mesh structure as far as possible. Other parts of the network is treated as an irregular network and Up*/Down* routing is applied. These above technologies can enhance the competence of inductive coupling based wireless 3D NoC.

Finally, we summarize our proposed methods, utilizing the on/off vertical link technique for saving power and employing improved Up*/Down* routing and mixed routing as routing scheme. Based on the above, we discuss how the current work could be explored further in order to develop power efficient wireless 3D NoC.