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Keio University

Thesis Abstract

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Thesis Title

Partial Reconfiguration Implementation on Fluid Dynamics Computation Using an FPGA

Thesis Summary

The field of high performance scientific computing lies at the crossroads of many disciplines and skill sets. Scientific computation from an application context makes some acquaintance with physics and engineering sciences. Then, problems in these application areas are solve using scientific processes, and the use of computers for numerical analysis to produce quantitative results. An efficient implementation of the practical formulations of the application problems requires some understanding of computer architecture, both on the CPU level and on the level of parallel computing.

One of the high performance computing (HPC) applications is computational fluid dynamics (CFD). In aerospace industry, CFD is used as a common design tool. It presents scientific computation methods to analyze fluid behavior for designing aircraft components such as engines and wings. Therefore, software packages for CFD are needed for aeronautical engineers and researchers. However, enormous floating-point calculations cause a long execution time required to simulate complete aeronautics configurations. It remains as a bottleneck in the design flow of new structures for the aircraft design. Thus, reducing the total execution time for aerodynamics analysis is one of the important challenges of current research in this field.

Recent advances in Field Programmable Gate Array (FPGA) technology make reconfigurable computing using FPGAs an attractive platform for accelerating scientific applications. The readily availability and high-power efficiency of high-density FPGAs make them attractive to the HPC community. Since their invention in the mid-1980s, FPGAs have been used to accelerate high performance applications on custom computing machines. Under such circumstance, a new type of computational systems is being focused for allocating a part of scientific operations to dedicated hardware in order to achieve both low-cost and high-performance.

In this thesis, two CFD codes are studied: UPACS (Unified Platform for Aerospace Computational Simulation) and FaSTAR (Fast Aerodynamics Routines) software packages. The problems of these codes are hard to be executed in parallel machines because of their irregular and unpredictable data structure. In addition, a single FPGA is not enough for the software packages because the whole modules are very large. Exploiting reconfigurable hardware with their advantages to make up for the inadequacy of the existing high performance computers has gradually become the solutions. Instead of using a large number of chips, partially reconfigurable hardware available in recent FPGAs is explored for these applications.

With the above aim, this thesis explores scientific computation of CFD applications and implements the target subroutines in FPGA by utilizing partial reconfiguration technology. The goal of this work is to achieve high performance compared to microprocessor execution and to clarify the relationships among hardware resources utilization, configuration time and performance according to the evaluation results.

UPACS developed by JAXA (Japan Aerospace Exploration Agency) is one of CFD packages to simulate compressible flow using multi-block grids. MUSCL (Monotone Upstream-centered Schemes for Conservation Laws) scheme in UPACS is chosen as a target subroutine, since it is used twice in core routine of UPACS. Partial reconfiguration is applied to the flux limiter functions (FLF) in MUSCL. Two types of partially reconfigurable design are implemented that are static and dynamic reconfigurations. Four FLFs are implemented for Turbulence MUSCL (TMUSCL) and eight FLFs are for Convection MUSCL (CMUSCL). In statically reconfigurable design, the implementation has successfully reduced the resource utilization by 44% to 63%. Total power consumption was also reduced by 33%. Configuration speed was improved by 34 times faster as compared to full reconfiguration method. In dynamically reconfigurable design, the implementation has successfully reduced resources utilization by 60%. Total power consumption was also reduced by 29%. Configuration speed was improved by 15 times faster compared to fully reconfiguration method. Both implementations also achieved at least 17 times speed-up compared with the software execution.

FaSTAR, another CFD package developed by JAXA, supports several solvers and adopts unstructured mesh as its grid form. The advection term computation module in FaSTAR is chosen as a target subroutine, which a time-consuming and large function. Therefore, a partially reconfigurable flux calculation scheme that would fit in a single FPGA was proposed. The flux computational module was developed and five flux calculation schemes were implemented as reconfigurable modules, these were: Roe, HLLE, HLLEW, AUSM^{+}-up, and SLAU. The implementation of this module has the advantages of saving up to 62.75% of resource and increasing the configuration speed by a factor of 6.28. Performance evaluation also shows that 2.65 times more acceleration was achieved compared to the Intel Core 2 Duo at 2.4 GHz.

Finally, we summarize our proposed implementation method, utilizing the partial reconfiguration technique for saving hardware resources and achieving faster performance in comparison with software execution. Based on the above, we discuss how the current work could be explored further in order to develop the scientific applications of FPGAs.