Title	Transient temperature behavior of transistor junctions under pulse operation
Sub Title	
Author	鈴木, 登紀男(Suzuki, Tokio) 広瀬, 治男(Hirose, Haruo)
Publisher	慶応義塾大学藤原記念工学部
Publication year	1966
Jtitle	Proceedings of the Fujihara Memorial Faculty of Engineering Keio University (慶応義塾大学藤原記念工学部研究報告). Vol.19, No.75 (1966.) ,p.199(43)- 209(53)
JaLC DOI	
Abstract	Based on the equivalent circuit approach, the temperature behavior of the transistor junction is investigated through the experiments. It is clarified for pulse operation that a few RC pairs present sufficiently good approximation to the junction temperature variation at a dynamic quasi-steady state. When mean power performance is considered, a low frequency pulse operation should require a transistor with negligibly small thermal resistances accompanied with small thermal time constants and with relatively high thermal resistances of large time constants.
Notes	
Genre	Departmental Bulletin Paper
URL	https://koara.lib.keio.ac.jp/xoonips/modules/xoonips/detail.php?koara_id=KO50001004-00190075-0043

Transient Temperature Behavior of Transistor Junctions under Pulse Operation

(Received December 5, 1966)

Tokio SUZUKI*
Haruo HIROSE**

Abstract

Based on the equivalent circuit approach, the temperature behavior of the transistor junction is investigated through the experiments. It is clarified for pulse operation that a few *RC* pairs present sufficiently good approximation to the junction temperature variation at a dynamic quasi-steady state.

When mean power performance is considered, a low frequency pulse operation should require a transistor with negligibly small thermal resistances accompanied with small thermal time constants and with relatively high thermal resistances of large time constants.

I. Introduction

Semiconductor devices which prevail these days have yet many problems to their applications to solve. Especially the thermal effects on the devices always bring them the serious limitation of possible power dissipation and sometimes the deterioration and the break-down. The temperature rise in the device often results in the variation of the characteristics that gives the design a lot of troubles, so it is significant and fatal that the thermal effects should give strong influence on the semiconductor devices.

Of the usual transistors, the upper limit of the temperature is given as 80°C for Ge devices and 150°C for those of Si when transistors may be operated in good conditions, therefore the possible collector dissipation decreases rapidly as the ambient temperature becomes higher. At pulse operation, the collector junction of the transistor behaves like the voltage across the *RC* parallel-series circuit that is driven by the pulse current source. This is measured by I_{cbo} method 1) 2) and the thermal impedances of the transistor from the equivalent concept give us a precise information of the behavior of the junction temperature under pulse operation. It is pointed out from the experimental results that the junction temperature becomes

---

*鈴木登紀男 Associate Professor, Faculty of Engineering, Keio University.
**広瀬治男 Instructor, Faculty of Engineering, Keio University.

1) T. Suzuki and H. Hirose, This PROCEEDINGS Vol. 19, No. 69, pp. 18—25 1965.

2) T. Suzuki and H. Hirose, This PROCEEDINGS to be published.

dangerously high when pulse powers are applied without consideration of the thermal time constants of the transistor.

II. Thermal impedance of transistors

Generally heat dissipation is achieved in three ways, i.e. conduction, convection and radiation. However we should take an interest only in the conduction of heat from the collector junction to the surroundings because convection will give a small contribution to the heat dissipation in the transistor itself, and radiation is negligible in the temperature range concerned. Of course in actual circuit applications the final heat flow from the junction will be done by the convection from the capsule into the air. But in our experiments, the test transistor is put into the oil bath so that the capsule temperature of the transistor is held constant. Therefore the conduction of heat is considered exclusively.

The equation for the present problem is the so-called diffusion equation

$$\nabla^2\phi = \frac{1}{h^2}\frac{\partial\phi}{\partial t} \tag{1}$$

where

$h^2 = k/cd$	diffusivity	($\mathrm{m}^2\ \mathrm{sec}^{-1}$)
$k =$	thermal conductivity	(Watt m^{-1} deg^{-1})
$c =$	specific heat	(Joule Kg^{-1} deg^{-1})
$d =$	density	(Kg m^{-3})

The time-term can be separated from the equation (1) and gives[3]

$$\frac{dT}{dt} + \frac{T}{\tau} = 0$$

$$T = e^{-\frac{t}{\tau}} \tag{2}$$

where

$\tau = \gamma^2 h^2$

$\gamma^2 =$ separation constants

The remainder is the Helmholtz equation that we could not solve without explicit boundary conditions expressed in an adequate coordinate system. However, assuming that the solution of the Helmholtz equation is presented as ψ, we could obtain the total solution as

$$\phi = \sum_{n=1}^{\infty} \psi_n e^{-\frac{t}{\tau_n}} = \sum_{n=1}^{\infty} \phi_n \tag{3}$$

where

$$\phi_n = \psi_n e^{-\frac{t}{\tau_n}}$$

---

[3] Moon, P. & Spencer, D. E. "Field Theory", VAN NOSTRAOND Co. 1961, p. 413.

Now we are interested only in the tempepature of the junction region, P. R. Strickland modified[4] the equation (2) into the form as follows

$$\frac{d\phi_n}{dt}+\frac{\phi_n}{\tau_n}=C_n\frac{d\phi_n}{dt}+\frac{\phi_n}{R_n}=0 \tag{4}$$

and if the space average of ϕ over the junction region is taken, the average of each ϕ_n is the same as the voltage across RC parallel circuit as shown in Fig. 1.

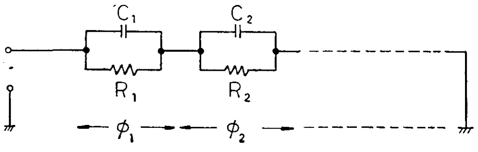


Fig. 1. Electrical analogue for the junction temperature. (ambient temperature be zero)

Therefore, when the pulse power is cut off, the temperature can be considered analogously as the voltage in the equivalent circuit. In general, τ_n contains the eigen value and numbers of n are infinite, but a good approximation can be obtained with two or three τ_ns for the pulse power used in the experiments as illustrated in the following section.

III. Equivalent circuit consideration and approximation of the junction temperature under pulse operation

When the pulse power (peak power P, repetition period T and width w) is applied to the collector junction of the transistor, by means of electrical analogue, the maximum voltage across the RC parallel-series circuit of Fig. 2 will be expressed in the time interval T

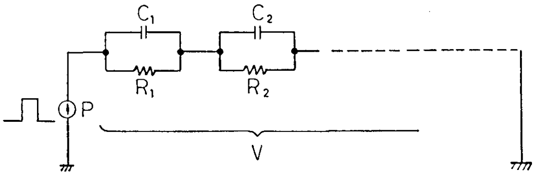


Fig. 2. Equivalent circuit for pulse operation.

$$V_{max}=PR_1\left(1-e^{-\frac{w}{R_1C_1}}\right)\sum_{k=0}^{m}e^{-\frac{kT}{R_1C_1}}+PR_2\left(1-e^{-\frac{w}{R_1C_1}}\right)\sum_{k=0}^{m}e^{-\frac{kT}{R_2C_2}}+\ldots\ldots \tag{5}$$

where the time t starts when the first pulse power is added to the junction and m is $[t/T]$ Gaussian symbol.

---

[4] Strickland, P. R.; IBM JOURNAL JAN. 1959, pp 35—45.

After a sufficiently long time a dynamic quasi-steady state is realized and

$$V_{max} = PR_1 \frac{1-e^{-\frac{w}{R_1C_1}}}{1-e^{-\frac{T}{R_1C_1}}} + PR_2 \frac{1-e^{-\frac{w}{R_2C_2}}}{1-e^{-\frac{T}{R_2C_2}}} + \ldots\ldots \tag{6}$$

whereas *dc* power gives

$$V_{dc} = PR_1 + PR_2 + \ldots\ldots \tag{7}$$

The temperature rise under the pulse operation is smaller than that of *dc* operation as far as the peak power is kept constant because the *RC* parallel circuit always offers a smaller impedance for an *ac* source than for *dc* one.

If the average power dissipation under pulse operation be adopted as the measure of the maximum power dissipation of the devices, there would arise a problem:

Now, suppose a transistor have a maximum power dissipation P_0, then the peak power would be P_0T/w where T and w are repetition period and width respectively, though the mean power is P_0. The temperature rise is obtained under the above mentioned pulse power as

$$\Delta T_j = T_1 \frac{T}{w} \frac{1-e^{-\frac{w}{R_1C_1}}}{1-e^{-\frac{T}{R_1C_1}}} + T_2 \frac{T}{w} \frac{1-e^{-\frac{w}{R_2C_2}}}{1-e^{-\frac{T}{R_2C_2}}} + \ldots\ldots \tag{8}$$

where

$$T_1 = P_0R_1, \qquad T_2 = P_0R_2 \;\ldots\ldots$$

To estimate the temperature rise at the mean power consideration, we must know which term in the equation (8) is larger than that of *dc* value. This is accomplished by the comparison of $(T/w)\{1-\exp(-w/R_nC_n)\}/\{1-\exp(-T/R_nC_n)\}$ with unity, so it will be useful to reform the equation by means of approximation as follows;

$$\begin{aligned} \Delta T_j = & \underbrace{\frac{T}{w}\{T_1+T_2+\ldots\ldots+T_m\}}_{\text{Group 1}} + \underbrace{\frac{T}{w}\{T_{m+1}\,(1-e^{-\frac{w}{R_{m+1}C_{m+1}}}) + \ldots\ldots T_n\,(1-e^{-\frac{w}{R_nC_n}})\}}_{\text{Group 2}} \\ & + \underbrace{T\left\{\frac{T_{n+1}}{R_{n+1}C_{n+1}}\ldots\ldots+\frac{T_p}{R_pC_p}\right\}}_{\text{Group 3}} + \underbrace{T\left\{\frac{T_{p+1}}{1-e^{-\frac{T}{R_{p+1}C_{p+1}}}}+\ldots\ldots+\frac{T_q}{1-e^{-\frac{T}{R_qC_q}}}\right\}}_{\text{Group 4}}, \\ & + \underbrace{\{T_{q+1}+\ldots\ldots\ldots\}}_{\text{Group 5}} \end{aligned} \tag{9}$$

where

$R_1C_1 \sim R_mC_m \ll w < T$	Group 1
$R_{m+1}C_{m+1} \sim R_nC_n \approx w < T$	Group 2
$w < R_{n+1}C_{n+1} \sim R_pC_p < T$	Group 3
$R_{p+1}C_{p+1} \sim R_qC_q \approx T$	Group 4
$T < R_{q+1}C_{q+1}\ldots\ldots$	Group 5

Each group in the equation is divided according to their time constants, comparing with the given pulse width and repetition period. The first group represents the remarkably high temperature rise if the ratio T/w could be large because each apparent resistance takes the *dc* value multiplied by the factor T/w. The last group shows the equal amount of resistance to the case of *dc* operation while all other groups remained offer somewhat larger values than those of *dc* power. This is easily understood by refering Fig. 3. Consequently, The sum of the resistances in the groups except the last one is of most interest in the present work. But the value of the summation of resistances in each group is dependent on the given pulse conditions that is, it varies with the pulse width and repetition period. Thus we should choose such a transistor for a given pulse power that the majority of thermal resistances of the transistor belongs to the last group in the above equation and all other resistances are negligible.

Actually, experimental errors will suppress small resistances and only relatively high resistances which are of most interest can be detected.

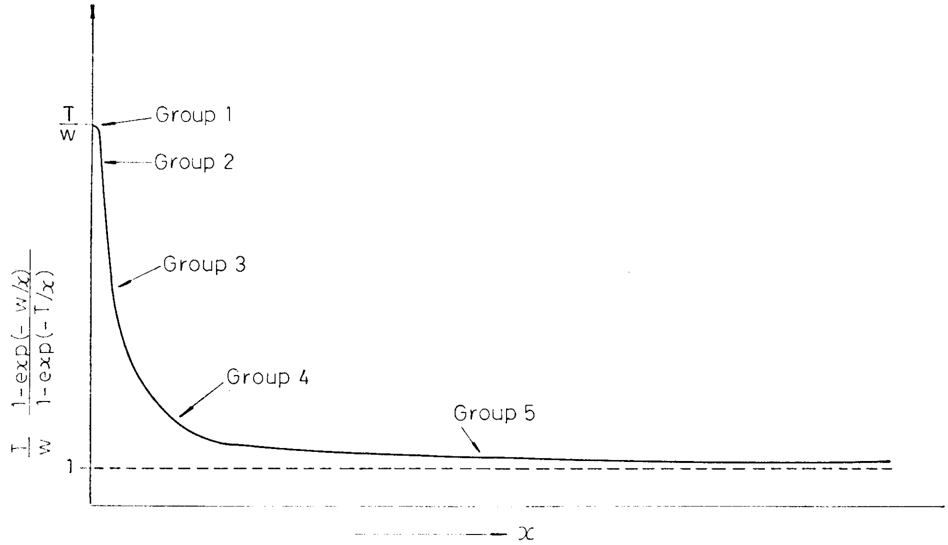


Fig. 3. Change of the factor $(T/w)\{1-\exp(-w/x)\}/\{1-\exp(-T/x)\}$ as x varies.

IV. Measurement of thermal impedance

The thermal impedance of the transistor can be measured by the equipment 1) 2) of which the block diagram is shown in Fig. 4. With use of the calibration curves for each transistor and the graphical method, the thermal impedances for several germanium transistors are estimated and tabulated as follows

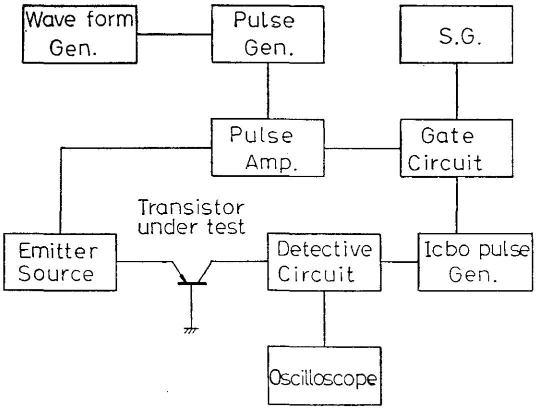


Fig. 4. Block diagram of the equipment for transient junction temperature measurement.

Thermal Impedance

Name of Transistors	R_1 $\frac{\text{deg}}{\text{Watt}}$	$C_1 \frac{\text{Watt ms}}{\text{deg}}$	τ_1 ms	R_2 $\frac{\text{deg}}{\text{Watt}}$	$C_2 \frac{\text{Watt ms}}{\text{deg}}$	τ_2 ms
2SB 44	2.77	2.82	7.8	114	3.20	365
2SB 75	3.06	3.34	10.2	165	3.42	565
2SB110	10.7	0.420	4.5	504	0.643	324
2SB170	negligible	——	——	384	2.68	1030

In the above experimentation, the given pulse power conditions are

Transistor	2SB 44	2SB 75	2SB110	2SB170
repetition period (ms)	100	50	48	100
pulse width (ms)	10	5	4.8	10
peak power (Watt)	4.0	2.0	1.0	1.6

The transient temperature behavior under the pulse operation is shown in Fig. 5 ($a \sim d$). which are translated from Photographs 1 ~ 8.

Photographs 1 ~ 8 demonstrate the temperature variation in I_{cbo} at the collector junctions of the corresponding transistors at the dynamic quasi-steady states while the pulse powers are at off-duty.

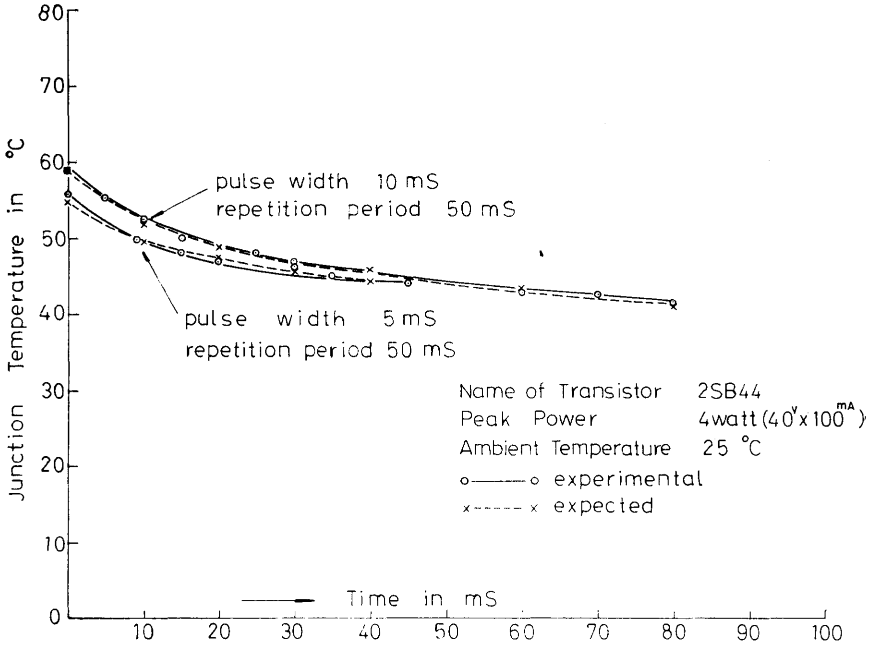


Fig. 5. (*a*)

Transient temperature behavior of transistor junction under pulse operation.

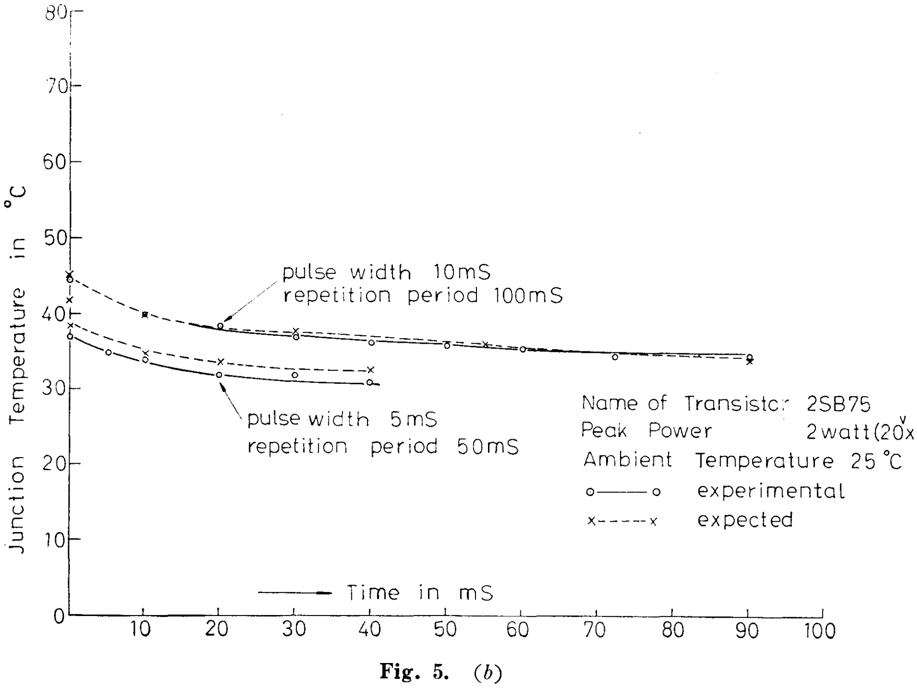


Fig. 5. (*b*)

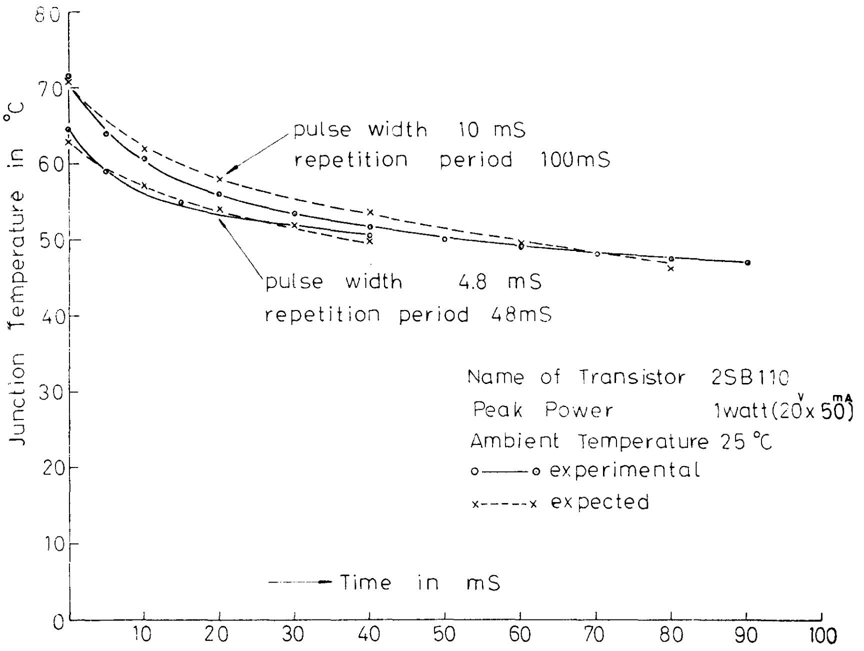

Junction Temperature in °C
80
70
60
50
40
30
20
10
0
pulse width 10 mS
repetition period 100mS
pulse width 4.8 mS
repetition period 48mS
Name of Transistor 2SB110
Peak Power 1watt(20V x 50mA)
Ambient Temperature 25 °C
o——o experimental
x-----x expected
Time in mS
10
20
30
40
50
60
70
80
90
100

Fig. 5. (*c*)

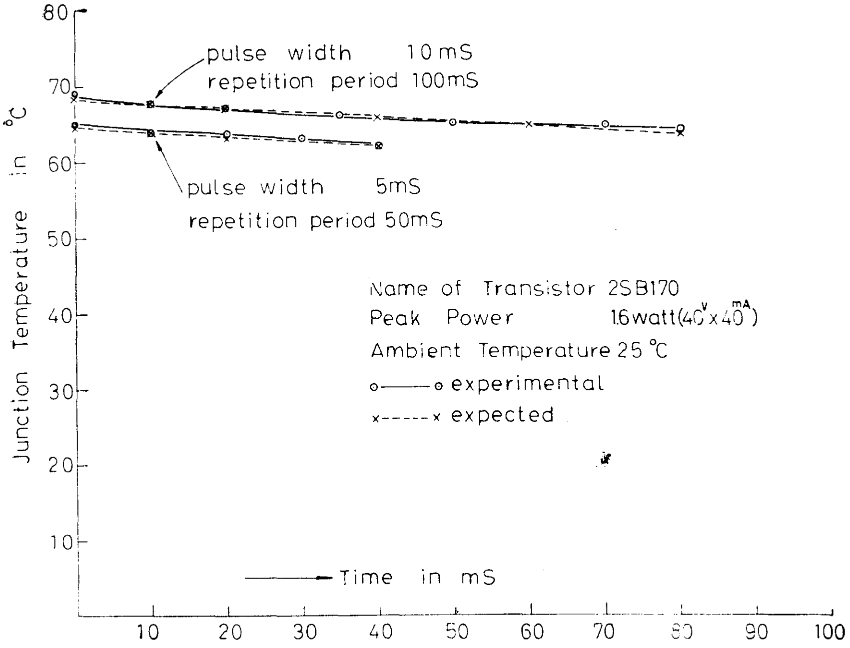
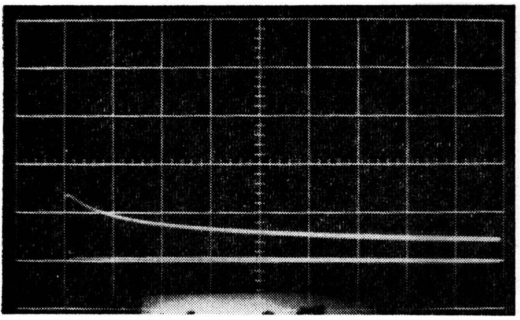

Junction Temperature in °C
80
70
60
50
40
30
20
10
pulse width 10mS
repetition period 100mS
pulse width 5mS
repetition period 50mS
Name of Transistor 2SB170
Peak Power 1.6watt(40V x 40mA)
Ambient Temperature 25 °C
o——o experimental
x-----x expected
Time in mS
10
20
30
40
50
60
70
80
90
100

Fig. 5. (*d*)

Photograph 1 ~ 8 The temperature variations in I_{cbo} at the collector junctions of the transistors at the dynamic quasi-steady states while pulse powers are at off-duty.

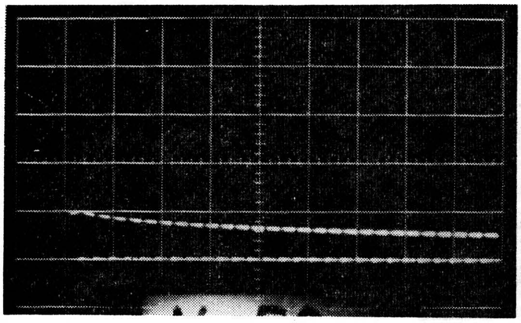


Photograph 1.

2SB 44

repetition period	100 ms
pulse width	10 ms
peak power	4 Watt

V : 0.5 V/div.
H : 10 ms/div.

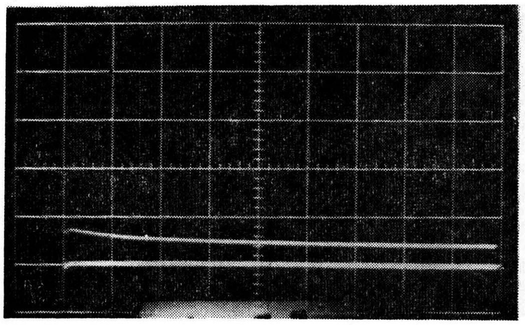


Photograph 2.

2SB 44

repetition period	50 ms
pulse width	5 ms
peak power	4 Watt

V : 0.5 V/div.
H : 5 ms/div.

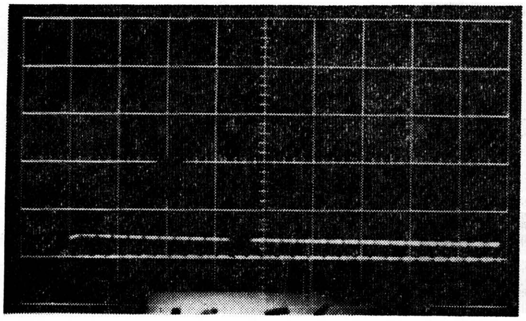


Photograph 3.

2SB 75

repetition period	100 ms
pulse width	10 ms
peak power	2 Watt

V : 0.5 V/div.
H : 10 ms/div.

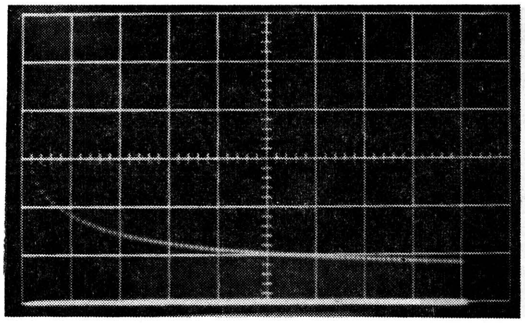


Photograph 4.

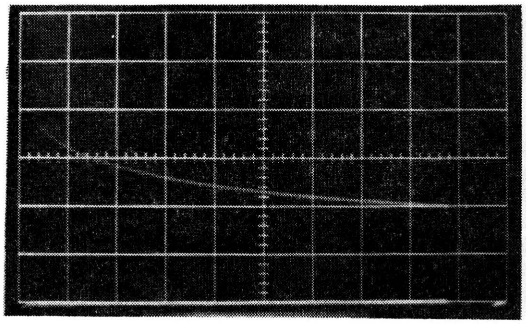
2SB 75

repetition period	50 ms
pulse width	5 ms
peak power	2 Watt

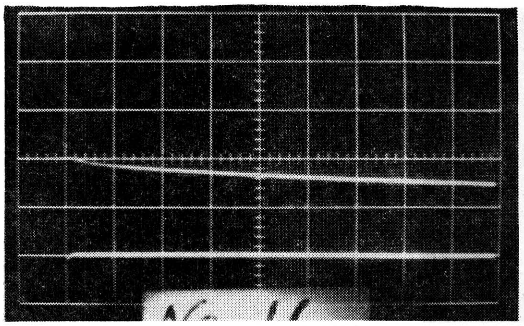
V : 0.5 V/div.
H : 5 ms/div.



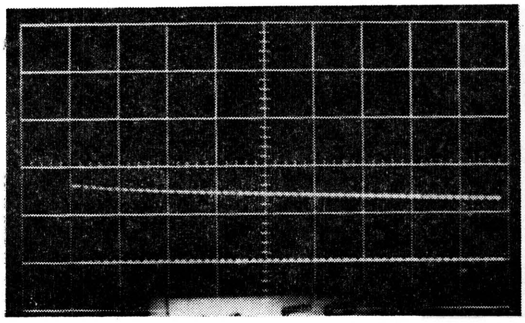
Photograph 5.
2SB110
repetition period 100 ms
pulse width 10 ms
peak power 1 Watt
V : 1 V/div.
H : 10 ms/div.



Photograph 6.
2SB110
repetition period 48 ms
pulse width 4.8 ms
peak power 1 Watt
V : 0.5 V/div.
H : 5 ms/div.



Photograph 7.
2SB170
repetition period 100 ms
pulse width 10 ms
peak power 1.6 Watt
V : 0.5 V/div.
H : 10 ms/div.



Photograph 8.
2SB170
repetition period 50 ms
pulse width 5 ms
peak power 1.6 Watt
V : 0.5 V/div.
H : 5 ms/div.

V. Discussion and conclusion

As seen in the former section, the temperature rises caused are different in their values and behavior though the average power is kept constant. The temperature dependency upon the pulse repetition period and width is in a sense very reasonable, but we are likely to ignor it because of no information of theraml impedances, therefore sometimes we get better performance and sometimes we can not or fail. In the latter case, responsible is not a transistor but users who hardly know the thermal impedances of the transistor.

It is of much importance and also of great difficulty to determine the ratings of the transistors in view of temperature rise, for deterioration or break-down of the transistor is not always caused by the large temperature rise of the junction. Even if the high temperature situation is produced by the applied pulse power the transistor may show no change on the characteristics as far as the duration of high temperature is extremely short. For the time being, the thresholds are not clarified against possible high temperature duration.

Problems are yet remained in the measurement of thermal impedances :

(1) I_{cbo} values are not the temperature itself but an integrated values that give an average temperature over the junction region.

(2) With the negative coefficients of electrical resistances to the temperature, the positive feed-back phenomena will occur on the junction area and then the current density at the high temperature region becomes much larger than the others in the area though the initial density is uniform. Furthermore, to estimate the dimension of the high current region is so much difficult, although these phenomena will take place in the usual transistor even at moderate operation.

(3) It will require the rigorous experimentation with considerable accuracy to determine the thermal impedance of the transistor, otherwise, the given information can not cover the temperature behavior under the pulse operation of which conditions are so different from those used in the measurement.

(4) Heat generation in other than the collector junction may contribute to some extent to the temperature rise of the junction, and the effect is now under consideration.

All the effects above mentioned must be investigated with regard to deterioration and break-down of transistors.

Acknowledgements

The authors wish to express their thanks to Prof. Yoshikazu Omoto and Prof. Motokichi Mori for helpful advices on the investigation of thermal problems of the transistor, further, the authors are grateful to Futoshi Kobayashi and Hideo Aoyagi for their helps in the experimentation.