

Cyclic Delay Estimation Schemes in Time Domain Cyclic Selective Mapping for Orthogonal Frequency Division Multiplexing Systems

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Thesis Abstract

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Thesis Title Cyclic Delay Estimation Schemes in Time Domain Cyclic Selective Mapping for Orthogonal Frequency Division Multiplexing Systems			
Thesis Summary Orthogonal frequency division multiplexing (OFDM) is a multicarrier transmission technique that has been recently adopted in many wireless communication standards. It has many advantages such as robustness to multipath fading and high spectrum efficiency. In spite of these advantages, OFDM suffers from its high peak-to-average power ratio (PAPR) signal which has become severe constraint in OFDM systems. The high PAPR may drive a power amplifier (PA) into a saturation region, cause interference among subcarriers, and corrupt the spectrum of the signal. In order to reduce the PAPR of the OFDM signal, many PAPR reduction schemes have been proposed and analyzed. Time domain cyclic-selective mapping (TDC-SLM) has been proposed to reduce the PAPR. At the transmitter side, the signal candidates (SCs) are generated by summing the original signal and its cyclic delayed versions. The SCs with the lowest PAPR are chosen for transmission. The conventional TDC-SLM scheme requires sending the amounts of cyclic delays as side information (SI) at a receiver side. In this dissertation, cyclic delay estimation schemes at the receiver side are proposed. The proposed schemes omit the transmission of the SI and improve the throughputs of the OFDM systems by up to 10%. Chapter 1 introduces the OFDM concept and wireless communication standards and the background of the research. The PAPR reduction schemes are then overviewed. The motivation of the research is represented in the last part of this chapter. In Chapter 2 a delayed correlation (DC) estimation scheme for TDC-SLM at the receiver side is investigated. At the transmitter side, only one mapping branch is assumed and a SC with the lowest PAPR is applied. At the receiver, DC is used to estimate the cyclic delay. The DC process multiplies the received signal in the time domain with the conjugate of the guard interval (GI) sequence. The PAPR reduction, the bit error rate performance, and the accuracy rate of the estimation are evaluated under various channel conditions. Chapter 3 proposes a DC-matched filtering (DC-MF) scheme that improves the DC estimation scheme in Chapter 2. The use of the MF makes the receiver be able to estimate the cyclic delays due to the generation of the SCs from multiple branches. TDC-SLM places the DC-MF after the frequency domain equalization (FDE) to remove the multipath components of the received signal. This proposed scheme is also evaluated with the nonlinear PA. Chapter 4 summarizes the results of each chapter and concludes this dissertation.			